100 MHz
VME FADC

User Manual

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Version: 2.11 as of 15.11.01

Revision Table:

Revision	Date	Modification
0.01	27.09.00	Generation
1.00	15.01.01	First official release
1.01	17.01.01	Trigger functionality added,
1.02	21.01.01	MBLT64 readout
1.03	01.06.01	Bug fix in acquisition register
1.10	01.08.01	**Documentation**: J190 description **Design Version 2 : (added Multiplexer Mode)** - Firmware Revision Register : 0x33000102 - new bit in Acquisition control register (bit 15; MULTIPLEXER Mode) - new Clock Predivider registers - new No_of_Sample registers - new Output 1 function in MULTIPLEXER Mode
2.00	29.10.01	V2 hardware revision, extended functionality
2.10	05.11.01	extended trigger functionality description
2.11	15.11.01	Bug fixes, ADC chip frequency range

1 Table of contents

2 Introduction

The SIS3300 is an eight channel ADC with a sampling rate of up to 105 MHz (for the individual channel) and a resolution of 12-bit. The board is a single width 6U VME card, which has no special (i.e. non standard VME) voltage requirements.
The two memory bank option in conjunction with multi event memory structure and a range of trigger options give the unit the flexibility to cover a variety of applications.
Applications comprise:

? digitization of “slow” detectors like calorimeters
? spectroscopy with Ge-detecors
? beam profile monitor readout
? serialised readout of ?-Strip detector data

As we are aware, that no manual is perfect, we appreciate your feedback and will try to incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under http://www.struck.de/manuals.htm. A list of available firmware designs can be retrieved from http://www.struck.de/sis3300firm.htm

3 Technical Properties/Features

3.1 Key functionality

Find below a list of key features of the SIS3300.

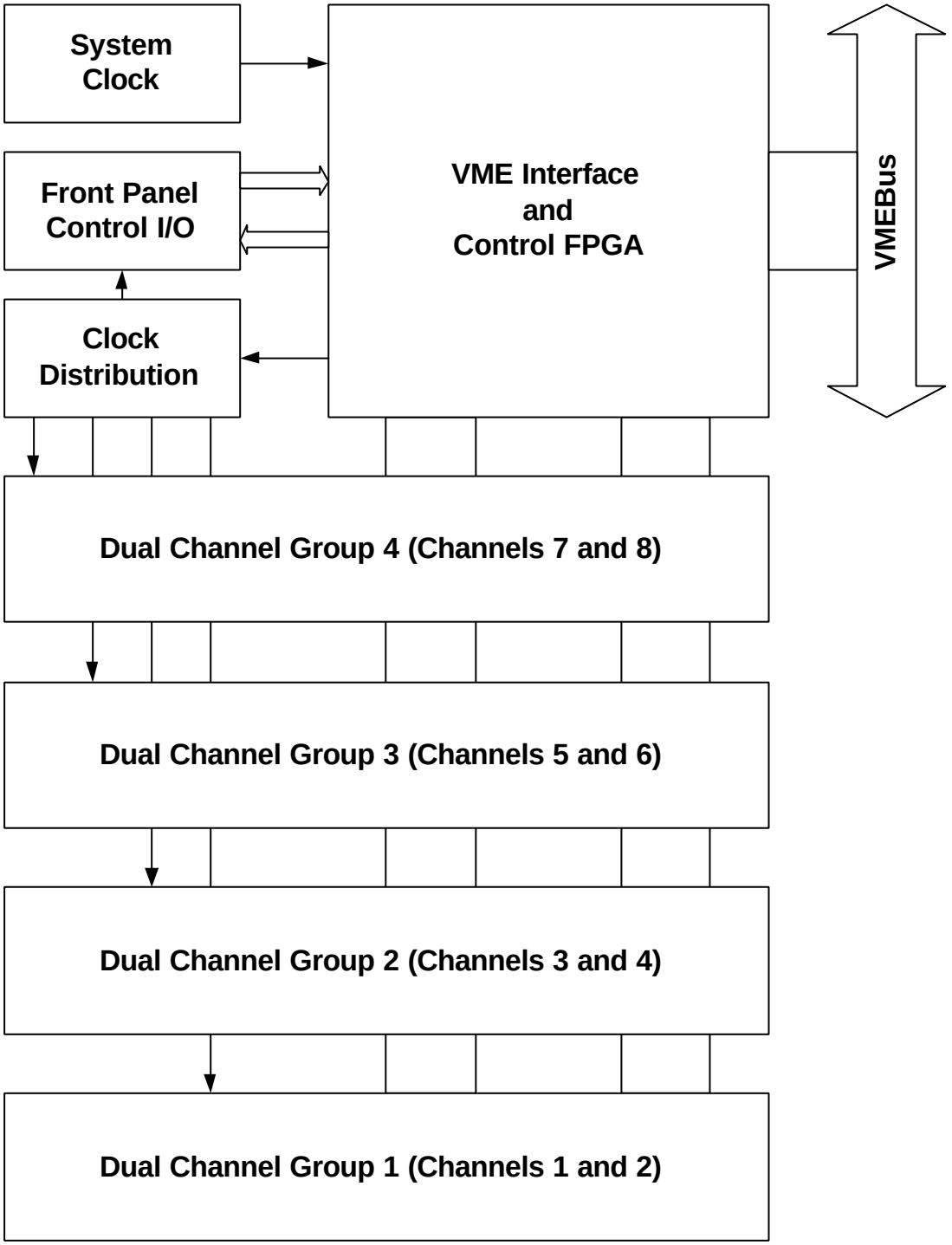
? 8 channels
? 12-bit resolution
? up to 105 MHz sampling rate per channel
? special clock modes (clock prescaling, external “arbitrary” clock
? > 80 MHz analog bandwidth*
? pedestal variance typical < 0.7 bit
? channel to channel crosstalk below noise (i.e. invisible in Fourier spectrum)
? external/internal clock
? multi event mode
? pre/post trigger option
? 128 Ksamples memory
? dual 128 Ksample memory option
? trigger generation
? 4 NIM control inputs/4 NIM control outputs
? A32 D32/BLT32/MBLT64
? Geographical addressing mode (in conjunction with VME64x backplane)
? Hot swap (in conjunction with VME64x backplane)
? VME64x Connectors
? VME64x Side Shielding
? VME64x Front panel
? VME64x extractor handles (on request)
? F1002 compatible P2 row A/C assignment
? +5 V, +12V and –12 V VME standard voltages

* The analog bandwidth of the ADC chip is 500 MHz, the bandwidth of the used input stage amplifier is 300 MHz, the connected circuitry should not reduce this, but for the time being we have no means to measure this parameter beyond 80 MHz.

Note: The SIS3300 shall not be operated on P2 row A/C extensions, like VSB e.g. due to the compatibility to the F1001 FADC modules clock and start/stop distribution scheme.

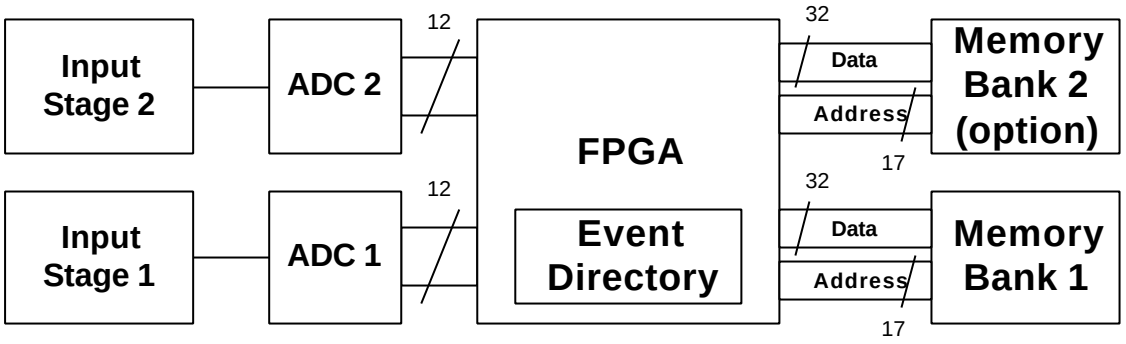
3.2 Module design

The SIS3300 consists of four identical groups of 2 ADC channels and a control section as shown in the simplified block diagram below.



3.2.1 Dual channel group

Two ADC channels form a group, which memory is handled by one Field Programmable Gate Array (FPGA).



3.3 Modes of Operation

The SIS3300 was developed with maximum flexibility in mind. The FPGA based design of the card allows to meet the requirements of many readout applications with dedicated firmware designs in the future. The initial firmware is supposed to furnish you with an easy to use yet powerful high speed high resolution Flash Analog to Digital Converter (FADC) implementation, that covers many everyday analog to digital applications.

3.4 Memory managment

The individual memory bank(s) can be used either as one contiguous memory or as a subdivided multi event memory. In addition memory depth can be limited in single event operation to match the requirements of the given application. The memory configuration is defined through the memory configuration register, while bank handling (on dual memory bank modules) is under control of the acquisition control register.

3.4.1 Single Event Mode

The full memory of 128 K Samples of the SIS3300 is used as one big circular buffer or as single shot memory in single event mode, unless memory size is limited by the event configuration register.

3.4.2 Multi Event Mode

The memory can be divided in up to 1024 pages or events to make the acquisition of shorter signals more efficient. The stop pointers for the individual page can be retrieved from the event directory. In auto start mode the ADC advances to the next page and starts sampling automatically.

3.4.3 Dual Bank Mode

Dual bank mode is available on cards that are stuffed with two 128K memory chips per channel. The single/multi event selection will influence both memory banks in the same fashion. Data from the inactive bank can be readout, while the other bank is acquiring new data. It may depend on the actual setup, whether the analog performance of the module is affected by parallel readout and acquisition.

3.4.4 Pre/Post Trigger Mode

Pre and Post trigger are available both in single and multi event mode.

3.5 Trigger control

The SIS3300 features pre/post trigger capability as well as start/stop mode acquisition and a gate mode (in which start and stop are derived from the leading and trailing edge of a single control input signal).
The trigger behaviour is defined by the acquisition control register.

3.6 Trigger generation

The trigger output of the SIS3300 can be either used to interact with external trigger logic or to base start/stop on a threshold (i.e. one individual threshold per ADC channel) of the digitized data. Trigger generation can be activated with two conditions:

? module armed (i.e. sample clock active, trigger can be used to start acquisition)
? module armed and started (trigger can be used to stop acquisition)

The user can select between triggering on the conditions above and below threshold

4 VME Addressing

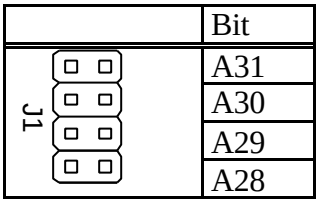
As the SIS3300 VME FADC features memory options with up to 2 banks of 4 times 128 K samples each, A32 addressing was implemented as the only option. Hence the module occupies an address space of 0xFFFFFF Bytes (i.e. 16 MBytes) are used by the module.

4.1 Base Address Selection

VME addressing capabilities are somewhat limited on the SIS3300 V1 printed circuit board (PCB) design due to missing lines. The revision of the SIS3300 board is printed in white on the lower edge of the component side of the PCB.

4.1.1 PCB revision SIS3300_V1

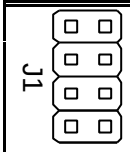
Address bits A28 to A31 of the A32 base address are defined by the four jumpers of jumper array J1 on V1 cards. An open position corresponds to a 1, a closed jumper reflects a 0. The position closest to the front panel defines the setting of Bit 31.



	Bit
	A31
	A30
	A29
	A28

4.1.2 PCB revision SIS3300_V2 and higher

The SIS3300 firmware addressing concept is a pragmatic approach to combine standard rotary switch style settings with the use of VME64x backplane geographical addressing functionality.
The base address is defined by the selected addressing mode, which is defined by jumper array J1 and possibly SW1 and SW2 (in non geographical mode).

	Function
	EN_A32
	EN_GEO
	EN_VIPA
	reserved

The table below summarises the possible base address settings.

J1 Setting			Bits							
A32	GEO	VIPA	31	30	29	28	27	26	25	24
x			SW1				SW2			
x	x		0	0	0	GA4	GA3	GA2	GA1	GA0
		x	Not implemented in this design							

Shorthand	Explanation
SW1/SW2	Setting of rotary switch SW1 or SW2 respective
GA0-GA4	Geographical address bit as defined by the VME64x(P) backplane

Note 1: This concept allows the use of the SIS3300 in standard VME as well as in VME64x environments, i.e. the user does not need to use a VME64x backplane.

Note 2: The factory default setting is EN_A32 closed, SW1=3, SW2=0 (i.e. the module will react to A32 addressing under address 0x30000000)

4.2 Address Map

The SIS3300 resources and their locations are listed in the table below.

- new Clock Predivider register
- new No_Of_Sample register

Note: Write access to a key address (KA) with arbitrary data invokes the respective action

Offset	Size in Bytes	BLT	Access	Function
0x00000000	4	-	W	Control Register (J-K register)
0x00000000	4	-	R	Status Register
0x00000004	4	-	R	Module Id. and Firmware Revision register
0x00000008	4	-	R/W	Interrupt configuration register
0x0000000C	4	-	R/W	Interrupt control register
0x00000010	4	-	R/W	Acquisition control/status register (J-K register)
0x00000014	4	-	R/W	Extern Start Delay register
0x00000018	4	-	R/W	Extern Stop Delay register
0x0000001C	4	-	R/W	Time stamp predivider register
0x00000020	4	-	KA W	General Reset
0x00000028	4		W	Trigger setup register
0x00000030	4	-	KA W	VME Start sampling
0x00000034	4	-	KA W	VME Stop sampling
0x00000040	4	-	KA W	Start auto bank switch
0x00000044	4	-	KA W	Stop auto bank switch
0x00000048	4	-	KA W	Clear bank 1 memory full
0x0000004C	4	-	KA W	Clear bank 2 memory full
0x00001000	0x1000	D32	R	Event Time Stamp directory bank 1
0x00002000	0x1000	D32	R	Event Time Stamp directory bank 2
0x00100000	4	-	W only	Event configuration register (all ADCs)
0x00100020	4	-	W only	Clock Predivider register (all ADCs)
0x00100024	4		W only	No_Of_Sample register (all ADCs)
0x00101000	0x1000		R	Special event directory bank 1
0x00102000	0x1000	-	R	Special event directory bank 2
Event information ADC group 1				
0x00200000	4	-	R/W	Event configuration register (ADC1, ADC2)
0x00200004	4		R/W	Threshold register (ADC1, ADC2)
0x00200008	4	-	R	Bank1 address counter (ADC1, ADC2)
0x0020000C	4	-	R	Bank2 address counter (ADC1, ADC2)
0x00200010	4	-	R	Bank1 Event counter (ADC1, ADC2)
0x00200014	4	-	R	Bank2 Event counter (ADC1, ADC2)
0x00200020	4	-	R/W	Clock Predivider register (ADC1, ADC2)
0x00200024	4	-	R/W	No_Of_Sample register (ADC1, ADC2)
0x00201000	0x1000	D32	R	Event directory bank 1 (ADC1, ADC2)
0x00202000	0x1000	D32	R	Event directory bank 2 (ADC1, ADC2)
Event information ADC group 2				
0x00280000	4	-	R/W	Event configuration register (ADC3, ADC4)
0x00280004	4		R/W	Threshold register (ADC3, ADC4)
0x00280008	4	-	R	Bank1 address counter (ADC3, ADC4)
0x0028000C	4	-	R	Bank2 address counter (ADC3, ADC4)
0x00280010	4	-	R	Bank1 Event counter (ADC3, ADC4)
0x00280014	4	-	R	Bank2 Event counter (ADC3, ADC4)
0x00280020	4	-	R/W	Clock Predivider register (ADC3, ADC4)
0x00280024	4	-	R/W	No_Of_Sample register (ADC3, ADC4)
0x00281000	0x1000	D32	R	Event directory bank 1 (ADC3, ADC4)
0x00282000	0x1000	D32	R	Event directory bank 2 (ADC3, ADC4)
Event information ADC group 3				

0x00300000	4	-	R/W	Event configuration register (ADC5, ADC6)
0x00300004	4		R/W	Threshold register (ADC5, ADC6)
0x00300008	4	-	R	Bank1 address counter (ADC5, ADC6)
0x0030000C	4	-	R	Bank2 address counter (ADC5, ADC6)
0x00300010	4	-	R	Bank1 Event counter (ADC5, ADC6)
0x00300014	4	-	R	Bank2 Event counter (ADC5, ADC6)
0x00300020	4	-	R/W	Clock Predivider register (ADC5, ADC6)
0x00300024	4	-	R/W	No_Of_Sample register (ADC5, ADC6)
0x00301000	0x1000	D32	R	Event directory bank 1 (ADC5, ADC6)
0x00302000	0x1000	D32	R	Event directory bank 2 (ADC5, ADC6)
Event information ADC group 4				
0x00380000	4	-	R/W	Event configuration Register (ADC7, ADC8)
0x00380004	4		R/W	Threshold register (ADC7, ADC8)
0x00380008	4	-	R	Bank1 address counter (ADC7, ADC8)
0x0038000C	4	-	R	Bank2 address counter (ADC7, ADC8)
0x00380010	4	-	R	Bank1 Event counter (ADC7, ADC8)
0x00380014	4	-	R	Bank2 Event counter (ADC7, ADC8)
0x00380020	4	-	R/W	Clock Predivider register (ADC7, ADC8)
0x00380024	4	-	R/W	No_Of_Sample register (ADC7, ADC8)
0x00381000	0x1000	D32	R	Event directory bank 1 (ADC7, ADC8)
0x00382000	0x1000	D32	R	Event directory bank 2 (ADC7, ADC8)
Bank 1 memory				
0x00400000	0x80000	D32/64	R/W*	Bank 1 memory (ADC1, ADC2)
0x00480000	0x80000	D32/64	R/W*	Bank 1 memory (ADC3, ADC4)
0x00500000	0x80000	D32/64	R/W*	Bank 1 memory (ADC5, ADC6)
0x00580000	0x80000	D32/64	R/W*	Bank 1 memory (ADC7, ADC8)
Bank 2 memory				
0x00600000	0x80000	D32/64	R/W*	Bank 2 memory (ADC1, ADC2)
0x00680000	0x80000	D32/64	R/W*	Bank 2 memory (ADC3, ADC4)
0x00700000	0x80000	D32/64	R/W*	Bank 2 memory (ADC5, ADC6)
0x00780000	0x80000	D32/64	R/W*	Bank 2 memory (ADC7, ADC8)

*W in D32 only (for memory test e.g.)

Note 1: The event information is identical for the four ADC groups (unless the module has a hardware problem), hence it will be sufficient for normal operation to retrieve the needed information from one group only.

Note 2: MBLT64 read access is supported from the (two) memory bank(s) only.

5 Register Description

5.1 Status register(0x0, read)

Bit	Function
31	
30	
29	
28	
27	
26	
25	
24	
23	
22	
21	
20	
19	P2_SAMPLE_IN
18	P2_RESET_IN
17	P2_TEST_IN
16	Status User Input
15	Status Control 15
14	Status Control 14
13	Status Control 13
12	Status Control 12
11	Status Control 11
10	Bank full pulse on LEMO output 3
9	Bank full pulse on LEMO output 2
8	Bank full pulse on LEMO output 1 (highest priority)
7	Status Control 7
6	Status Control 6
5	Status trigger generation (1=armed and started, 0=armed)
4	Status trigger output inversion(1=inverted, 0=straight)
3	Status Control 3
2	multiplexer mode = 0: Status of user/trigger output (1=trigger output, 0=user output) multiplexer mode = 1: output set by multiplexer out pulse
1	Status User Output (1=output on, 0=output off)
0	Status User LED (1=LED on, 0=LED off)

The power up or key reset content is 0x0 (see default settings of control register).

5.2 Control Register(0x, write)

The control register is in charge of the control of most of the basic properties of the SIS3300 board in write access. It is implemented via a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which location is 16-bit higher in the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time.
On read access the same register represents the status register.

Bit	Function
31	Clear reserved 15
30	Clear reserved 14
29	Clear reserved 13
28	Clear reserved 12
27	Clear reserved 11
26	clear bank full pulse to output 3
25	clear bank full pulse to output 2
24	clear bank full pulse to output 1
23	Clear reserved 7
22	Clear reserved 6
21	Activate trigger upon armed
20	Non inverted trigger output
19	Clear reserved 3
18	Enable user output/disable trigger output (*)
17	Clear user output (*)
16	Switch off user LED (*)
15	Set reserved 15
14	Set reserved 14
13	Set reserved 13
12	Set reserved 12
11	Set reserved 11
10	set bank full pulse to output 3
9	set bank full pulse to output 2
8	set bank full pulse to output 1
7	Set reserved 7
6	Set reserved 6
5	Activate trigger upon armed and started
4	Invert trigger output
3	Set reserved 3
2	Enable trigger output/disable user output
1	Set user output (if bit 2 is not set)
0	Switch on user LED

(*) denotes power up default setting

5.3 Module Id. and Firmware Revision Register (0x4, read)

This register reflects the module identification of the SIS3300 and its minor and major firmware revision levels. The major revision level will be used to distinguish between substantial design differences and experiment specific designs, while the minor revision level will be used to mark user specific adaptations.

Bit	Function	Reading
31	Module Id. Bit 15	3
30	Module Id. Bit 14	
29	Module Id. Bit 13	
28	Module Id. Bit 12	
27	Module Id. Bit 11	3
26	Module Id. Bit 10	
25	Module Id. Bit 9	
24	Module Id. Bit 8	
23	Module Id. Bit 7	0
22	Module Id. Bit 6	
21	Module Id. Bit 5	
20	Module Id. Bit 4	
19	Module Id. Bit 3	0
18	Module Id. Bit 2	
17	Module Id. Bit 1	
16	Module Id. Bit 0	
15	Major Revision Bit 7	
14	Major Revision Bit 6	
13	Major Revision Bit 5	
12	Major Revision Bit 4	
11	Major Revision Bit 3	
10	Major Revision Bit 2	
9	Major Revision Bit 1	
8	Major Revision Bit 0	
7	Minor Revision Bit 7	
6	Minor Revision Bit 6	
5	Minor Revision Bit 5	
4	Minor Revision Bit 4	
3	Minor Revision Bit 3	
2	Minor Revision Bit 2	
1	Minor Revision Bit 1	
0	Minor Revision Bit 0	

5.3.1 Major revision numbers

Find below a table with major revision numbers used to date

Major revision number	Application/user
0x01 to 0x0F	Generic designs
0x10	Amanda

5.4 Interrupt configuration register (0x8)

This read/write register controls the VME interrupt behaviour of the SIS3300 ADC. Four interrupt sources are foreseen, for the time being three of them are associated with an interrupt condition, the fourth condition is reserved for future use.
The interrupter type is DO8 .

5.4.1 IRQ mode

In RORA (release on register access) mode the interrupt will be pending until the IRQ source is cleared by specific access to the corresponding disable VME IRQ source bit. After the interrupt is serviced the source has to be activated with the enable VME IRQ source bit again.
In ROAK (release on acknowledge) mode , the interrupt condition will be cleared (and the IRQ source disabled) as soon as the interrupt is acknowledged by the CPU. After the interrupt is serviced the source has to be activated with the enable VME IRQ source bit again. ROAK IRQ mode can be used in conjunction with the University of Bonn LINUX Tundra Universe II driver by Dr. Jürgen Hannappel on Intel based VME SBCs.

Bit	Function	Default
31		0
30		0
29		0
28		0
27		0
26		0
25		0
24		0
23		0
22		0
21		0
20		0
19		0
18		0
17		0
16		0
15		0
14		0
13		0
12	RORA/ROAK Mode (0: RORA; 1: ROAK)	0
11	VME IRQ Enable (0=IRQ disabled, 1=IRQ enabled)	0
10	VME IRQ Level Bit 2	0
9	VME IRQ Level Bit 1	0
8	VME IRQ Level Bit 0	0
7	IRQ Vector Bit 7; placed on D7 during VME IRQ ACK cycle	0
6	IRQ Vector Bit 6; placed on D6 during VME IRQ ACK cycle	0
5	IRQ Vector Bit 5; placed on D5 during VME IRQ ACK cycle	0
4	IRQ Vector Bit 4; placed on D4 during VME IRQ ACK cycle	0
3	IRQ Vector Bit 3; placed on D3 during VME IRQ ACK cycle	0
2	IRQ Vector Bit 2; placed on D2 during VME IRQ ACK cycle	0
1	IRQ Vector Bit 1; placed on D1 during VME IRQ ACK cycle	0
0	IRQ Vector Bit 0; placed on D0 during VME IRQ ACK cycle	0

The power up default value reads 0x 00000000

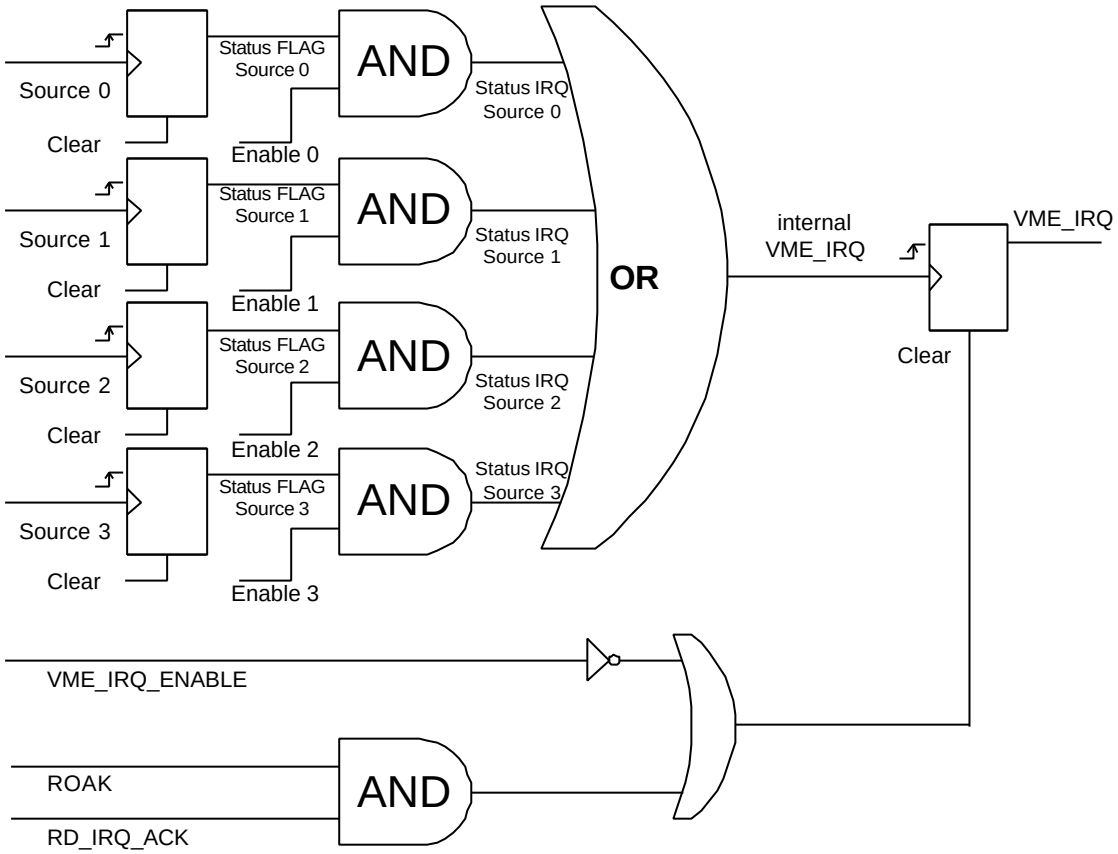
5.5 Interrupt control register (0xC)

This register controls the VME interrupt behaviour of the SIS3300 ADC. Four interrupt sources are foreseen, for the time being three of them are associated with an interrupt condition, the fourth condition is reserved for future use.

Bit	Function (w)	(r)	Default
31	unused	Status IRQ source 3 (user input)	0
30	unused	Status IRQ source 2 (reserved)	0
29	unused	Status IRQ source 1 (end of last event, bank full)	0
28	unused	Status IRQ source 0 (end of event)	0
27	unused	Status VME IRQ	0
26	unused	Status internal IRQ	0
25	unused	0	0
24	unused	0	0
23	Clear IRQ source 3	Status flag source 3	0
22	Clear IRQ source 2	Status flag source 2	0
21	Clear IRQ source 1	Status flag source 1	0
20	Clear IRQ source 0	Status flag source 0	0
19	Disable IRQ source 3	0	0
18	Disable IRQ source 2	0	0
17	Disable IRQ source 1	0	0
16	Disable IRQ source 0	0	0
15	unused	0	0
14	unused	0	0
13	unused	0	0
12	unused	0	0
11	unused	0	0
...	...	...	0
4	unused	0	0
3	Enable IRQ source 3	Status enable source 3 (read as 1 if enabled, 0 if disabled)	0
2	Enable IRQ source 2	Status enable source 2 (read as 1 if enabled, 0 if disabled)	0
1	Enable IRQ source 1	Status enable source 1 (read as 1 if enabled, 0 if disabled)	0
0	Enable IRQ source 0	Status enable source 0 (read as 1 if enabled, 0 if disabled)	0

The power up default value reads 0x 00000000

The generation of the status flags, the IRQ flags and the actual IRQ is illustrated with the schematic below:



5.6 *Acquisition control register (0x10, read/write)*

The acquisition control register is in charge of most of the settings related to the actual configuration of the digitization process.
Like the control register it is implemented in a J/K fashion.

Bit	Write Function	Read
31	Clear MULTIPLEXER Mode	0
30	Clear Clock Source Bit2	0
29	Clear Clock Source Bit1	0
28	Clear Clock Source Bit0	0
27	Disable external clock random mode	0
26	Disable front panel gate mode (not start/stop)	0
25	Disable P2 Start/Stop logic	0
24	Disable front panel LEMO start/stop logic	0
23	Disable external stop delay	Bank 2 full
22	Disable external start delay	Bank 2 busy
21	Disable multi event mode 0 : Enable sample clock will be cleared with end of event 1 : Enable sample clock will be cleared at end of bank only (i.e. with last page of memory)	Bank 1 full
20	Disable Autostart (in multi event mode only)	Bank 1 busy
19	Disable reserved	0
18	Disable auto bank switch mode	Bank switch busy
17	Disable sample clock for memory bank 2 (arm for sampling)	0
16	Disable sample clock for memory bank 1 (arm for sampling)	ADC_BUSY
15	Set MULTIPLEXER Mode	Status MULTIPLEXER Mode
14	Set clock source Bit 2	Status clock source Bit 2
13	Set clock source Bit 1	Status clock source Bit 1
12	Set clock source Bit 0	Status clock source Bit 0
11	Enable external clock random mode	Status external clock random mode
10	Enable front panel gate mode (not Start/Stop)	Status front panel gate mode
9	Enable P2 Start/Stop logic	Status P2 start/stop logic
8	Enable front panel Lemo Start/Stop logic	Status front panel start/stop logic
7	Enable external stop delay (value defined by start delay register)	Status external stop delay
6	Enable external start delay (value defined by stop delay register)	Status external start delay
5	Enable multi event mode 0 : Enable Sample Clock will be cleared with end of event 1 : Enable Sample Clock will be cleared at end of bank only (i.e. with last page of memory)	Status multi event mode
4	Enable Autostart (in multi event mode only)	Status Autostart
3	Enable reserved	Status reserved
2	Enable auto bank switch mode	Status auto bank switch mode
1	Enable Sample Clock for Memory Bank 2 (arm for sampling)	Status sample clock bank 2
0	Enable Sample Clock for Memory Bank 1 (arm for sampling)	Status sample clock bank 1

The power up default value reads 0x

Clock source bit setting table:

Clock Source Bit2	Clock Source Bit1	Clock Source Bit0	Clock Source
0	0	0	internal 100 MHz
0	0	1	internal 50 MHz
0	1	0	internal 25 MHz
0	1	1	internal 12.5 MHz
1	0	0	internal 6.25 MHz
1	0	1	internal 3.125 MHz
1	1	0	external clock (front panel)
1	1	1	P2-Clock

The external clock can range from xxx to 105 MHz. Lower sampling rates into memory can be accomplished with a sampling clock within the specified range in combination with the clock predivider register in multiplexer mode or random external clock mode.

5.7 Key address general reset (0x20, write)

A write with arbitrary data to this register (key address) resets the SIS3300 to it's power up state.

5.8 Key address VME start sampling (0x30, write)

A write with arbitrary data to this register (key address) will initiate sampling on the active memory bank.

5.9 Key address VME stop sampling (0x34, write)

A write with arbitrary data to this register (key address) will halt sampling on the active memory bank.

5.10 External Start Delay register (0x14, read/write)

Pretrigger operation can be implemented via the start delay register in conjunction with front panel start/stop or gate mode operation. The external and autostart start signal (or leading edge of the gate) will be delayed by the value of the register+2 clocks if the external start delay is enabled in the acquisition control register.

Bit	
32	unused, read as 0
...	
16	unused, read as 0
15	START_DELAY_BIT15
..	
..	
0	START_DELAY_BIT0

The power up default value is 0

5.11 External Stop Delay register (0x18, read/write)

Posttrigger operation can be implemented via the stop delay register in conjunction with front panel start/stop or gate mode operation. The external stop signal (or trailing edge of the gate) will be delayed by the value of the register+2 clocks if the external stop delay is enabled in the acquisition control register.

Bit	
32	unused, read as 0
...	
16	unused, read as 0
15	STOP_DELAY_BIT15
..	
..	
0	STOP _DELAY_BIT0

The power up default value is 0

Note: The user can generate a gate of defined length (in clock ticks) by fanning a short pulse to the start and stop input with start/stop mode active, stop delay enabled and the stop delay register programmed to the desired gate width. Pipelining will have to be taken into account, i.e. the digitised signal is about 40 ns (with the module sampling at 100 MHz) ahead of the respective control signal, a fact that can be used in external trigger decisions.
For longer external trigger decisions one can consider to pipeline the ADC data in the FPGA in future firmware revisions before storing them to memory.

5.12 Time stamp predivider register (0x1C)

The (read/write) time stamp predivider register is used to define a prescale factor for the frequency of the time stamp counter. The time stamp counter counts at the clock rate with the time stamp predivider value of 0 and 1, a prescale factor of 2 ... 65535 is selected by writing the corresponding value to the register.

Bit	
31	unused, read as 0
...	
16	unused, read as 0
15	Time stamp predivider BIT15
..	
..	
0	Time stamp predivider BIT0

The power up default value is 0

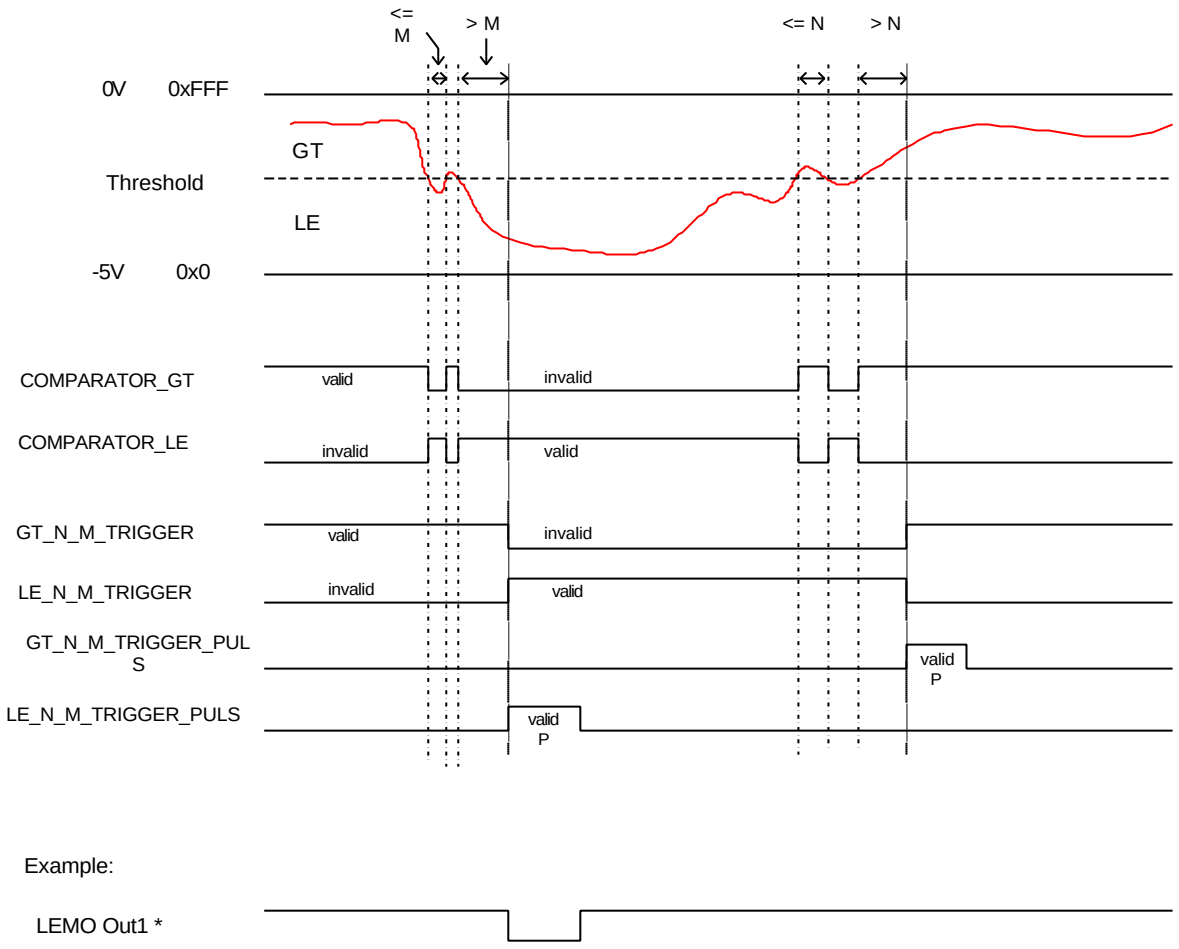
Note: A predivider value of 0 can not be used with firmware V201

5.13 Trigger setup register (0x28)

The behaviour of the trigger output of the SIS3300 can be controlled by this register. The user can select between a M over, N under threshold or a pulsed trigger output with pulse width P. At the same time the register holds the values for N, M and P as shown in the table below.

Bit	
31	unused
30	unused
29	unused
28	enable pulse mode
27	unused
26	unused
25	unused
24	enable N M mode
23	unused
...	...
20	unused
19	bit 3 of P
18	bit 2 of P
17	bit 1 of P
16	bit 0 of P
15	unused
...	...
12	unused
11	bit 3 of N
10	bit 2 of N
9	bit 1 of N
8	bit 0 of N
7	unused
...	...
4	unused
3	bit 3 of M
2	bit 2 of M
1	bit 1 of M
0	bit 0 of M

The function of the trigger setup register is illustrated with the drawing below:



5.14 Event Time Stamp directory bank 1 (0x1000-0x1ffc, read only)

The event time stamp directory can be used to measure time between triggers (stops) in multi event mode. A scaler counting the ADC clock is enabled with the first stop (hence the time stamp for the first event will read 0 always). The counter value (of the 24-bit wide) scaler is written to the corresponding location for subsequent events.

offset address	Time Stamp (D23:D0)
0x0	Time Stamp 0
..	
0xffc	Time Stamp 1023

5.15 Event Time Stamp directory bank 2 (0x2000-0x2ffc, read only)

As for bank 1.

offset address	Time Stamp (D23:D0)
0x0	Time Stamp 0
..	
0xffc	Time Stamp 1023

5.16 Event configuration register (0x100000, write only)

The number of memory divisions (events) is defined by this register in multi event mode. The lowest three bits define the number of memory divisions as listed in the table below. On dual bank units both memory banks will be affected by the configuration of the event configuration register. The maximum number of events is defined by the size of the event directory, which has 1024 entries.. The user has to enable the trigger event directory by setting bit 12 in the event configuration register and set the FPGA trigger address in the four ADC group event configuration registers afterwards. The FPGA trigger address is used to identify the four otherwise indistinguishable FPGAs when the 2 time 4 trigger bits are copied from the ADC FPGAs to the control FPGA.

Bit	function	Default
31	unused; read 0	0
...	...	...
13	unused; read 0	0
12	enable trigger event directory	0
11	unused; read 0	0
10	unused; read 0	0
9	FPGA trigger address A1 (used for ADC group N configuration register)	0
8	FPGA trigger address A0 (used for ADC group N configuration register)	0
7	unused; read 0	
..	..	
4	unused; read 0	0
3	Enable Wrap around mode (no address auto stop) 0 : Autostop at end of page 1 : Wrap around page until STOP (External or KEY)	0
2	Page size Bit 2	0
1	Page size Bit 1	0
0	Page size Bit 0	0

The power up default value reads 0x 00000000

The page/event size is defined by the 3 page size bits as follows:

Page size Bit 2	Page size Bit 1	Page size Bit 0	Page size	Number of divisions (Events/Bank)
0	0	0	128 K Samples	1
0	0	1	16K Samples	8
0	1	0	4 K Samples	32
0	1	1	2 K Samples	64
1	0	0	1 K Samples	128
1	0	1	512 Samples	256
1	1	0	256 Samples	512
1	1	1	128 Samples	1024

Note: The value of the register is copied autonomously to the 4 ADC groups. As the event configuration register is read only, the user will have to read back the value from one of the ADC groups in case read back functionality is desired.

5.17 ADC group N event configuration register (0x200000, 0x280000, 0x300000 and 0x380000)

These four registers have the same structure as the event configuration register, but they hold the information for the individual ADC FPGA and are read/write. If trigger event directory information is desired the FPGA trigger address bits and the enable bit have to be set as shown below:

ADC group	Address	Register Setup
1	0x200000	0x10yy
2	0x280000	0x11yy
3	0x300000	0x12yy
4	0x380000	0x13yy

yy: common setup for lower 8 bits containing page size and wrap/no wrap configuration

Note: As the event configuration register is copied to the four ADC group N event configuration registers on write access, the user will have to make sure, that this register remains unchanged in trigger event directory mode.

5.18 Threshold register (0x200004)

This read write register holds the threshold for ADC channels 1 and 2, via the highest bit of each channel the user can select between greater (GT) or less than/equal (LE) as trigger criterion.

Bit	31	30-28	27-16	15	14-12	11-0
Function	0:GT 1:LE	unused	threshold ADC 1	0:GT 1:LE	unused	threshold ADC 2

5.19 Bank 1 address counter (0x200008)

This read only register holds the current address counter for ADC group 1 and bank 1. The counter is 17 –bit wide. The counter will change while the ADC is sampling, after the ADC was stopped, the stop position can be retrieved (in multi event mode it will have to be read from the event directory). The address counter points to the next memory location that will be written to (see event directory also).

Bit	31-17	16-0
Function	unused, read back as 0	address counter

5.20 Bank 2 address counter (0x20000C)

Same as bank 1 address counter, but for bank 2 of ADC group 1.

5.21 Bank 1 event counter (0x200010)

This read only register holds the current event counter for ADC group 1 and bank 1. The counter is 12–bit wide. The counter will change while the ADC is sampling (as events are coming in). The returned value is the current event number.

Bit	31-12	11-0
Function	unused, read back as 0	event counter

5.22 Bank 2 event counter (0x200014)

Same as bank 1 event counter, but for bank 2 of ADC group 1.

5.23 Clock Predivider register (0x100020, write only)

The Clock Predivider factor (max. 255; 0xff) is defined by this register. It is used in MULTIPEXER mode only.

Bit	Function	Default
31	Unused; read 0	0
..	..	
8	Unused; read 0	0
7	Clock Predivider bit 7 (MSB)	0
..	..	
0	Clock Predivider bit 0 (LSB)	0

The power up default value reads 0x 00000000

5.24 No_Of_Sample register (0x100024, write only)

The No_of_Sample factor (max. 255; 0xff) is defined by this register. It is used in MULTIPEXER mode only.

Bit	Function	Default
31	Unused; read 0	0
..	..	
8	Unused; read 0	0
7	No_Of_Sample bit 7 (MSB)	0
..	..	
0	No_Of_Sample bit 0 (LSB)	0

The power up default value reads 0x 00000000

Note: The value of these registers (Clock Predivider, No_of_Sample) is copied autonomously to the 4 ADC groups. As the register is write only, the user will have to read back the value from one of the ADC groups in case read back functionality is desired.

5.25 Trigger event directory bank 1 (0x101000 – 0x101ffc)

Trigger information from the 4 ADC groups is copied to this register if
1.) the function is enabled in the event configuration register
2.) the address bits are set in the four ADC group event configuration registers

offset address	(D31)	(D30)	(D29)	(D28)	(D27)	(D26)	(D25)	(D24)	(D21:20)	(D19)	(D18:D17)	Event Data End Address (D16:D0)
0x0	T1	T2	T3	T4	T5	T6	T7	T8	0	W	0	(End Address + 1) of Event 0
..	...	...	...	...	...	...	...	...	...	...		...
0xffc	T1	T2	T3	T4	T5	T6	T7	T8	0	W	0	(End Address + 1) of Event 1023

W: wrap around bit
T1-T8 trigger information ADC 1-ADC8, 1: ADC channel has met trigger criterion for this event, 0: ADC channel has not triggered for this event

5.26 Trigger event directory bank 2 (0x102000 – 0x102ffc)

Same as above, but for bank 2.

5.27 Event directory bank 1 (0x201000 – 0x201ffc)

The event directory holds the stop pointer(s) (i.e. end address+1) of memory bank 1.
The directory is 32 bits wide, a wrap around bit (i.e. bit 19) will be set if the page was filled at least once (i.e. if the memory pointer has reached the end)

offset address	(D31:24)	(D23:22)	(D21:20)	(D19)	(D18:D17)	Event Data End Address (D16:D0)
0x0	0	T2, T1	0	W	0	(End Address + 1) of Event 0
..	...	...	...	...		...
0xffc	0	T2, T1	0	W	0	(End Address + 1) of Event 1023

W: wrap around bit
T1, T2 trigger information ADC 1, ADC 2 of ADC group

5.28 Event directory bank 2 (0x202000 – 0x202ffc)

The event directory holds the stop pointer(s) (i.e. end address+1) of memory bank 2.
The directory is 32 bits wide, a wrap around bit (i.e. bit 19) will be set if the page was filled at least once (i.e. if the memory pointer has reached the end)

offset address	(D31:24)	(D23:22)	(D21:20)	(D19)	(D18:D17)	Event Data End Address (D16:D0)
0x0	0	T2, T1	0	W	0	(End Address + 1) of Event 0
..	...	...	...	...		...
0xffc	0	T2, T1	0	W	0	(End Address + 1) of Event 1023

W: wrap around bit
T1, T2 trigger information ADC 1, ADC 2 of ADC group

5.29 Bank 1 memory (0x400000 – 0x5ffffc)

Bank1 memory is 128 KSamples (i.e. 512 KByte deep). The 32-bit wide memory locations hold the data of 2 ADCs each. Readout can be done with D32 or BLT32 (MBLT64 and 2eMBLT64 as future options), for memory tests D32 write cycles are supported also.

5.29.1 ADC group 1 memory (0x400000-0x47fffc, ADC channels 1 and 2)

offset address	ADC 1			ADC 2		
	D31:29	D28	D27:16	D15:13	D12	D11:0
0x0	U 0 0	OR bit	12-bit data	0 0 0	OR bit	12-bit data
..						
0x7fffc	U 0 0	OR bit	12-bit data	0 0 0	OR bit	12-bit data

U: status of user bit if enabled, 0 otherwise
OR : Out of range, set with over or underflow

5.29.2 ADC group 2 memory (0x480000-0x4ffffc ADC channels 3 and 4)

offset address	ADC 3			ADC 4		
	D31:29	D28	D27:16	D15:13	D12	D11:0
0x0	U 0 0	OR bit	12-bit data	0 0 0	OR bit	12-bit data
..						
0x7fffc	U 0 0	OR bit	12-bit data	0 0 0	OR bit	12-bit data

U: status of (input) user bit
OR : Out of range, set with over or underflow

5.29.3 ADC group 3 memory (0x500000-0x57fffc, ADC channels 5 and 6)

offset address	ADC 5			ADC 6		
	D31:29	D28	D27:16	D15:13	D12	D11:0
0x0	U 0 0	OR bit	12-bit data	0 0 0	OR bit	12-bit data
..						
0x7fffc	U 0 0	OR bit	12-bit data	0 0 0	OR bit	12-bit data

U: status of user bit if enabled, 0 otherwise
OR : Out of range, set with over or underflow

5.29.4 ADC group 3 memory (0x580000-0x5ffffc ADC channels 7 and 8)

offset address	ADC 7			ADC 8		
	D31:29	D28	D27:16	D15:13	D12	D11:0
0x0	U 0 0	OR bit	12-bit data	0 0 0	OR bit	12-bit data
..						
0x7fffc	U 0 0	OR bit	12-bit data	0 0 0	OR bit	12-bit data

U: status of user bit if enabled, 0 otherwise
OR : Out of range, set with over or underflow

5.30 Bank 2 memory (0x600000 – 0x7ffffc)

Bank 2 memory is an option to allow for parallel readout from one memory bank, while the other memory bank is acquiring data. The second memory bank has the same structure as bank 1.

6 Operation

6.1 Configuration:

? Issue key reset

? define in Interrupt configuration register
- VME Irq Level and Vector
- type of Irq requester

? define in Interrupt control register
- enable Irq source

? define in Acquistion register
- Set Clock source
- Set Start/Stop or Gate mode
- Enable/Disable P2 External Start/Stop
- Enable/Disable LEMO External Start/Stop
- Enable/Disable External Stop Delay
- Enable/Disable External Start Delay
- Set Single or Multi Event Mode
- if Multi Event then enable/disable Autostart

? define in Event configuration register
- Enable/Disable Autostop at end address of Page
- Set Page size

6.2 Arm for sampling:

? define in Acquistion register
- Enable Sample Clock for Memory Bank1 or Bank2

6.3 Start Sampling:

? in Single Event mode
- Issue key Start or External Start

? in Multi Event mode with Autostart disabled
- Issue key Start or External Start for **each** Event

? in Multi Event mode with Autostart enabled
- Issue key Start or External Start for the **first** Event only

6.4 Stop Sampling (Event):

? in Single Event mode with Autostop is enabled
- sampling stops automatically at the end address of the page

? in Single Event mode with Autostop is disabled (Wrap around mode)
- Issue key Stop or External Stop

? in Multi Event mode with Autostop is enabled
- sampling stops automatically at the end address of each page

? in Multi Event mode with Autostop is disabled (Wrap around mode)
- Issue key Stop or External Stop for each Event

6.5 End of Sampling (clear arm / disable Sample Clock):

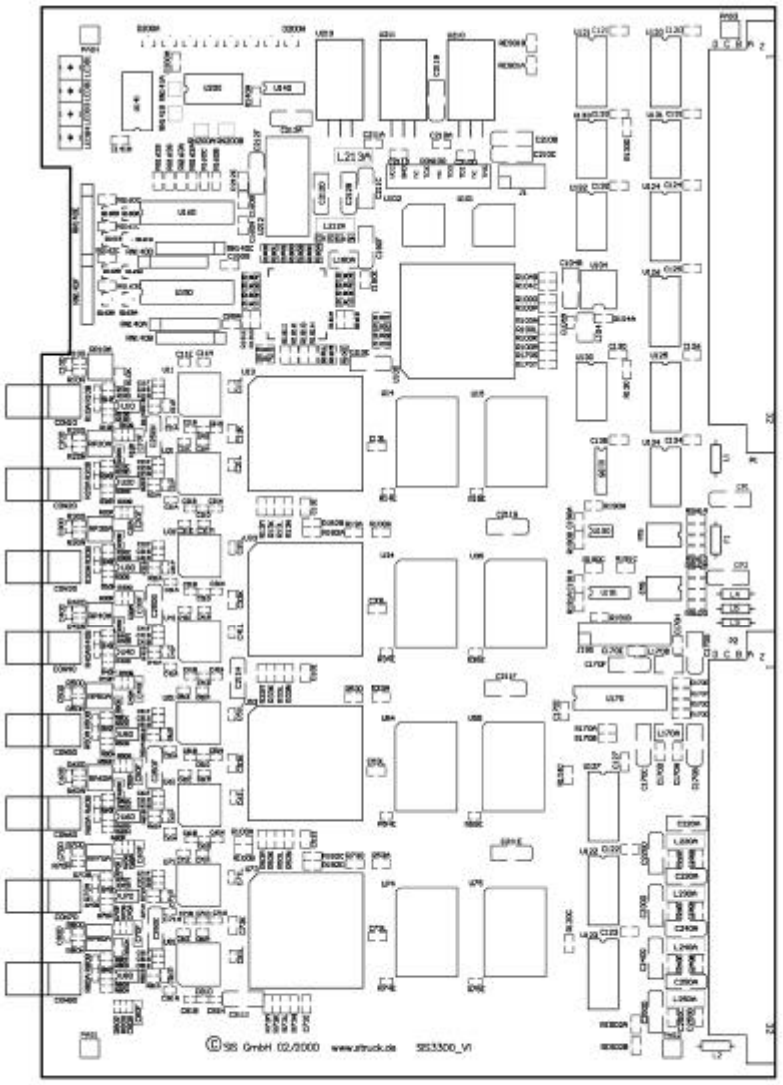
? in single event mode
the “Sample Clock Enable “ bit of the sampling bank is cleared by the logic at the end of sampling (one event)

? in multi event mode
the “Sample Clock Enable “ bit of the sampling bank is cleared by the logic at the end of sampling (last event)

The user software can poll on the status of the sample clock enable bit in the acquisition control register or use the end of event or bank full interrupt conditions.

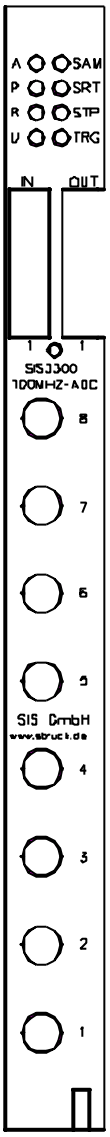
7 Board layout

A printout of the silk screen of the component side of the PCB is shown below.



8 Front panel

The SIS3300 is a single width (4TE) 6U VME module. A sketch of the front panel (without handles) is show below.



8.1 Control In/Outputs

The control I/O section features 8 LEMO00 connectors with NIM levels.

Designation	Inputs	Outputs	Designation
4	Clock In	Clock Out	4
3	Start	Ready for Start/bank full output	3
2	Stop	Ready for Stop/bank full output	2
1	User in	User out/trigger/Multiplexer Strobe/bank full output	1

The ready for start and ready for stop outputs can be used to interfere with external deadtime logic. Ready for start will become active as soon as the sample clock for one of the banks is active. Ready for stop will go active as soon as the start signal was seen by the module.

The external clock must be a symmetric signal unless the module is operated in external random clock mode
The width of an external start/stop pulse must be greater or equal two sampling clock periods.

8.1.1 Control input termination

The control inputs are configured for 50 ? termination (i.e. with 47 ?) by default.
Each input is terminated with a resistor network (5 pins, 4 resistors, common pin to socket pin 6) to ground, the names of the input sockets are listed in the table below.

Designation	Inputs	Resistor Network
4	Clock In	RN140A
3	Start	RN140B
2	Stop	RN140C
1	User in	RN140D

8.2 Analog inputs

8.2.1 Single ended LEMO version

The analog inputs of the single ended version are terminated with 50 ? . The input range of the initial series is 5V, it is shifted with the offset adjustment potentiometer to match the required user input voltage range of 0 ... –5V or +2.5 V ... –2.5V.

8.2.2 Differential version

The differential input version will be based on another printed circuit design, input termination and availbale input ranges are yet to be defined.

8.3 LED's

The SIS3300 has 8 front panel LEDs to visualise part of the modules status. The user (and access) LED are a good way to check first time communication/addressing with the module.

Color	Designator	Function
Red	A	Access to SIS3300 VME slave port
Yellow	P	Power
Green	R	Ready, on board logic configured
Green	U	User, to be set/cleared under program control
Red	SAM	Sampling,
Yellow	SRT	Start, lit with start input (or leading edge in gate mode)
Green	STP	Stop, lit with stop input (or trailing edge in gate mode)
Green	TRG	Trigger, lit if one or more channels are above threshold

The on duration of the access, sampling, start, stop and trigger LEDs is stretched to guarantee visibility even under low rate conditions.

8.4 PCB LEDs

The 8 surface mounted red LEDs D200A to D200H on the top left corner of the component side of the SIS3300 are routed to the control FPGA, their use may depend on the firmware design.

9 Jumpers/Configuration

9.1 J1

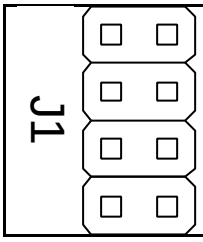
The function of J1 depends on the PCB (printed circuit board) revision level. The board revision level is printed in white on the lower edge of the card on the component side as a text of the form SIS3300_V1 e.g.

9.1.1 SIS3300_V1

Selection of bits 31-28 of the 32-bit A32 address (see. base address section)

9.1.2 SIS3300_V2 (and higher)

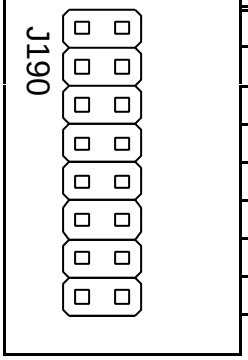
The SIS3300 supports several addressing modes, the actual mode is selected by jumper array J1. The given mode is selected if its corresponding jumper is in place. The four jumper positions are described in the table below. The A32 jumper is closest to the modules front panel.



Jumper	Function	Factory default
A32	enable A32 addressing	closed
GEO	enable geographical addressing	open
VIPA	not implemented yet	open
reserved	reserved	open

9.2 J190 Reset

Jumper 5 of jumper array J190 defines the reset behaviour of the SIS3300 upon VME Sysreset. If the jumper is closed the module will be reset with VME Sysreset. The other fields of the array are unused in the current firmware design.



Jumper	Function	Factory default
1	unused	open
2	enable watchdog	closed
3	unused	open
4	unused	open
5	unused	open
6	Connect module reset to VME_Sysreset	closed
7	unused	open
8	unused	open

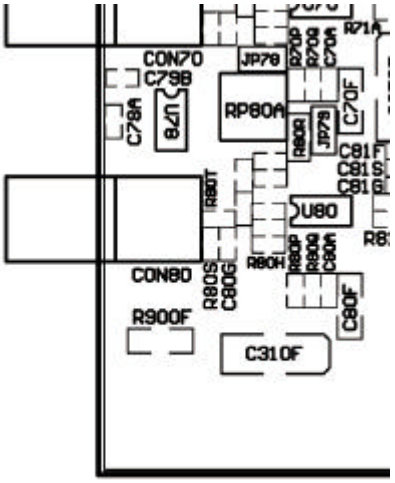
The enable watchdog jumper has to be removed during the initial JTAG firmware load.

9.3 Offset adjustment

The pedestal or offset of the ADC channels can be adjusted with the potentiometers RP10A through RP80A (see table below). The sensitivity for the positive or negative offset can be reduced by two limit jumpers (2 mm), the full range is available with both jumpers open. Do not install both jumpers for a channel in parallel.

channel	limit pos. offset	limit neg. offset	Offset-Potentiometer
1	JP78	JP79	RP80A
2	JP76	JP77	RP70A
3	JP58	JP59	RP60A
4	JP56	JP57	RP50A
5	JP38	JP39	RP40A
6	JP36	JP37	RP30A
7	JP18	JP19	RP20A
8	JP16	JP17	RP10A

The position of the two jumpers JP78 and JP79 close to potentiometer RP80A for ADC channel 1 is illustrated in the portion of the board shown below. The displayed area is the vicinity of the channel 1 LEMO input connector (CON80).



9.4 JTAG

The SIS3300 on board logic can load its firmware either from two serial PROMs or via the JTAG port on connector CON100. A list of firmware designs can be found under http://www.struck.de/sis3300firm.htm.
Hardware like the XILINX HW-JTAG-PC in connection with the appropriate software will be required for in field JTAG firmware upgrades.
The JTAG connector is a 9 pin single row 1/10 inch header, the pin assignment on the connector can be found in the table below.

Pin	Short hand	Description
1	VCC	Supply voltage
2	GND	Ground
3	nc	not connected, cut to avoid polarity mismatch
4	TCK	test clock
5	nc	not connected
6	TDO	test data out
7	TDI	test data in
8	nc	not connected
9	TMS	test modus

10 Appendix

10.1 Data acquisition modes

10.1.1 Multiplexer mode

Multiplexer mode was implemented to facilitate data acquisition with external multiplexing hardware. One of the outputs of the SIS3300 can be used to control the external multiplexing circuitry.
Multiplexer mode is activated by setting Bit 15 of the acquisition control register. Upon a start (external or via VME key address) the analog input will be latched to memory after (N –10) * clock cycles. At the same time a pulse of width one clock cycle will be generated on ouput 1. Acquisition will terminate after M samples.

* The ADC has an internal pipeline of 12 Clock cycles.
Note: The minimum value for the Predivider register value is 4

Example : Assume one multiplexing cycle consists of 20 words. The analog signal will become valid after 11 ? s and will be written to memory after 12 ? s.

Set internal Sampling clock to 12.5 MHz ✍ Clock cycle = 80 ns
Preset Predivider register to 0x96 (150) ✍ 150 x 80 ns = 12 ? s
Preset No_Of_Sample register to 0x14 (20)
Write 0x8000 (set Bit 15) to acquisition control register.

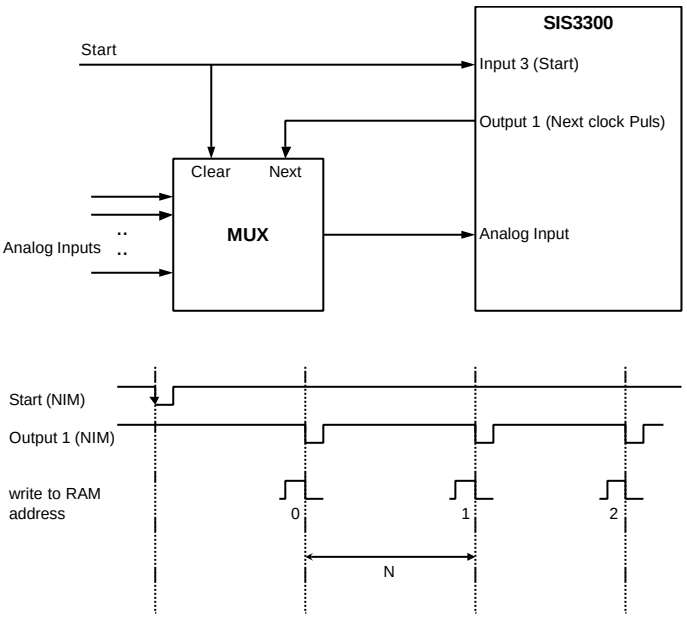


Illustration of multiplexer mode

10.1.2 Random external clock mode

Random external clock mode allows to operate the SIS3300 with basically arbitrary external clock pulse trains. The module is clocked with the internal clock (typically at 100 MHz) and a data word will be stored to memory upon the next leading edge of the internal clock when a leading edge on the external clock input is detected. Internal pipelining has to be taken into account, at 100 MHz the datum will precede the clock by about 100 ns (i.e. 10 clock ticks).
Random external clock mode is activated by writing 0x800 to the acquisition control register .

10.1.3 Auto bank switch mode

Auto bank switch mode was introduced for efficient use of the two memory banks on acquisition . The mode is activated by issuing a KEY_START_AUTO_BANK_SWITCH after the feature was activated by setting bit 2 in the acquisition control register. The bank full flags (B1_FULL and B2_FULL) are cleared with the KEY, at the same time a first start is generated if AUTOSTART is enabled also. Data will be acquired into memory bank 1 until the bank is full. At this point the flag B1_FULL will be set and acquisition changes over to bank 2 (if the flag B2_FULL is not set). The user can read out data from bank 1 in parallel to ongoing acquisition into bank 2 and clear the B1_FULL flag after the readout was completed. As soon as memory bank 2 is filled acquisition will be handed over to bank 1 again if B1_FULL has been cleared already.
The active memory bank will acquire data until the bank is filled if a KEY-STOP_AUTO_BANK_SWITCH is issued.

10.2 consumption

The SIS3300 is a single supply design to facilitate operation in any VME environment, i.e. the module does not require special backplanes or non standard VME voltages.
The power consumption of a two memory bank module digitizing at 100 MHz was measured to be:

Voltage	Current
+ 5V	< 6A
+12 V	< 40 mA
- 12 V	< 60 mA
P < 32 W	

10.3 Operating conditions

10.3.1 Cooling

Although the SIS3300 is mainly a 2.5 and 3.3 V low power design, substantial power is consumed by the Analog to Digital converter chips. Hence forced air flow is required for the operation of the board. The board may be operated in a non condensing environment at an ambient temperature between 10? and 40? Celsius. A power up warm up time of some 10 minutes is recommended to ensure equilibrium on board temperature conditions.

10.3.2 Hot swap/live insertion

Please note, that the VME standard does not support hot swap by default. The SIS3300 is configured for hot swap in conjunction with a VME64x backplane. In non VME64x backplane environments the crate has to be powered down for module insertion and removal.

10.4 P2 row A/C pin assignments

The P2 connector of the SIS3300 has several connections on rows A and C for the F1002 compatible use at the DESY H1 FNC subdetector. This implies, that the module can not be operated in a VME slot with a special A/C backplane, like VSB e.g.. The pin assignments of P2 rows A/C of the SIS3300 is shown below:

P2A	Function	P2C	Function
1	-5.2 V	1	-5.2 V
2	-5.2 V	2	-5.2 V
3	-5.2 V	3	-5.2 V
4	not connected	4	not connected
5	not connected	5	not connected
6	DGND	6	DGND
7	P2_CLOCK_H	7	P2_CLOCK_L
8	DGND	8	DGND
9	P2_START_H	9	P2_START_L
10	P2_STOP_H	10	P2_STOP_L
11	P2_TEST_H	11	P2_TEST_L
12	DGND	12	DGND
13	DGND	13	DGND
14	DGND	14	DGND
15	DGND	15	DGND
16	not connected	16	not connected
...	...	17	...
31	not connected	18	not connected

10.5 Row d and z Pin Assignments

The SIS3300 is prepared for the use with VME64x and VME64xP backplanes. Foreseen features include geographical addressing (PCB revisions V2 and higher) and live insertion (hot swap). The prepared pins on the d and z rows of the P1 and P2 connectors are listed below.

Position	P1/J1		P2/J2	
	Row z	Row d	Row z	Row d
1		VPC (1)		
2	GND	GND (1)	GND	
3				
4	GND		GND	
5				
6	GND		GND	
7				
8	GND		GND	
9		GAP*		
10	GND	GA0*	GND	
11	RESP*	GA1*		
12	GND		GND	
13		GA2*		
14	GND		GND	
15		GA3*		
16	GND		GND	
17		GA4*		
18	GND		GND	
19				
20	GND		GND	
21				
22	GND		GND	
23				
24	GND		GND	
25				
26	GND		GND	
27				
28	GND		GND	
29				
30	GND		GND	
31		GND (1)		GND (1)
32	GND	VPC (1)	GND	VPC (1)

Note: Pins designated with (1) are so called MFBL (mate first-break last) pins on the installed 160 pin connectors, VPC(1) pins are connected via inductors.

10.6 Connector types

The VME connectors and the two different types of front panel connectors used on the SIS3300 are:

Connector	Purpose	Part Number
160 pin zabcd	VME P1/P2	Harting 02 01 160 2101
LEMO PCB	Coax. control connector	LEMO EPB.00.250.NTN
90^{o} PCB LEMO	Analog input connector	LEMO EPL.00.250.NTN

11 Future firmware extensions

The first firmware revision (major and minor revision level 1) was developed to cover the requirements of the DESY H1 FNC and to provide a solid base for more advanced applications. In the meantime trigger functionality and other features have been added. Future extensions will comprise the implementation of:

? MBLT64 and 2eMBLT64
? readout sparsification

More functionality, like on the fly data processing and filtering, can be implemented with given user feedback as the need arises.

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