VMIVME-6015
Quad-Serial Input/Output Interface Board

Product Manual

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500-006015-000 Rev. U

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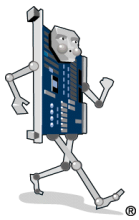

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VMIC Safety Summary

NOTE The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product. VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

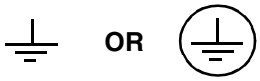
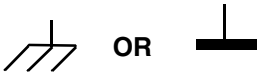
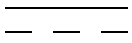
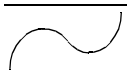
Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing, and adjusting.

Safety Symbols

General definitions of safety symbols used in this manual:

Symbol	Description
	Product manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the product manual in order to protect against damage to the system.
	Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).
	Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.
	Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manal.
	Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.
	Alternating current (power line).
	Direct current (power line).
	Alternating or direct current (power line).

Symbol	Description
WARNING	**WARNING** denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.
CAUTION	**CAUTION** denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.
NOTE	**NOTE** denotes important information. It calls attention to an operating procedure, a practice, a condition, or the like, which is essential to highlight.

CHAPTER

1

Introduction

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Introduction to the VMIVME-6015

The VMIVME-6015 is a quad-channel, multifunctional Serial Input/Output (SIO) peripheral interface board, designed to satisfy a wide variety of serial data communications requirements in VMEbus systems. The basic function of the VMIVME-6015 is a serial-to-parallel, parallel-to-serial, controller; however, it is software configurable so that its "personality" may be optimized for any given serial data communications application.

The VMIVME-6015 is capable of handling asynchronous protocols, synchronous byte-oriented protocols (such as IBM Bisync) and synchronous bit-oriented protocols (such as HDLC and IBM SDLC). This SIO controller can also be used to support virtually any serial protocol for applications other than data communications (cassette or floppy disk interface, for example).

The VMIVME-6015 can generate and check Character Recognition Codes (CRCs) in any synchronous mode and may be programmed to check data integrity in various modes. The controller also has facilities for modem controls and in applications where these controls are not needed the modem controls may be used for general purpose I/O.

The VMIVME-6015 is designed with two MK68564 SIO dual-channel multifunction peripheral circuits that support a self-test capability. When the loop mode bit is set in the command register, the loop mode is activated to support Built-in-Test functions.

The VMIVME-6015 supports the following features:

- Four independent full duplex channels
- Directly addressable registers (all control registers are read/write)
- Data rates in synchronous or asynchronous modes
- 0 to 1 Mbits/s transfer rate
- Self-test capability
- Receive data registers are quadruply buffered, transmit registers are doubly buffered
- Each channel may be independently configured for RS-232, RS-422, RS-423 or RS-485, or as a low cost RS-485 token passing network
- Modem status can be monitored
- Separate modem controls for each channel
- Asynchronous features
  - -- 5, 6, 7 or 8 bits per character
  - -- 1, 1-1/2 or 2 stop bits
  - -- Even, odd, or no parity
  - -- x1, x16, x32 and x64 clock modes
  - -- Break generation and detection
  - -- Parity, overrun and framing error detection
- Byte synchronous features
  - -- Internal or external character synchronization
  - -- One or two sync characters in separate registers
  - -- Automatic sync character insertion
  - -- CRC-16 or CRC-CCITT block check generation and checking
- Bit synchronous features
  - -- Abort sequence generation and detection
  - -- Automatic zero insertion and deletion
  - -- Automatic flag insertion between messages
  - -- Address field recognition
  - -- I-field residue handling
  - -- Valid receive messages protected from overrun
  - -- CRC-CCITT block check generation and checking

Description and Specifications

The following are sources for description and specification information.

The Quad-serial Input/Output Interface Board specification (Document number 800-006015-000) is available from:

VMIC
12090 South Memorial Parkway
Huntsville, AL 35803-3308
PH: 256-880-0444
1-800-240-7782
FX: 256-650-7245
Email: customer.service@vmic.com
Internet: www.vmic.com
PDF for the VMIVME-6015: www.vmic.com/products/chap7/pdf/800-006015-000.pdf

The MK68564 Serial Input Output specification is available from:

STMicroelectronics
1000 East Bell Road
Phoenix, AZ 85022
PH: 602-485-6100
FX: 602-485-6102
Internet: www.us.st.com
PDF for the MK68654: www.us.st.com/stonline/books/pdf/docs/2337.pdf

The Epic Ei68C153 Bus Interrupter Module (VME) specification is available from:

Epic Semiconductor, Inc.
4801 S. Lakeshore Dr.
Suite 203
Tempe, AZ 85282
PH: 480-730-1000
FX: 480-838-4740
Internet: www.epicsemi.com
PDF for the Ei68C153: www.epicsemi.com/153.pdf

Motorola MC68153 BIM

The VMIVME-6015 was originally manufactured using the Motorola MC68153 BIM, which is now out of production. The Epic Ei68C153 BIM is being used as a replacement on all newly-manufactured VMIVME-6015 boards. Any references to the Ei68C153 in this document are also applicable to the MC68153.

CHAPTER

2

Theory of Operation

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Introduction

The VMIVME-6015 Board is a quad-channel, multifunctional Serial Input/Output (SIO) Board designed to satisfy a wide variety of serial data communication requirements in microcomputer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller; however, within that role, it is system software configurable, so that its "personality" may be optimized for any given serial data communications application.

The VMIVME-6015 is capable of handling asynchronous protocols, synchronous byte-oriented protocols (such as IBM Bisync) and synchronous bit-oriented protocols (such as HDLC and IBM SDLC).

The VMIVME-6015 can generate and check Character Recognition Codes (CRCs) in any synchronous mode and may be programmed to check data integrity in various modes. The VMIVME-6015 also has facilities for modem controls in each channel.

Functional Description

A detailed functional block diagram of the VMIVME-6015 is shown in Figure 2-1 on page 21. SIO data is supplied to the front panel subminiature "D" connectors and on-board signal conditioning electronics is provided to support EAI RS-232, RS-422, RS-423 and RS-485 compatible signals. Input signal conditioning options are independently jumper-selectable by the user. Two MK68564 SIO integrated circuits are provided for serial-to-parallel conversion and parallel-to-serial conversion. A Bus Interrupter Module (BIM) Ei68C153 is provided to support the interrupts generated by the SIO integrated circuits.

Address Logic

The VMIVME-6015 Board is designed with address decode logic that allows the user to select a board jumper address within the short I/O memory address map. An 8-bit DIP switch is designed to provide inputs to the address comparator as shown in Figure 2-2 on page 22. A comparison is made with address bits A08 through A15. A jumper (AM) is provided, as shown in Figure 2-2, that gives the user the option of selecting short supervisory or nonprivileged I/O transfers.

The eight least significant bits (LSBs) of address (A01 through A07) are used by the VMIVME-6015 for internal I/O register transfers.

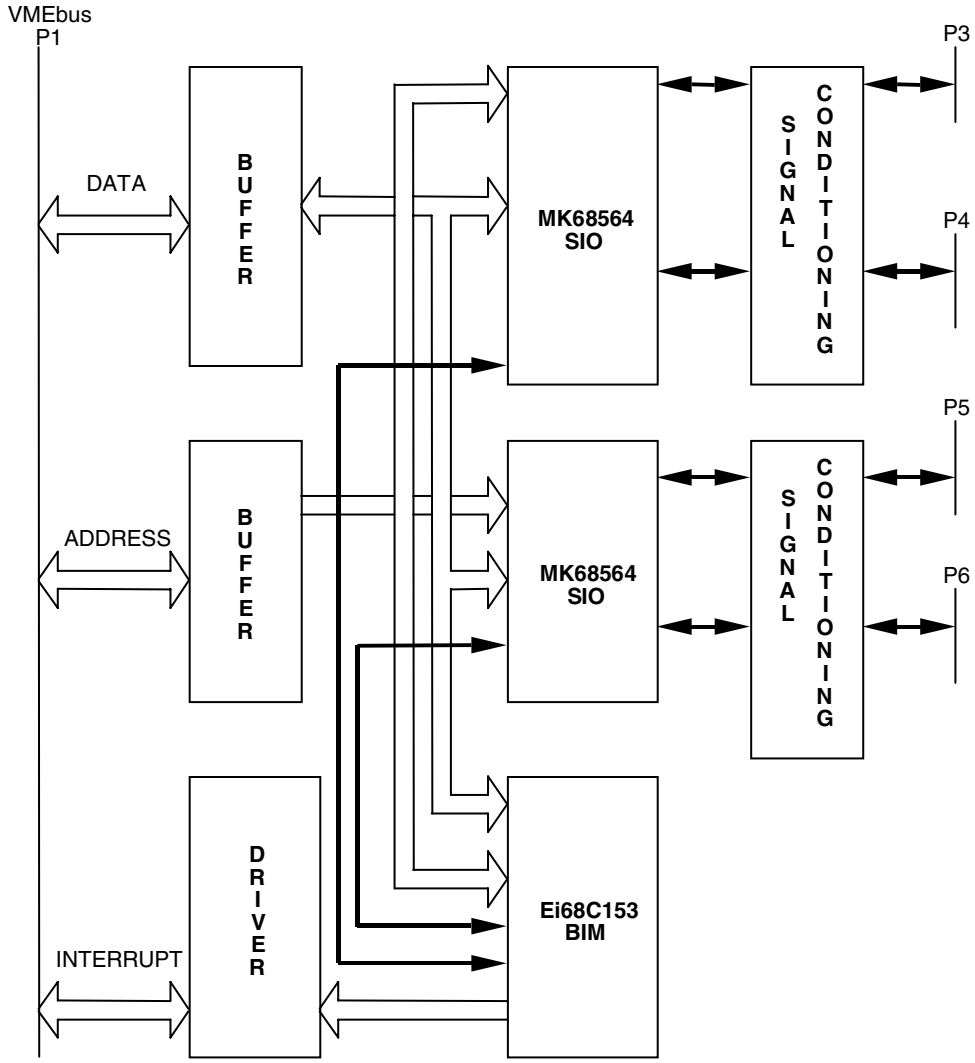

Figure 2-1 Block Diagram of VMIVME-6015

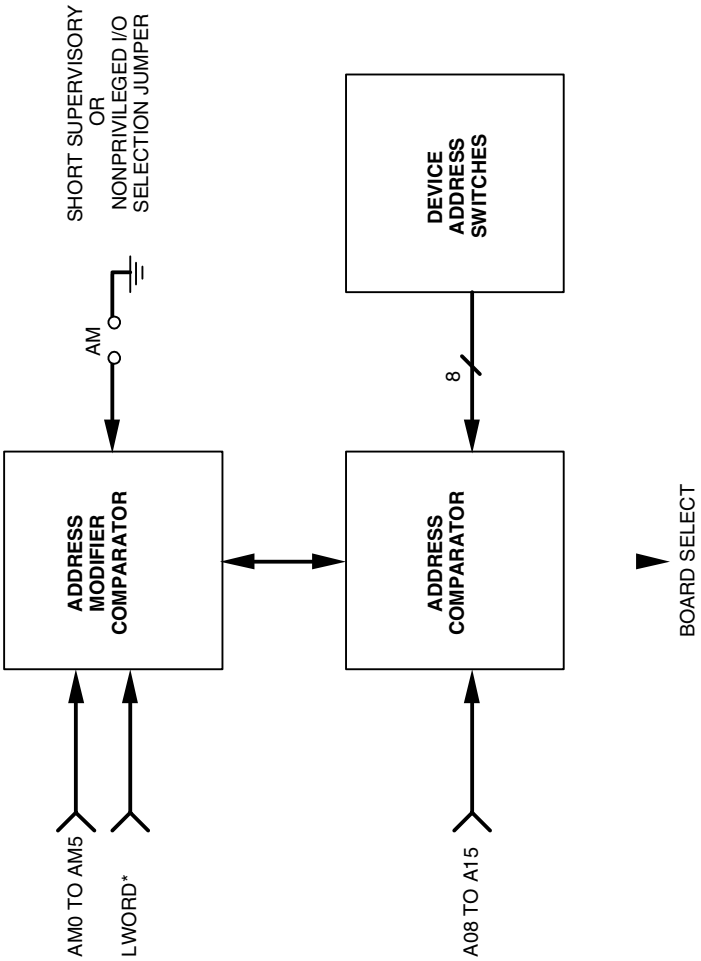

Figure 2-2 Device Address Selection

VMEbus Foundation Logic

The VMIVME-6015 foundation logic consists primarily of an 8-bit data I/O buffer, a control signal buffer, a DTACK generator and a BIM. Additional logic is provided to generate the clock signals for the MK68564 SIO integrated circuit. A functional block diagram of the foundation logic is shown in Figure 2-3 on page 26.

Interrupt Logic

A detailed functional block diagram of the interrupt logic is shown in Figure 2-4 on page 27. The VMIVME-6015 is designed with Epic's Ei68C153 BIM. Only two of the four channels available on Ei68C153 are used by the VMIVME-6015. Channel 3 of the BIM is used for serial Channels 0 and 1, and Channel 2 of the BIM is used for serial Channels 2 and 3.

The MK68564 SIO integrated circuit is designed to operate as an independent, interrupting "peripheral". It contains an Internal Vector Register (IVR); therefore, the Ei68C153 must be programmed so that it will not generate vector data and DTACK.

The Vector Register within the MK68564 is different from the other 24 registers within the SIO chip, because it may be accessed through either Channel "A" or Channel "B" of the SIO during an R/W cycle. During an interrupt acknowledge cycle, the contents of the Vector Register are passed to the VMEbus to be used as a pointer to an interrupt service routine. If the status affects vector bit is low in the Interrupt Control Register (ICR) any data written to the Vector Register will be returned unmodified during a read cycle or an IACK cycle. If the status affects vector bit is high, the lower three bits of the vector returned during a read or IACK cycle are modified to reflect the highest priority interrupt pending in the SIO at that time. The upper five bits written to the Vector Register are unaffected. After a hardware reset, this register contains an "0F" HEX value which is the uninitialized interrupt vector assignment of the 680XX CPU.

MK68564 Serial Input/Output (SIO) Integrated Circuit

The MK68564 SIO is a VLSI designed for a simple and efficient interface to the VMEbus. All data transfers between the MK68564 SIO and the VMEbus Central Processing Unit (CPU) are asynchronous to the system clock.

The MK68564 SIO chip offers an elaborate interrupt scheme to provide fast interrupt response in real-time applications. The interrupt vector points to an interrupt service routine in the CPU memory. To service operations in both MK68564 SIO channels and to eliminate the necessity of writing a status analysis routine (as required for a polling scheme), the MK68564 SIO can modify the interrupt vector so it points to one of eight interrupt service routines.

The VMIVME-6015 contains two sources of clocks to generate a wide variety of baud rates. Jumper selection is provided as shown in Figure 2-5 on page 30. Details concerning the baud rates are provided in Section 4.

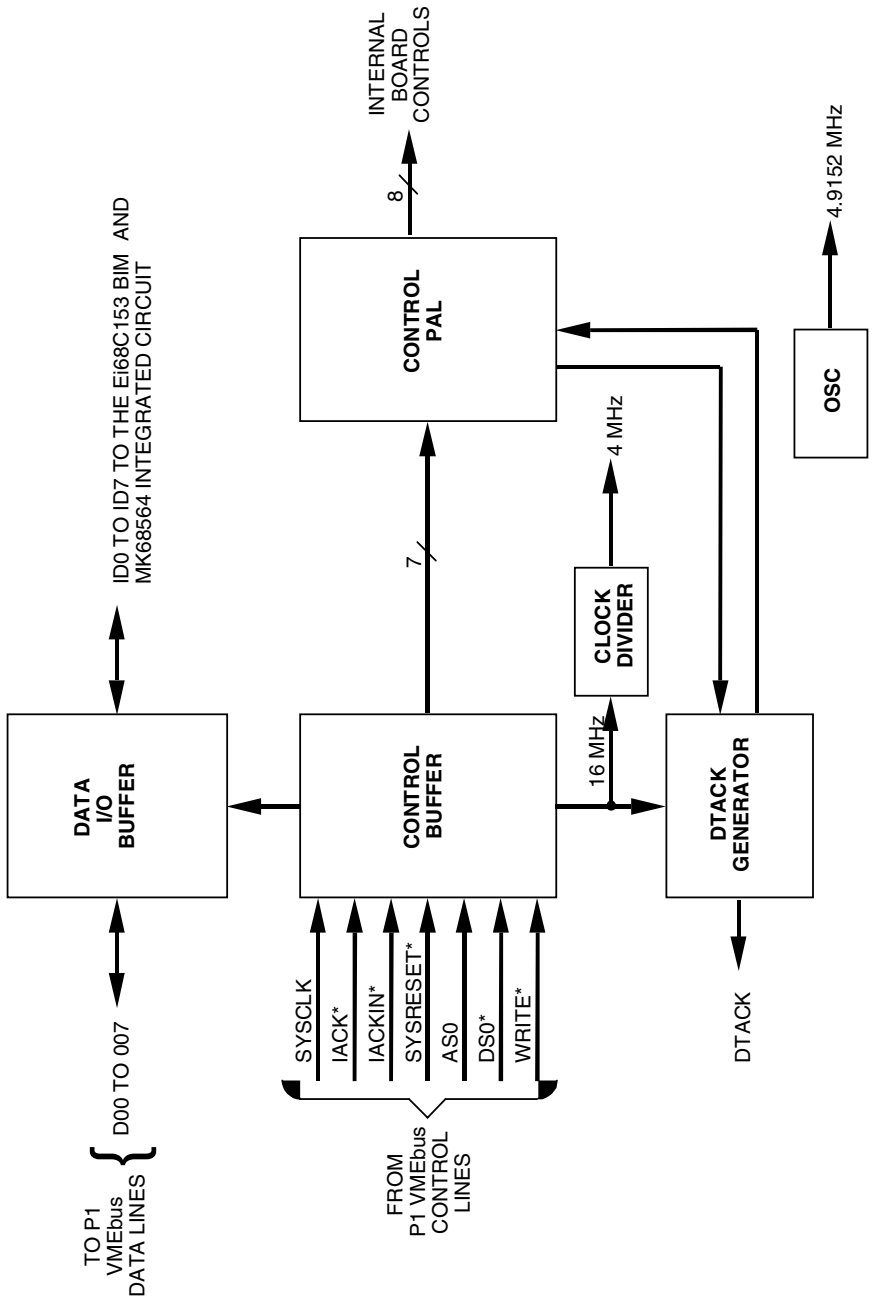

Figure 2-3 VMEbus Foundation Logic

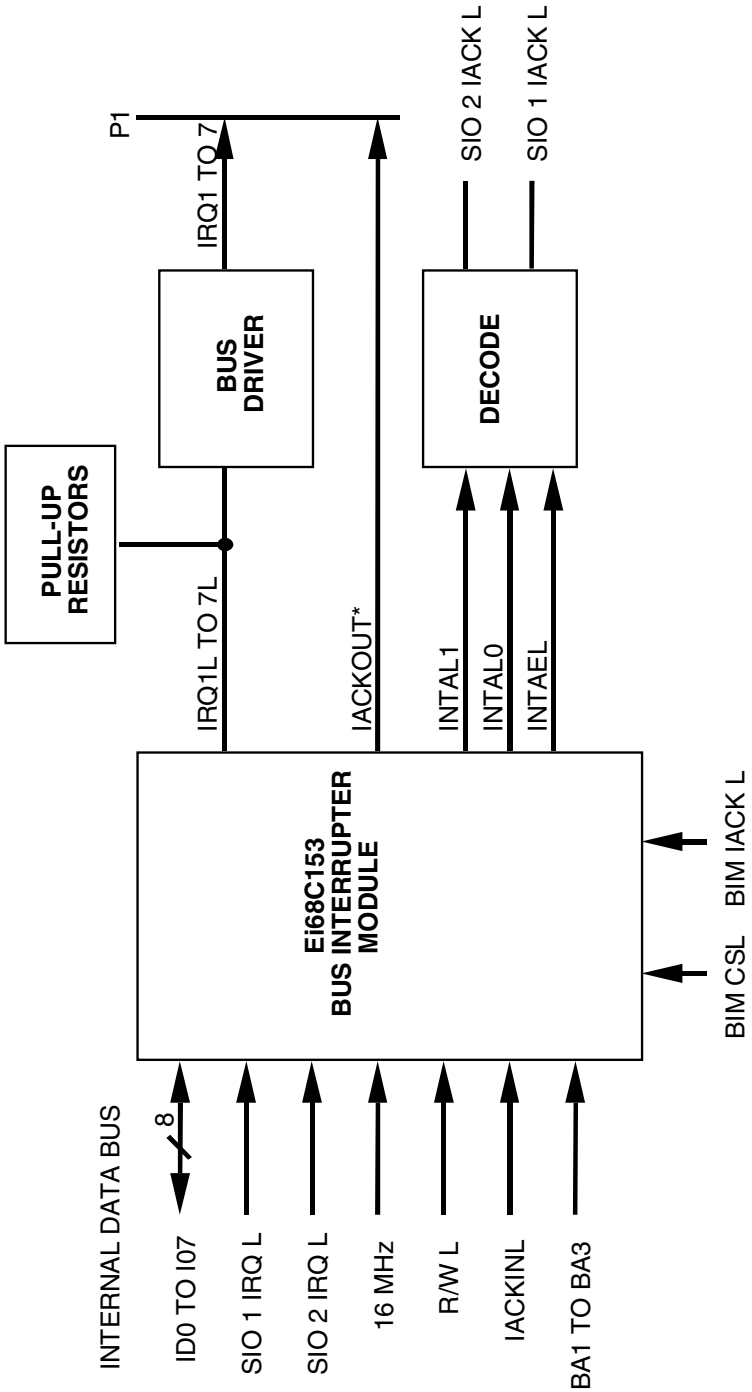

Figure 2-4 Interrupter Functional Block Diagram

Self-Test

The MK68564 SIO chip is designed with internal self-test logic that supports a loop test on each channel.

When the loop mode bit is set in the command register, the receiver shift clock input pin (RxC) and the receiver data input pin (RxD) are electrically disconnected from the internal logic. The transmit data output pin (TxD) is connected to the internal receiver data logic and the transmit shift clock pin (TxC) is connected to the internal receiver shift clock logic. All other features of the MK68564 SIO are unaffected.

RS-485 Token Passing Network

The VMIVME-6015 SIO interface provides an easy connection to the new RS-485 interface standard. RS-485 is an upgraded version of the earlier RS-422 standard for balanced voltage digital interface circuits. Up to 32 RS-485 devices can be multidropped onto a single low cost 24-gauge twisted-pair cable, forming a half duplex network (see Figure 2-6 on page 31). The RS-485 transmitter in the VMIVME-6015 is controlled via the RS-232 request-to-send signal. The RS-485 interface is typically capable of 0 to 100 Kbaud at distances up to 4,000 feet.

A network of RS-485 devices would normally be implemented in a token bus topology. All devices would be wired in line, one after another, forming a single main bus. One device would have the (imaginary) token and thereby the ability to transmit onto the bus. All the RS-232 devices connected to the bus via a VMIVME-6015 need to share some common software in order to determine which device has possession of the token and to control their request-to-send signals.

RS-485 improvements over RS-422 include higher receiver input impedance, increased generator drive and a greater common mode voltage range. The VMIVME-6015 will operate with a common mode voltage (ground potential difference) of ±7 V peak. This means that the ground voltage difference between any two VMIVME-6015s in a network can be up to 7 V. Since the signal grounds between RS-485 devices are normally not connected, problems caused by ground loop currents are virtually eliminated. This fact, along with the inherent common mode noise rejection of differential transmission, makes RS-485 a viable interface for multipoint communication in both data processing and industrial control applications.

In the interval between the time when one transmitter releases the line and another transmitter becomes active, the line is "floating". During this floating period, noise can very easily be picked up by the RS-485 receivers. This will produce erroneous data on the RS-232 output. The software controlling the network will normally interrogate all received characters and thereby reject this noise input.

A situation which must be avoided is noise received immediately prior to the line becoming active and the transmission of the first data character. This noise triggers the asynchronous receiver element in the associated equipment, causing one or more characters of the real data to be missed. One way to reduce this possibility is to provide a slight time delay between when the RS-485 generator becomes active and when the first data character is transmitted.

Other types of networks include those with a single transmitter and multiple receivers and those with a single receiver and multiple transmitters (see Figure 2-7 and Figure 2-8 on page 33). Both types of these networks are commonly used where there is one controlling device (master) and several devices being controlled (slaves). This network allows full duplex operation over two pairs of twisted-pair wire.

Figure 2-9 on page 33 shows two VMIVME-6015s being used as simple line drivers. Control of the RS-232 RTS signal is not required in this application.

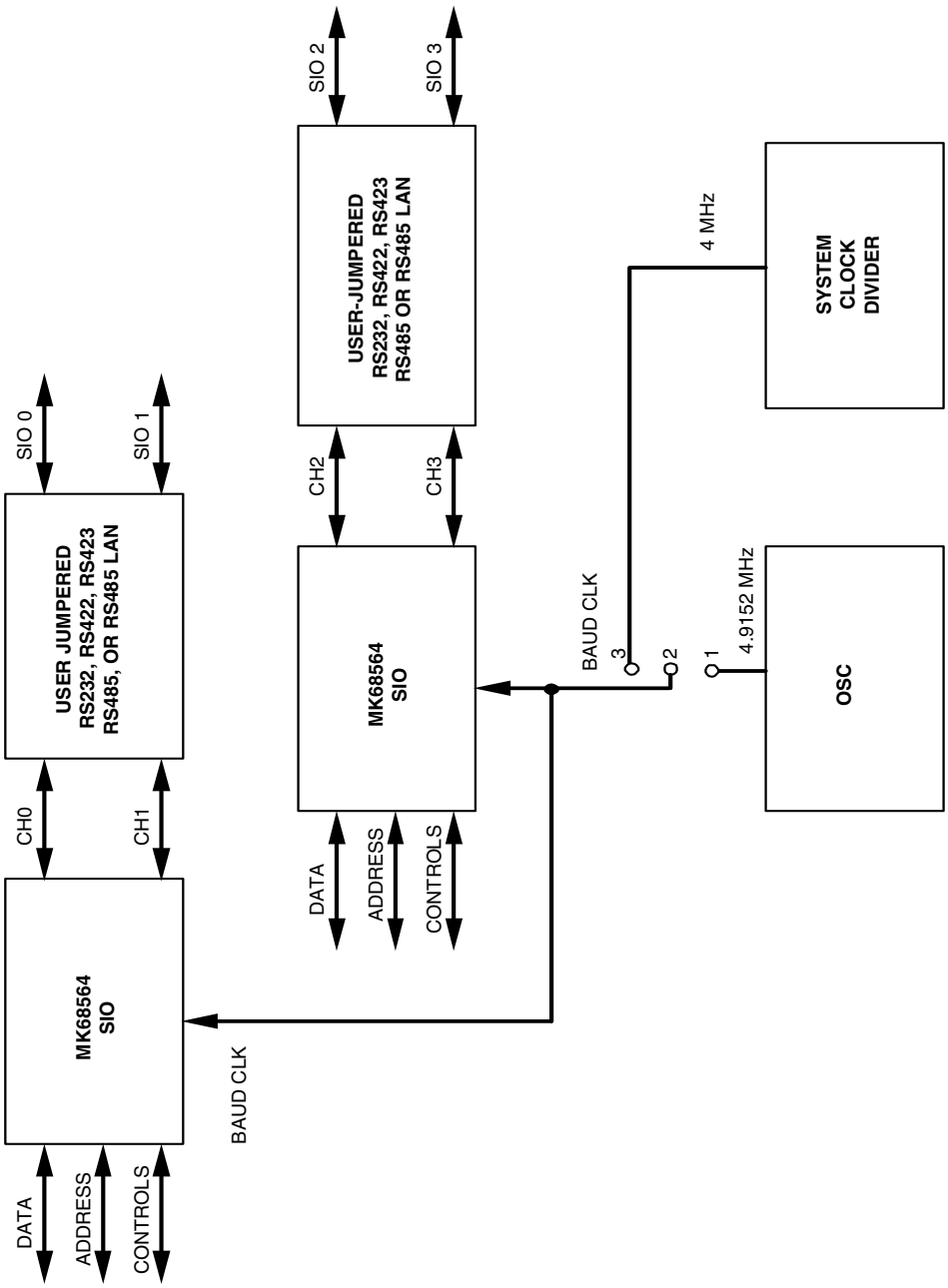

Figure 2-5 SIO Configuration

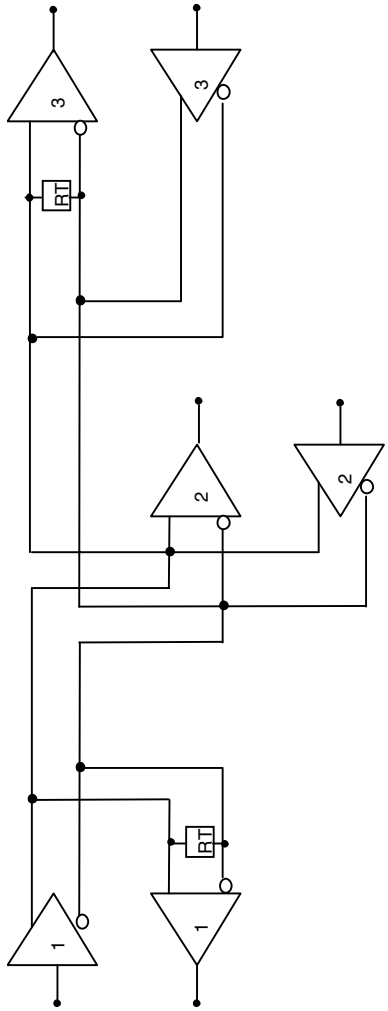

Figure 2-6 RS485 Half Duplex Network

Terminations

Termination resistors are provided by the VMIVME-6015 to terminate the ends of the transmission line(s). Termination is used to reduce reflections on a transmission line. Reflections are due primarily to capacitive loading. Proper termination becomes increasingly important as baud rate and line length increases.

There are two general classes of transmission; single direction transmission and bidirectional transmission. A single direction transmission line, comprised of a single transmitter and a single receiver, is normally terminated only at the receiver end of the line. A single direction transmission line, comprised of a single transmitter and multiple receivers, is normally terminated at both ends of the line. A bidirectional transmission line, comprised of multiple transmitters and one or more receivers, is normally terminated at both ends of the line.

Proper termination means that the transmission line is terminated at its end(s) in a resistive value close to its characteristic impedance. A 24-gauge twisted-pair wire, which is a common RS-422/-485 cable, typically has a characteristic impedance of about 100Ω. RS-422A generator circuits are specified to drive a maximum load of 100Ω. RS-485 generator circuits have increased drive capability and are specified to drive a maximum load of 60Ω. This means that the user would normally terminate a bidirectional line at both ends with 120Ω terminations only if all generators on that line are RS-485 compatible. The generators in the VMIVME-6015 may be configured for RS-485. If one or more generators on a bidirectional line are only RS-422A compatible (less drive capability), the user should probably use 240Ω termination at each end.

Having the terminations exactly match the characteristic impedance of the transmission line is usually not critical to most RS-422/-485 applications. The termination values would only be of critical importance when the limits of baud rate and/or line length are being driven to the maximum.

Sometimes the final value chosen for termination will be a trade-off between the wave shape and the voltage swing of the signal. RS-485 and RS-422A networks are designed to be wired in a point-to-point fashion. All devices are wired in line, one after another forming a single main line (a bus topology). Stub lengths off of the main line are not recommended. If a RS-485 receiver is not being used (left disconnected), it is possible that noise on the inputs will be generated; therefore, the user should ground all unused inputs.

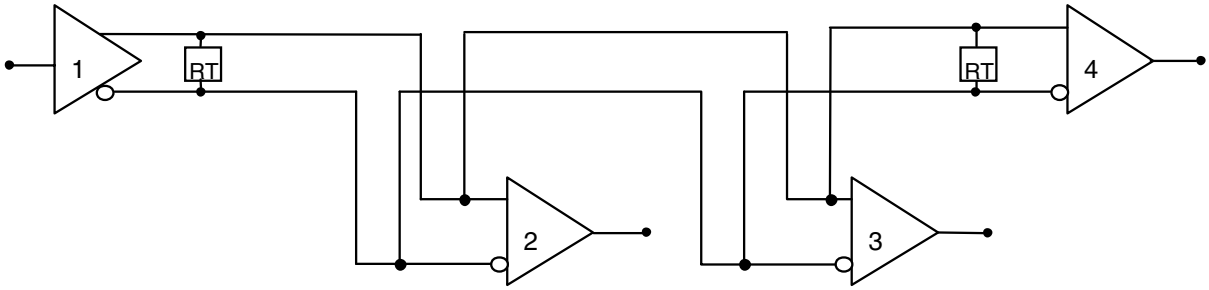

Figure 2-7 Single Transmitter and Multiple Receiver

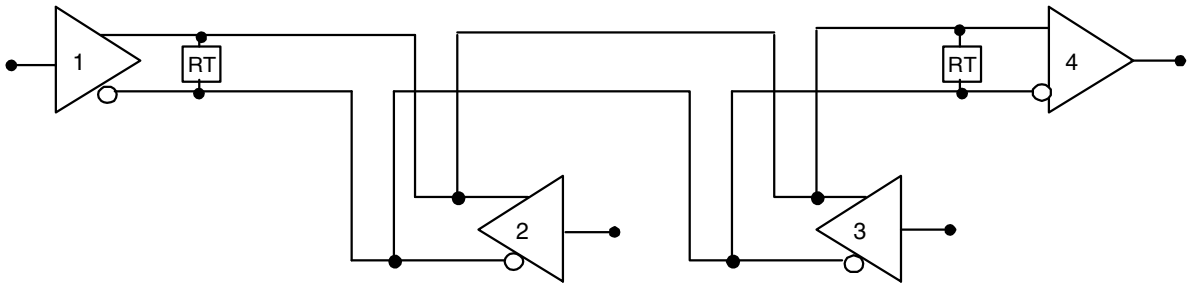

Figure 2-8 Single Receiver and Multiple Transmitter

Figure 2-9 Simple Line Driver

CHAPTER

3

Programming

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Introduction

This section describes the programming requirements for the VMIVME-6015 Serial Input/Output (SIO) Board. The VMIVME-6015 SIO Board is designed with two MK68564 SIO integrated circuits, each of which contains a transmitter, a receiver, modem control logic, interrupt control logic, a Baud Rate Generator (BRG), ten read/write registers and two read only status registers. Each channel can communicate with the Central Processing Unit (CPU) using polling or interrupts, or both. Each channel also has the ability to connect the transmitter output into the receiver without disturbing any external hardware.

MK68564 SIO Register Set

The register set is the heart of each channel. A channel may be configured for different communication protocols and interface options by programming these registers. Each register group associated with each I/O channel is defined with its addresses as shown in Table 3-1 on page 52. Detailed register bit maps are provided in Table 3-2 on page 54 through Table 3-5 on page 57. Additional addressing and register bit definitions are provided in Table 3-6 on page 58.

Register Description

The following paragraphs describe the MK68564 SIO registers. Each register is detailed in terms of bit configuration, the active states of each bit, bit definitions, bit functions and their effects upon the internal hardware and external pins.

CMDREG (Command Register)

This register contains command and reset functions used in programming the SIO. This register is reset to OOH by a channel or by hardware reset. All bits, except loop mode will be read as "zeros" during a read cycle.

Bits D7 and D6

CRC reset codes "one" and "zero".

NULL CODE

The **NULL CODE** has no effect on the MK68564 SIO. It is used when writing to the CMDREG for any reason other than a CRC reset.

RESET RECEIVER CRC CHECKER

It is necessary in synchronous modes (except SDLC) to reset the receiver CRC circuitry between received messages. The CRC circuitry may be reset by one of the following: disabling the receiver, setting the enter hunt mode bit in the Receiver Control Register (RCR), or issuing this reset command. The CRC circuitry is reset automatically in SDLC mode when the end of frame flag is detected. This reset command will initialize the CRC checker circuit to all "ones" in SDLC mode and all "zeros" in the other synchronous modes.

RESET TRANSMIT CRC GENERATOR

This command resets the CRC generator to all "ones" in SDLC mode and all "zeros" in the other synchronous modes. This command should be issued after the transmitter is enabled, but before the first character of a message is loaded into the transmit buffer.

RESET TRANSMIT UNDERRUN/EOM LATCH

This command resets the Underrun/EOM Latch in status register 0 if the transmitter is enabled. The Underrun/EOM Latch controls the transmission of CRC at the end of a message in synchronous modes. When a transmit underrun occurs and this latch is low, CRC will be appended to the end of the transmission.

Bits D5, D4 and D3

Command Codes.

COMMAND 0 (NULL)

The null command has no effect on the MK68564 SIO.

COMMAND 1 (Send Abort - SDLC)

This command is used in SDLC mode to transmit a sequence of eight to 13 "ones". This command always empties the transmit buffer and sets the transmit Underrun/EOM Latch in status register 0 to a "one".

COMMAND 2 (Reset External/Status Interrupts)

After an external status interrupt (a change on a modem line or a break condition, for example), the upper five bits in status register 0 are latched. This command re-enables these bits and allows interrupts to occur again as a result of a status change. Latching the status bits captures short pulses, until the CPU has time to read the change. This command should be issued prior to enabling external status interrupts.

COMMAND 3 (Channel Reset)

This command disables both the receiver and transmitter, forces TxD to a marking state ("one"), forces the modem control signals high, resets any pending interrupts from this channel and resets all control registers. All Control Registers for the channel must be rewritten after a channel reset command.

COMMAND 4 (Enable Interrupt on Next Rx Character)

This command is used to reactivate the **RECEIVE INTERRUPT ON FIRST CHARACTER ONLY INTERRUPT** mode. This command is normally issued after the present message is completed, but before the next message begins to be assembled. The next character to enter the receive data FIFO after this command is issued will cause a receiver interrupt request.

NOTE If the data FIFO has more than one character stored when this command is issued, the first previously stored character will cause the receiver interrupt request.

COMMAND 5 (Reset Tx Interrupt Pending)

When the transmit interrupt enable mode is selected, the transmitter requests an interrupt when the transmit buffer becomes empty. In those cases, where there are no more characters to be sent (at the end of message, for example), issuing this command resets the pending transmit interrupt and prevents any further transmitter interrupt requests until the next character has been loaded into the transmit buffer, or until CRC has been completely sent.

COMMAND 6 (Error Reset)

This command resets the upper seven bits in Status Register 1. Anytime a special receive condition exists when **RECEIVE INTERRUPT ON FIRST CHARACTER ONLY** mode is selected, the data with the special condition is held in the receive data FIFO until this command is issued.

COMMAND 7 (Null)

The null command has no effect on the MK68564 SIO.

Bits D2 and D1

Not used (read as zeros).

D0 - Loop Mode

When this bit is set to a "one", the transmitter output is connected to the receiver input and TxC (active low) is connected to the receiver clock. RxC (active low) and RxD pins are not used by the receiver; they are bypassed internally. RxC (active low) may still be used as the Baud Rate Generator (BRG) output in loop mode.

MODECTL (Mode Control Register)

The **MODECTL** contains control bits that affect both the receiver and the transmitter. This register must be initialized before loading the interrupt, Tx and Rx Control Registers and the Sync Word Registers. This register is reset to 00 HEX by a channel or by hardware reset.

Bits D7 AND D6 - Clock Rate 1 and 0

These bits specify the multiplier between the input shift clock rates (TxC (active low) and RxC (active low)) and the data rate. The same multiplier is used for both the transmitter and receiver, although the input clock rates may be different. In x16, x32 and x64 clock modes, the receiver start bit detection logic is enabled; therefore, for synchronous modes, the x1 clock rate must be specified. Any clock rate may be specified for asynchronous mode; however, if the x1 clock rate is selected, synchronization between the receive data and the receive clock must be accomplished externally.

Bits D5 and D4 - Sync Modes 1 and 0

These bits select the various options for character synchronization. These bits are ignored unless sync modes is selected in the stop bits field of this register.

Bits D3 and D2 (Stop Bits 1 and 0)

These bits determine the number of stop bits added to each asynchronous character that is transmitted. The receiver always checks for one stop bit in asynchronous mode. A special code (00) signifies that a synchronous mode is to be selected. A one and one half stop bit is not allowed if x1 clock rate is selected because it will lock up the transmitter.

Bit D1 - Parity Even/odd

If the parity enable bit is set, this bit determines whether parity is checked as even or as odd. (1 = even, 0 = odd). This bit is ignored if the parity enable bit is reset.

Bit D0 - Parity Enable

If this bit is set to "one", one additional bit position beyond those specified in the bits/character control field is added to the transmitted data and is expected in the receive data. The received parity bit is transferred to the CPU as part of the data character, unless eight bits per character is selected in the Receiver Control Register (RCR).

INTCTL (Interrupt Control Register)

This register contains the control bits for the various interrupt modes and the DMA handshaking signals. This register is reset to 00 HEX by a channel or by hardware reset.

Bit D7 - CRC-16/SDLC-CRC

This bit selects the CRC polynomial used by both the transmitter and receiver. When set to a "one", the CRC-16 polynomial ($x^{16} + x^{15} + x^2 + 1$) is used; when reset to a "zero", the SDLC-CRC polynomial ($x^{16} + x^{12} + x^5 + 1$) is used. If the SDLC mode is selected, the CRC generator and checker are preset to all "ones" and a special check sequence is used. The SDLC-CRC polynomial must be selected in SDLC mode. Failure to do so will result in receiver CRC errors. When a synchronous mode, other than SDLC, is selected the CRC generator and checker are preset to all "zeros" (for both polynomials). This bit must be programmed before CRC is enabled in the receiver and transmitter Control Registers, to assure valid CRC generation and checking. This bit is ignored in asynchronous modes.

Bit D6 - Tx Ready Enable

When this bit is set to a "one", the TxRDY (active low) output pin will pulse low for three clock cycles when the transmit buffer becomes empty. When this bit is "zero", the TxRDY (active low) pin is held high.

Bit D5 - Rx Ready Enable

When this bit is set to a "one", the RxRDY (active low) output pin will pulse low for three clock cycles when a character is available in the receive buffer. If a special receive condition is detected when the **RECEIVE INTERRUPT ON FIRST CHARACTER ONLY** interrupt mode is selected, the RxRDY (active low) pin will not become active; instead, a special receive condition interrupt will be generated. When this bit is "zero", the RxRDY (active low) pin will be held high.

Bits D4 and D3 - Receive Interrupt Modes 1 and 0

Together, these two bits specify the various character available conditions that will cause interrupt requests. When receiver interrupts are enabled, a special receive condition can cause an interrupt request and modify the interrupt vector. Special receive conditions are: Rx overrun error, framing error (in async mode), end of frame (in SDLC mode) and parity error (when selected). The Rx overrun error and the parity error conditions are latched in Status Register 1 when they occur; they are cleared by an error reset command (Command 4) or by a hardware or channel reset.

RECEIVE INTERRUPTS DISABLED

This mode prevents the receiver from generating an interrupt request and clears any pending receiver interrupts. If a character is available in the receiver data FIFO, or if a special receive condition exists before or during the time receiver interrupts are disabled and receiver interrupts are then enabled without clearing these conditions, an interrupt request will immediately be generated.

RECEIVE INTERRUPT ON FIRST CHARACTER ONLY

The receiver requests an interrupt in this mode on the first available character (or stored FIFO character), or on a special receive condition. If a special receive condition occurs, the data with the special condition is held in the receive data FIFO until an error reset command (command 6) is issued.

THE RECEIVE INTERRUPT ON FIRST CHARACTER ONLY

The **RECEIVE INTERRUPT ON FIRST CHARACTER ONLY** mode can be re-enabled by the enable interrupt on next Rx character command (command 4). If this interrupt mode was terminated by a special receive condition, the error reset command must be issued before command 4 for proper operation to resume.

INTERRUPT ON ALL RECEIVE CHARACTERS

This mode allows an interrupt for every character received (or character in the receive data FIFO) and provides a unique vector (if status affects vector is enabled) when a special receive condition exists. When the interrupt request is due to a special condition, the data containing that condition is not held in the receive data FIFO.

Bit D2 - Status Affects Vector

When this bit is "zero", the value programmed into the Vector Register is returned during a read cycle or an interrupt acknowledge cycle. If the Vector Register has not been programmed following a hardware reset, then 0F HEX is returned.

When this bit is a "one", the vector returned during a read cycle or an interrupt acknowledge cycle is variable. The variable field returned depends on the highest priority pending interrupt at the start of the cycle.

The status affects vector control bits from both channels are logical "ORed" together; therefore, if either is programmed to a "one", its operation affects both channels. This is the only control bit that functions in this manner on the MK68564.

NOTE Special receive conditions: parity error, Rx overrun error, framing error (async), end of frame (SDLC).

Bit D1 - Transmit Interrupt Enable

When this bit is set to a "one", the transmitter will request an interrupt whenever the transmit buffer becomes empty. When this bit is "zero", no transmitter interrupts will be requested.

Bit D0 - External Status Interrupt Enable

When this bit is set to a "one", an interrupt will be requested by the external status logic on any of the following occurrences: a transition (high-to-low or low-to-high) on the DCD (active low), CTS (active low), or SYNC (active low) input pins, a break/abort condition that has been detected and terminated, or at the beginning of CRC transmission when the transmit Underrun/EOM Latch in status register 0 becomes set. When this bit is "zero", no external status interrupts will occur.

If this bit is set when an external status condition is pending, an interrupt will be requested. It is recommended that a reset external/status interrupt command (command 2 in the command register) be issued prior to enabling external status interrupts.

SYNC 1 (SYNC Word Register 1)

This register is programmed to contain the transmit sync character in the monosync mode, the first eight bits of the 16-bit sync character in the bisync mode, or the transmit sync character in the external sync mode. This register is not used in asynchronous mode. In the SDLC mode, this register is programmed to contain the secondary address field used to compare against the address field of the SDLC frame. The SIO does not automatically transmit the station address at the beginning of a response frame. This register is reset to 00 HEX by a channel or hardware reset.

SYNC 2 (SYNC Word Register 2)

This register is programmed to contain the receive sync character in the monosync mode, the last eight bits of the 16-bit sync character in the bisync mode, or a flag character (01111110) in the SDLC mode. This register is not used in the external sync mode and the asynchronous Mode. This register is reset to 00 HEX by a channel or hardware reset.

RCVCTL (Receiver Control Register)

This register contains the control bits and parameters for the receiver logic. This register is reset to 00 HEX by a channel or hardware reset.

Bits D7 and D6 - Receiver Bits/Character 1 and 0

The state of these two bits determines the number of bits to be assembled as a character in the received serial data stream. If parity is enabled, one additional bit will be added to each character. The number of bits per character can be changed while a character is being assembled, but only before the number of bits currently programmed is reached. All data is right-justified in the shift register and transferred to the receive data FIFO in 8-bit groups.

In asynchronous mode, transfers are made at character boundaries and all unused bits of a character are set to a "one". In synchronous modes and SDLC mode, an 8-bit segment of the serial data stream is transferred to the data FIFO when the internal counter reaches the number of bits programmed for less than eight bits per character, no parity, the most significant bit(s) (MSBs) of the first transfer will be the least significant bit(s) (LSBs) of the next transfer.

Bit D5 - Receiver Auto Enables

When this bit is set to a "one" and the receiver enable bit is also set, a low on the DCD (active low) input pin becomes the enable for the receiver. When this bit is "zero", the DCD (active low) pin is simply an input to the SIO and its status is displayed in status register 0.

Bit D4 - Enter Hunt Mode

This bit, when written to a "one", re-arms the receiver synchronization logic and forces the comparison of the received bit stream to the contents of Sync Word Register 1 and/or Sync Word Register 2, depending upon which synchronous mode is selected, until bit synchronization is achieved. The SIO automatically enters the hunt mode after a channel or hardware reset, after an Abort condition is detected, or when the receiver is disabled. When the hunt mode is entered, the hunt sync bit in status register 0 is set to a "one". When synchronization is achieved, the hunt sync bit is reset to a "zero". If external status interrupts are enabled, an interrupt request will be generated on both transitions of the hunt sync bit. enter hunt mode has no effect in asynchronous modes. This bit is not latched and will always be ready as a "zero".

Bit D3 - Receiver CRC Enable

This bit, when set to a "one" in a synchronous mode other than SDLC, is used to initiate CRC calculation at the beginning of the last byte transferred from the Receiver Shift Register to the receive data FIFO. This operation occurs independently of the number of bytes in the receive data FIFO. As long as this bit is set, CRC will be calculated on all characters received (data or sync). When a particular byte is to be excluded from CRC calculation, this bit should be reset to a "zero" before the next byte is transferred to the receive data FIFO. If this feature is used, care must be taken to ensure that eight bits per character are selected in the receiver because of an inherent 8-bit delay from the Receiver Shift Register to the CRC checker.

When this bit is set to a "one" in SDLC mode, the SIO will calculate CRC on all bits between the opening and closing flags. There is no delay from the Receiver Shift Register to the CRC checker in SDLC mode. This bit is ignored in asynchronous modes.

Bit D2 - Address Search Mode (SDLC)

Setting this bit to a "one" in SDLC mode forces the comparison of the first non-flag character of a frame with the address programmed in Sync Word Register 1 or the global address (11111111). If a match does not occur, the frame is ignored and the receiver remains idle until the next frame is detected. No receiver interrupts can occur in this mode, unless there is an address match. This bit is ignored in all modes except SDLC.

Bit D1 - Sync Character Load Inhibit

When this bit is set to a "one" in any synchronous mode except SDLC, the SIO compares the byte in Sync Word Register 1 with the byte about to be loaded into the receiver data FIFO. If the two bytes are equal the load is inhibited and no receiver interrupt will be generated by this character. CRC calculation is performed on all bytes, whether they are loaded into the data FIFO or not, when the receiver CRC is enabled. Note that the register used in the comparison contains the transmit sync character in monosync and external sync modes. This bit is ignored in SDLC mode because all flag characters are automatically stripped in this mode without performing CRC calculations on them.

If this bit is set to a "one" in asynchronous modes, any character received matching the contents of Sync Word Register 1 will not be loaded into the receive data FIFO and no receiver interrupt will be generated for the character.

Bit D0 - Receiver Enable

When this bit is sent to a "one", receiver operation begins if Rx auto enables mode is not selected. This bit should be set only after all receiver parameters are established and the receiver is completely initialized. When this bit is "zero", the receiver is disabled; the receiver CRC checker is reset and the receiver is in the hunt mode.

XMTCTL (Transmitter Control Register)

This register contains the control bits and parameters for the transmitter logic. This register is reset to 00 HEX by a channel or hardware reset.

Bits D7 and D6 - Transmit Bits/Character 1 and 0

The state of these two bits determine the number of bits in each byte transferred from the transmit buffer to the Transmit Shift Register. All data written to the transmit buffer must be right-justified with the LSBs first. The five or less mode allows transmission of 1 to 5 bits per character; however, the CPU should format the data characters as shown. If parity is enabled, one additional bit per character will be transmitted.

Bit D5 - Transmit Auto Enables

When this bit is set to "one" and the transmit enable bit is also set, a low on the CTS (active low) input pin will enable the transmitter. When this bit is "zero" the CTS (active low) pin is simply an input to the SIO and its status is displayed in status register 0.

Bit D4 - Send Break

When set to a "one", this bit immediately forces the transmit data output pin (TxD) to a spacing condition (continuous zeros), regardless of any data being transmitted at the time. This bit functions whether the transmitter is enabled or not. When this bit is reset to "zero", the transmitter will continue to send the contents of the Transmit Shift Register. The Transmit Shift Register may contain sync characters, data characters, or all "ones".

Bit D3 - Transmitter CRC Enable

This bit determines if CRC calculations are performed on a transmitted data character. If this bit is a "one" at the time, a character is loaded from the transmit buffer to the Transmit Shift Register, CRC is calculated on the character. CRC is not calculated on any automatically inserted sync characters. CRC is not automatically appended to the end of a message unless this bit is set and the transmit Underrun/EOM status bit in status register 0 is reset when a transmit underrun condition occurs. If this bit is a "zero" when a character is loaded from the transmit buffer into the Transmit Shift Register, no CRC calculations are performed on the character. This bit is ignored in asynchronous modes.

Bit D2 - DTR (Data Terminal Ready)

This is the control bit for the DTR (active low) output pin. When this bit is set to a "one", the DTR (active low) pin goes low; when this bit is reset to a "zero", the DTR (active low) pin goes high.

Bit D1 - RTS (Request To Send)

This is the control bit for the RTS output signal. In synchronous modes, when this bit is set to a "one", the RTS signal goes high; when this bit is reset to a "zero", the RTS signal goes low. In asynchronous modes, when this bit is set to a “one”, the RTS signal goes high; when this bit is reset to a “zero”, the RTS signal will go low only after all the bits of the character are transmitted, and the transmit buffer is empty.

The RTS bit is also used to enable/disable the differential circuitry that drives the transmit data when RS-422A, RS-423 and RS-485 differential communications are selected. When the RTS bit is set to a “one” the differential circuitry is disabled; when the RTS bit is reset to a “zero”, the differential circuity is enabled.

NOTE: The RTS bit is Not used to enable/disable the single ended circuity that drives the transmit data when RS-232 single ended communications are selected.

Bit D0 - Transmitter Enable

Data is not transmitted until this bit is set to a "one", until the send break bit is reset and, if Tx auto enables mode is selected, until the CTS (active low) pin is low. To transmit sync or flag characters in synchronous modes, this bit has to be set when the transmit buffer is empty. Data or sync characters in the process of being transmitted are completely sent if this bit is reset to "zero" after transmission has started. If this bit is reset during the transmission of a CRC character, sync or flag characters are sent instead of the CRC character.

STAT 0 (Status Register 0 - Read Only)

This register contains the status of the receive and transmit buffers and the status bits for the five sources of external status interrupts.

Bit D7 - Break/Abort

This bit is reset by a channel or hardware reset. In asynchronous modes, this bit is set when a break sequence (null character plus framing error) is detected in the received data stream. An external status interrupt, if enabled, is generated when break is detected. The interrupt service routine must issue a reset external/status interrupt command (command 2) to the SIO, so the break detection logic can recognize the termination of the break sequence.

The break/abort bit is reset to a "zero" when the termination of the break sequence is detected in the incoming data stream. The termination of the break sequence also causes the generation of a external/status interrupt. Command 2 must be issued to enable the break detection logic to look for the next break sequence. A single extraneous null character is present in the receiver after the termination of a break; it should be read and discarded.

In SDLC mode, this bit is set by the detection of an abort sequence (seven or more "ones") in the received data stream. The external/status interrupt is handled the same way as in the case of a break sequence. The break/abort bit is not used in the other synchronous modes.

Bit D6 - Transmit Underrun/Eom

This bit is set to a "one" following a hardware or channel reset, when the transmitter is disabled or when a send abort command (command 1) is issued. This bit can only be reset by the reset transmit underrun/OEM latch command in the Command Register. This bit is used to control the transmission of CRC at the end of a message in synchronous modes. When a transmit underrun condition occurs and this bit is low, CRC will be appended to the end of the transmission and this bit will be set. Only the "zero" to one transition of this bit causes an external status interrupt, when enabled. This bit is not used in asynchronous modes.

Bit D5 - CTS (Clear To Send)

This bit indicates the inverted state of the CTS (active low) input pin at the time of the last change of any of the five external status bits. Any transition of the CTS (active low) input causes the CTS bit to be latched and generates an external status interrupt request, if enabled. To read the current state of the CTS (active low) pin, this bit must be read immediately following a reset external status interrupts command (command 2).

Bit D4 - Hunt/Sync

In asynchronous modes, this bit indicates the inverted state of the SYNC (active low) input pin at the time of the last change of any of the five external status bits. Any transition of the SYNC (active low) input causes the hunt/sync bit to be latched, if enabled, and generates an external status interrupt request. To read the current state of the SYNC (active low) pin, this bit must be read immediately following a reset external/status interrupt command (command 2).

In external sync mode, the SYNC (active low) pin is used by external logic to signal character synchronization. When synchronization is achieved, the SYNC (active low) pin is driven low on the second rising edge of the receive clock (RxC) (active low) on which the last bit of the sync character was received. Once the SYNC (active low) pin is low, it should be held low until the end of the message and then driven back high. If enabled, both transitions on the SYNC (active low) pin cause external status interrupt requests. The inverted state of the SYNC (active low) pin is indicated by this bit.

In monosync, bisync and SDLC modes, this bit indicates when the receiver is in the hunt mode. This bit is set to a "one" following a hardware or channel reset, after the enter hunt mode bit is written high, when the receiver is disabled, or when an abort sequence (SDLC mode) is detected. This bit will remain in this state until character synchronization is achieved. External status interrupt requests will be generated on both transitions of the hunt sync bit.

Bit D3 - DCD (Data Carrier Detect)

This bit indicates the inverted state of the DCD (active low) input pin at the time of the last change of any of the five external status bits. Any transition of the DCD (active low) input causes the DCD bit to be latched and if enabled, generates an external status interrupt request. To read the current state of the DCD (active low) pin, this bit must be read immediately following a reset external/status interrupts command (command 2).

Bit D2 - Transmit Buffer Empty

This bit is set to a "one" when the transmit buffer becomes empty and when the last CRC bit is transmitted in synchronous or SDLC modes. This bit is reset when the transmit buffer is loaded or while the CRC character is being sent in synchronous or SDLC modes. This bit is set to a "one" following a hardware or channel reset.

Bit D1 - Interrupt Pending

Any interrupt condition, pending in the interrupt control logic for this channel, will set this bit to a "one". This bit is reset to "zero" by a hardware channel reset, or when all the interrupt conditions are cleared.

Bit D0 - Receive Character Available

This bit is set to a "one" when a character becomes available in the receive data FIFO. This bit is reset to "zero" when the receive data FIFO (receive buffer) is read, or by a hardware or channel reset.

STAT 1 (Status Register 1) Read Only

This register contains the special receive condition status bits and the residue codes for the I-field in the SDLC receive mode. The all sent bit is set high and all other bits are reset to a low by a channel or by hardware reset.

Bit D7 - SDLC (End of Frame)

This bit is used only in SDLC mode. When set to a "one", this bit indicates that a valid closing flag has been received and that the CRC framing error bit and residue codes are valid. If receiver interrupts are enabled, a special receive condition interrupt will also be generated. This bit can be reset by issuing an error reset command (command 6). This bit is also updated by the first character of the following frame. This bit is a "zero" in all modes except for SDLC.

Bit D6 - CRC Framing Error

In asynchronous modes, if a framing error occurs, this bit is set to a "one" for the receive character in which the framing error occurred. When this bit is set to a "one", a special receive condition interrupt will be requested, if receiver interrupts are enabled. Detection of a framing error adds an additional one-half bit time to the character time, so that the framing error is not interpreted as a new start bit.

In synchronous and SDLC modes, this bit indicates the result of comparing the received CRC value to the appropriate check value. A "zero" indicates that a match has occurred. This bit is usually set since most bit combinations result in a non-zero CRC, except for a correctly completed message. Receiver interrupts are not requested by the CRC error bit.

The CRC framing bit is not latched in any receiver mode. It is always updated when the next character is received. An error reset command (command 6) will always reset this bit to "zero".

Bit D5 - Receive Overrun Error

This bit indicates that the receive data FIFO has overflowed. Only the character that has been written over is flagged with this error. When the character is read, the error condition is latched until reset by the error reset command (command 6). If receiver interrupts are enabled, the overrun character and all subsequent characters received, until the error reset command is issued, will generate a special receive condition interrupt request.

Bit D4 - Parity Error

When parity is enabled this bit is set to a "one" for those characters whose parity does not match the programmed sense (even/odd). This bit is latched so that once an error occurs, it remains set until the error reset command (command 6) is issued. If parity is a special receive condition, a parity error will cause a special receive condition interrupt request on the character containing the error on all subsequent characters until the error reset command is issued.

Bits D3, D2, D1 - Residue Codes 2, 1 and 0

In those cases of the SDLC receive mode, where the I-field is not an integral multiple of the character length, these three bits indicate the length of the residual I-field read in the previous bytes. These codes are meaningful only for the transfer in which the end of frame bit is set. This field is set to "000" by a channel or hardware reset and can leave this state only if SDLC mode is selected and a character received.

NOTE I-field bits are right-justified in all cases.

If a receive character length, different from eight bits, is used for the I-field, a table similar to the previous one may be constructed for each different character length. For no residue (that is, the last character boundary coincides with the boundary of the I-field and CRC field) refer to the residue codes shown in Table 3-1 on page 52.

Bit D0 - All Sent

This bit is only active in asynchronous modes; it is always high in synchronous or SDLC modes. This bit is low while the transmitter is sending characters; it will go high only after all the bits of the characters are transmitted and the transmit buffer is empty.

DATARG (Data Register)

The Data Register is actually two separate registers; a write only register that is the transmit buffer and a read only register that is the receiver buffer. The receiver buffer is also the top register of a three register stack called the receive data FIFO. The Data Register is not affected by a channel or hardware reset.

TCREG (Time Constant Register)

This register contains the time constant used by the down counter in the Baud Rate Generator (BRG). The time constant may be changed at any time, but the new value does not take effect until the next time the time constant is loaded into the down counter. It is recommended that the BRG be disabled before writing to this register, as no attempt was made to synchronize the loading of a new time constant with the clock used to drive the BRG. This register is reset to 00 HEX by a channel or by hardware reset.

BRGCTL (Baud Rate Generator Control Register)

This register contains the control bits used to program the BRG and to select the BRG output mode. This register is reset to 00 HEX by a channel or by hardware reset.

Bits D7, D6, D5 and D4

Not used (read as zeros).

Bit D3 - Receiver Clock, Internal/External

This bit determines the direction of the RxC (active low) pin. When this bit is set to a "one", the RxC (active low) pin is the output of the BRG. If this bit is a "zero", the RxC (active low) pin is an input and an external source must supply the receiver clock. The receiver clock is always the signal on the RxC (active low) pin, except in loop mode, when the transmitter clock is connected internally to the receiver clock.

Bit D2 - Transmitter Clock, Internal/External

This bit determines the direction of the TxC (active low) pin. When this bit is set to a "one", the TxC (active low) pin is the output of the BRG. If this bit is a "zero", the TxC (active low) pin is an input and an external source must supply the transmitter clock. The transmit clock is always the signal on the TxC (active low) pin.

Bit D1 - Divide by 64/4

This bit specifies the minimum BRG input clock cycles to output clock cycle. This minimum occurs when the Time Constant Register is loaded with a 01 HEX value. When this bit is set to a "one", 64 input clocks are required for every output clock. When this bit is a "zero", four input clocks are required for every output clock.

Bit D0 - BRG (Baud Rate Generator Enable)

This bit controls the operation of the BRG. When this bit is set to a "one", the BRG will start counting down from the value left in the down counter when this bit was last reset to "zero". If the Time Constant Register is loaded while this bit is reset, the new time constant value is loaded immediately into the down counter. The BRG is disabled from counting when this bit is reset.

VECTRG (Interrupt Vector Register)

This register is used to hold a vector that is passed to the CPU during an interrupt acknowledge cycle. This register can also be accessed through a read/write cycle. If the status affects vector bit in the Interrupt Control Register is disabled, the value programmed into the Vector Register will be passed to the CPU during an interrupt acknowledge cycle or a read cycle. If the status affects vector bit in either channel is enabled, the lower three bits of this register are modified, according to the table listed in the Interrupt Control Register description. With status affects vector ON and no interrupt pending in the SIO, the lower three bits will be read as 011. Only one Vector Register exists in the SIO, but it can be accessed through either channel. This register is reset to 0F HEX by a hardware reset only.

Table 3-1 MK68564 SIO Internal Register Map

	ADDRESS (HEX)	ABBREVIATION	REGISTER NAME	ACCESS
CHANNEL 0 (P3)	01	CMDREG	Command Register	R/W
	03	MODECTL	Mode Control Register	R/W
	05	INTCTL	Interrupt Control Register	R/W
	07	SYNC 1	Sync Word Register 1	R/W
	09	SYNC 2	Sync Word Register 2	R/W
	0B	RCVCTL	Receiver Control Register	R/W
	0D	XMTCTL	Transmitter Control Register	R/W
	0F	STAT 0	Status Register 0	Read Only
	11	STAT 1	Status Register 1	Read Only
	13	DATARG	Data Register	R/W
	15	TCREG	Time Constant Register	R/W
	17	BRGCTL	Baud Rate Generator Control Register	R/W
	19	VECTRG	Vector Register*	R/W
	1B	Not Used		
	1D	Not Used		
	1F	Not Used		
CHANNEL 1 (P4)	21	CMDREG	Command Register	R/W
	23	MODECTL	Mode Control Register	R/W
	25	INTCTL	Interrupt Control Register	R/W
	27	SYNC 1	Sync Word Register 1	R/W
	29	SYNC 2	Sync Word Register 2	R/W
	2B	RCVCTL	Receiver Control Register	R/W
	2D	XMTCTL	Transmitter Control Register	R/W
	2F	STAT 0	Status Register 0	Read Only
	31	STAT 1	Status Register 1	Read Only
	33	DATARG	Data Register	R/W
	35	TCREG	Time Constant Register	R/W
	37	BRGCTL	Baud Rate Generator Control Register	R/W
	39	VECTRG	Vector Register*	R/W
	3B	Not Used		
	3D	Not Used		
	3F	Not Used		

*Only one Vector Register is accessible through either channel.

Table 3-1 MK68564 SIO Internal Register Map (Continued)

	ADDRESS (HEX)	ABBREVIATION	REGISTER NAME	ACCESS
CHANNEL 2 (P5)	41	CMDREG	Command Register	R/W
	43	MODECTL	Mode Control Register	R/W
	45	INTCTL	Interrupt Control Register	R/W
	47	SYNC 1	Sync Word Register 1	R/W
	49	SYNC 2	Sync Word Register 2	R/W
	4B	RCVCTL	Receiver Control Register	R/W
	4D	XMTCTL	Transmitter Control Register	R/W
	4F	STAT 0	Status Register 0	Read Only
	51	STAT 1	Status Register 1	Read Only
	53	DATARG	Data Register	R/W
	55	TCREG	Time Constant Register	R/W
	57	BRGCTL	Baud Rate Generator Control Register	R/W
	59	VECTRG	Vector Register*	R/W
	5B	Not Used		
	5D	Not Used		
	5F	Not Used		
CHANNEL 3 (P6)	61	CMDREG	Command Register	R/W
	63	MODECTL	Mode Control Register	R/W
	65	INTCTL	Interrupt Control Register	R/W
	67	SYNC 1	Sync Word Register 1	R/W
	69	SYNC 2	Sync Word Register 2	R/W
	6B	RCVCTL	Receiver Control Register	R/W
	6D	XMTCTL	Transmitter Control Register	R/W
	6F	STAT 0	Status Register 0	Read Only
	71	STAT 1	Status Register 1	Read Only
	73	DATARG	Data Register	R/W
	75	TCREG	Time Constant Register	R/W
	77	BRGCTL	Baud Rate Generator Control Register	R/W
	79	VECTRG	Vector Register*	R/W
	7B	Not Used		
	7D	Not Used		
	7F	Not Used		
BIM	81	CR0	Not Used	
	83	CR1	Not Used	
	85	CR2	Channels 2, 3	Control Register 2
	87	CR3	Channels 0, 1	Control Register 3
	89	VR0	Not Used	
	8B	VR1	Not Used	
	8D	VR2	Not Used	
	8F	VR3	Not Used	

*Only one Vector Register is accessible through either channel.

NOTE This board contains unused registers which require the address space from $xx00 to $xxFF.

Table 3-2 Register Bit Functions for Channel 0 (P3)

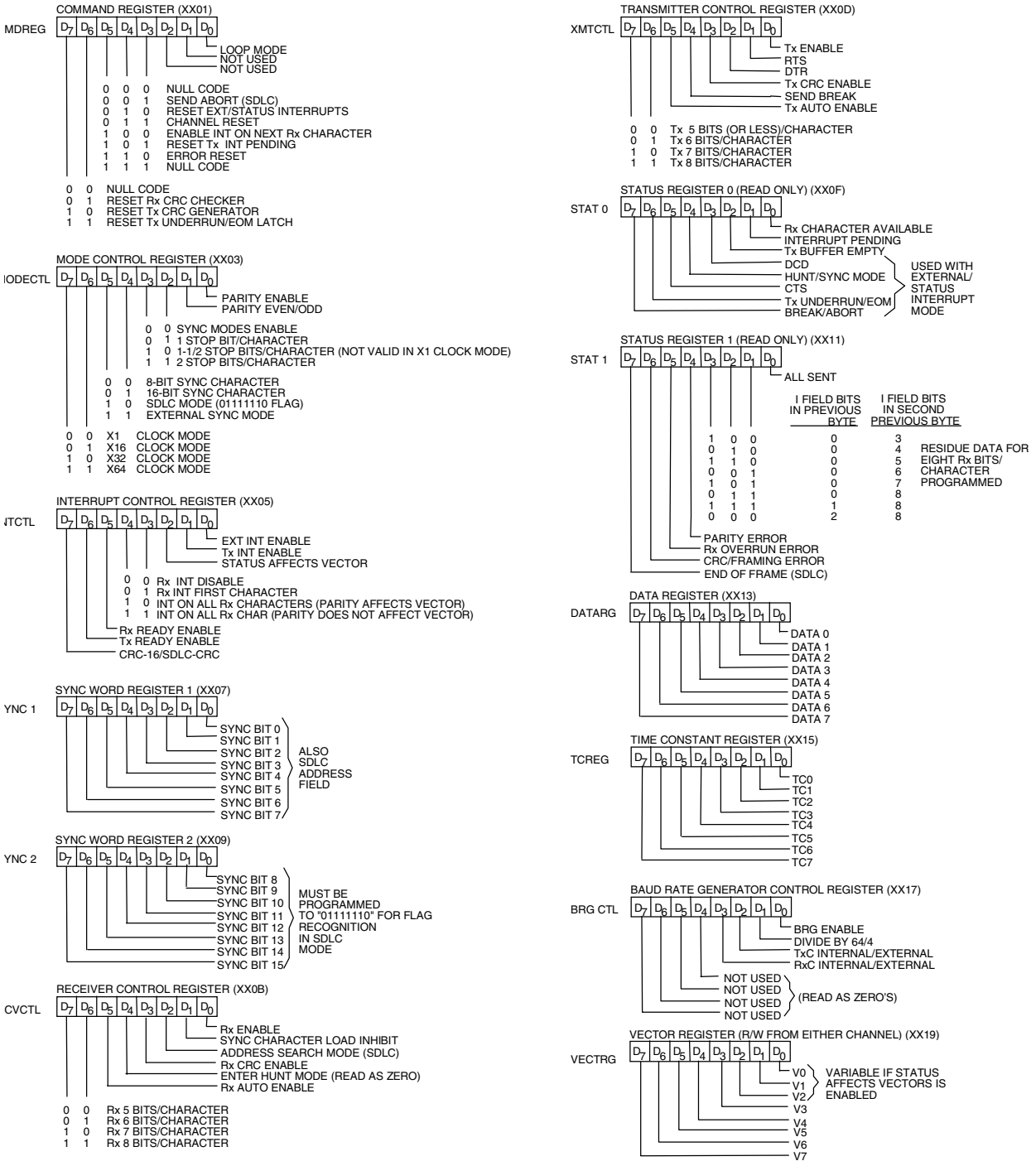

Table 3-3 Register Bit Functions for Channel 1 (P4)

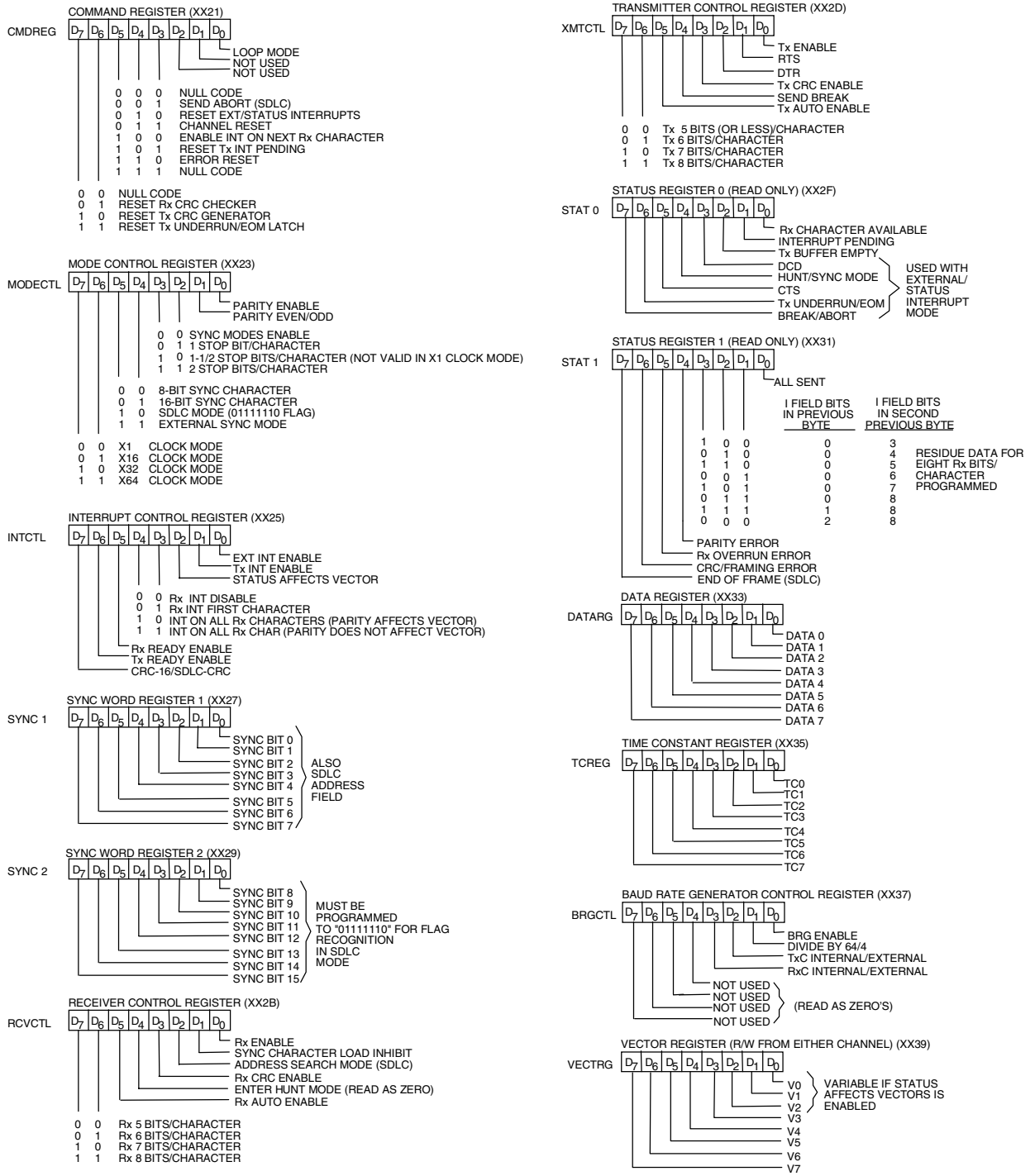

Table 3-4 Register Bit Functions for Channel 2 (P5)

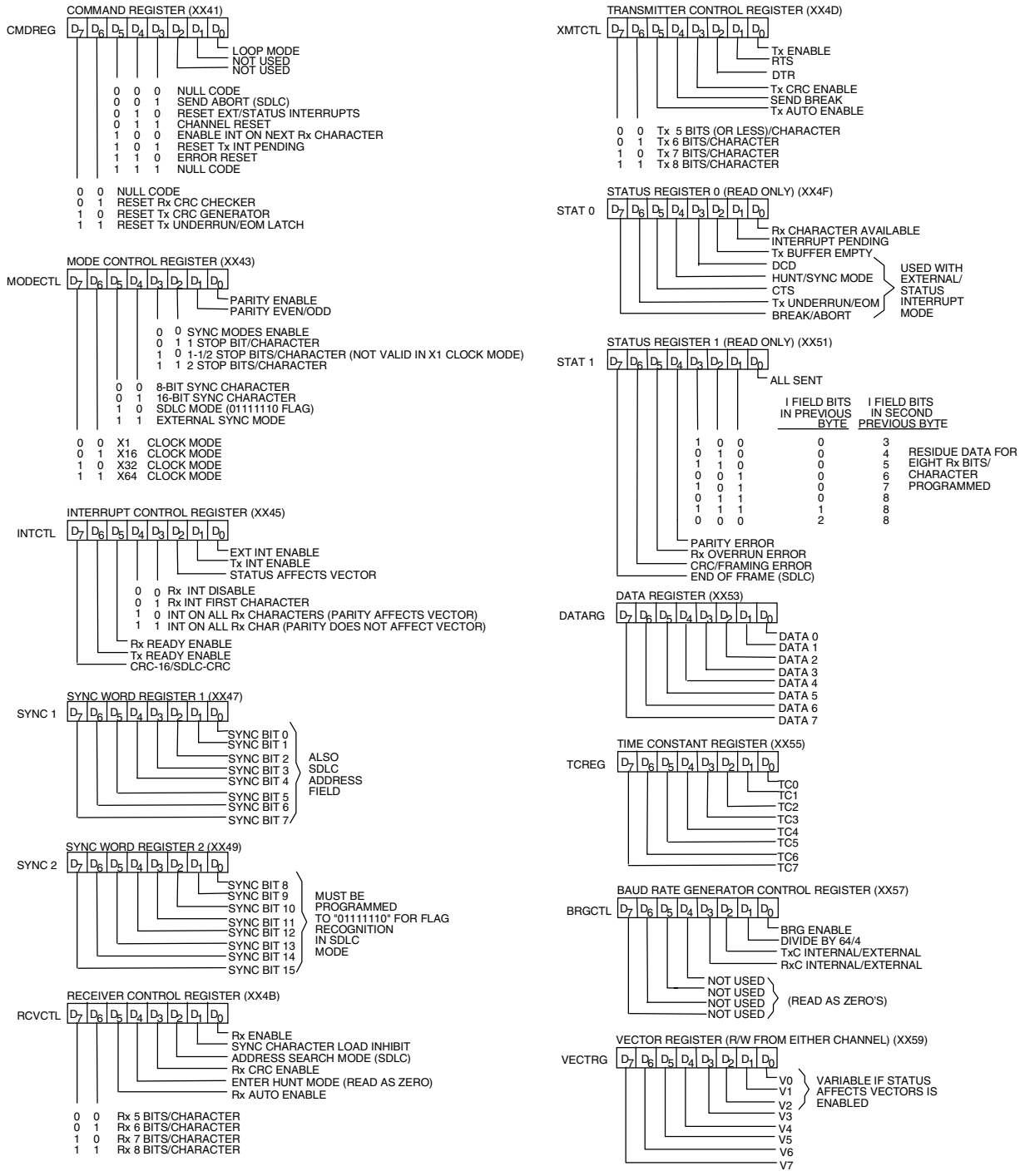

Table 3-5 Register Bit Functions for Channel 3 (P6)

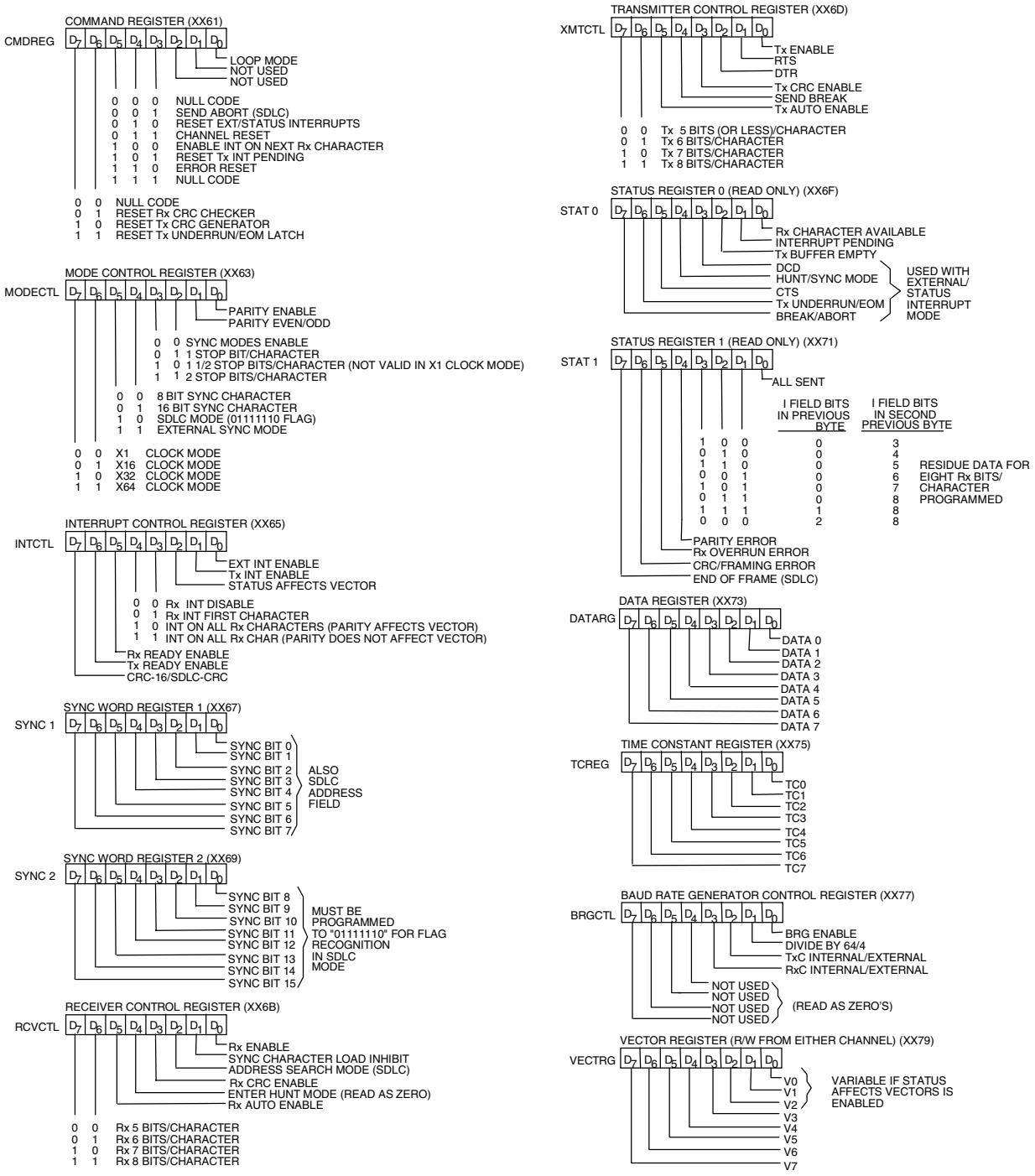

Table 3-6 Address and Register Bit Definitions for the BIM Ei68C153

HEX ADDRESS										
A15-A12	A11-A8	A7-A4	A3-A0							
X	X	8	1	**CONTROL REGISTER 0**							
				IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
				NOT USED							
X	X	8	3	**CONTROL REGISTER 1**							
				IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
				NOT USED							
X	X	8	5	**CONTROL REGISTER 2 (CH 2 AND 3)**							
				IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
				FLAG	FAC	$\overline{X/IN}$	IRE	IRAC	L2	L1	L0
X	X	8	7	**CONTROL REGISTER 3 (CH 0 AND 1)**							
				IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
				FLAG	FAC	$\overline{X/IN}$	IRE	IRAC	L2	L1	L0
X	X	8	9	**VECTOR REGISTER 0**							
				IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
				NOT USED							
X	X	8	B	**VECTOR REGISTER 1**							
				IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
				NOT USED							
X	X	8	D	**VECTOR REGISTER 2**							
				IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
				NOT USED							
X	X	8	F	**VECTOR REGISTER 3**							
				IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
				NOT USED							

Programming the Ei68C153 BIM

The Ei68C153 contains eight programmable read/write registers. There are four Control Registers (CR0 to CR3) that govern operation of this device. The other four (VR0 to VR3) are Vector Registers that contain the vector data used during an interrupt acknowledge cycle. Address and register bit definitions for the BIM Ei68C153 are shown in Table 3-6 on page 58.

Control Registers

There is a Control Register for each interrupt source, i.e., CR2 controls INT2 (0, and 1), CR3 controls INT3. CR0 and CR1 are not used.

Vector Registers

Each interrupt input has its own associated Vector Register. Each register is 8 bits wide and supplies a data byte during its interrupt acknowledge cycle if the associated external/internal (X/IN (active low)) (Bit 05) Control Register bit is clear. This data can be status, identification, or address information depending on system usage. The information is programmed by the system user.

Device reset

When the Ei68C153 is reset, the registers are set to a known condition. The Control Registers are set to all zeros (low). The Vector Registers are set to $0F. This value is the MC68000 vector for an uninitialized interrupt vector.

Control Register 0

Not used.

Control Register 1

Not used.

Control Register 2 and 3

The bits for Control Register 2 and 3 are as follows:

Bit 07 (Flag 7)

Bit 7 is a flag that can be used in conjunction with the test and set instruction of the MC68000. It can be changed without affecting chip operation and is useful for processor-to-processor communication and resource allocation.

Bit 06 - (FAC - Auto Clear)

If Bit 6 is set, the flag bit is automatically cleared during an interrupt acknowledge cycle.

Bit 05 - (X/IN - External/Internal)

Bit 5 of the Control Register determines the response of the Ei68C153 during an interrupt acknowledge cycle. If the X/IN (active low) bit is clear (low level) the BIM will respond with vector data and a DTACK (active low) signal, i.e., an internal response. If X/IN (active low) is set, the vector is not supplied and no DTACK (active low) is given by the BIM, i.e., an external device should respond.

Bit 04 - (IRE - Interrupt Enable)

This field Bit 4 must be set (high level) to enable the bus interrupt request associated with the Control Register. Thus, if the INTX (active low) line is asserted and IRE is cleared, no interrupt request (IRQX) active low will be asserted.

Bit 03 - (IRAC - Interrupt Auto-Clear)

If the Bit 3 is set, Bit 4 is cleared during an interrupt acknowledge cycle responding to this request. This action of clearing Bit 4 disables the interrupt request. To re-enable the interrupt associated with this register, Bit 4 must be set again by writing to the Control Register.

Bits 02, 01 and 00 - (L2, L1, L0 - Interrupt Level)

The least significant 3-bit field of the register determines the level at which an interrupt will be generated:

L2	L1	L0	IRQ Level
0	0	0	DISABLED
0	0	1	IRQ1
0	1	0	IRQ2

A value of "zero" in the field disables the interrupt.

Vector Registers 0 Through 3

Not used.

Baud Rate Selection and Programming

Each channel contains a programmable BRG. Each BRG consists of an 8-bit Time Constant Register (TCR), an 8-bit down counter, a Control Register and a flip-flop on the output to provide a square wave signal out. Because of an input flip-flop, the maximum output of the BRG is one-fourth the input clock frequency. Maximum frequency occurs when the divide-by-four mode is selected and the TCR is loaded with the minimum count of "01" HEX. The BRG can be programmed to drive the transmitter (TxC), the receiver (RxC), both (BRG output TxC and RxC), or neither (TxC and RxC are inputs).

The BRG should be disabled before the CPU writes to the TCR. See Table 3-2 on page 54 and Table 3-5 on page 57 for the register bit functions of the BRG and Table 3-7 on page 62 and Table 3-8 on page 64 for the baud rate selection information.

Baud Rate Programming

Table 3-7 and Table 3-8 show the correct programming of the clock mode bits, divide by 64/4-bit and the TCR for the desired data rate. For example, for a baud rate of 9,600, the divide by 64/4-bit would be set to "zero" (divide by 4 chosen); a value of $80 HEX would be loaded into the TCR ($80 HEX = 128 dec.); and Bits 7 and 6 in the Command Register would be set to "zero" (X1 clock mode). For the 4.9152 MHz clock, osc jumper pins 1 and 2 should be jumpered. For a 4 MHz clock, osc jumper pins 2 and 3 should be jumpered.

Table 3-7 4.9152 MHz Clock

RATE	DIV*	TIME CONSTANT IN DECIMAL	CLOCK MODE	ACTUAL	%ERROR
76.8 k	4	16	X1	76.8 k	
	4	1	X16	76.8 k	
38.4 k	4	32	X1	38.4 k	
	4	2	X16	38.4 k	
	4	1	X32	38.4 k	
19.2 k	4	64	X1	19.2 k	
	64	4	X1	19.2 k	
	4	4	X16	19.2 k	
	4	2	X32	19.2 k	
	4	1	X64	19.2 k	
9600	4	128	X1	9600	
	64	8	X1	9600	
	4	8	X16	9600	
	4	4	X32	9600	
	4	2	X64	9600	
7200	4	170	X1	7228	.39%
4800	4	0	X1	4800	
	64	16	X1	4800	
	4	16	X16	4800	
	64	1	X16	4800	
	4	8	X32	4800	
	4	4	X64	4800	
3600	64	21	X1	3657	1.6%
	4	21	X16	3657	1.6%
2400	64	32	X1	2400	
	6	32	X16	2400	
	64	2	X16	2400	
	6	16	X32	2400	
	64	1	X32	2400	
	4	8	X64	2400	

*DIV represents the condition of the divide by 64/4 pin in the BRG Control Register.

Table 3-7 4.9152 MHz Clock (Continued)

RATE	DIV*	TIME CONSTANT IN DECIMAL	CLOCK MODE	ACTUAL	%ERROR
2000	64	38	X1	2021	1.1
	4	38	X16	2021	1.1
1800	64	43	X1	1786	.78
	4	43	X16	1786	.78
1200	64	64	X1	1200	
	4	64	X16	1200	
	64	4	X16	1200	
	4	32	X32	1200	
	64	2	X32	1200	
	4	16	X64	1200	
	64	1	X64	1200	
600	64	128	X1	600	
	4	128	X16	600	
	64	8	X16	600	
	4	64	X32	600	
	64	4	X32	600	
	4	32	X64	600	
	64	2	X64	600	
300	64	0	X1		
	4	0	X16	300	
	64	16	X16	300	
	4	128	X32	300	
	64	8	X32	300	
	4	64	X64	300	
	64	4	X64	300	
110	64	44	X16	109	.83
	64	22	X32	109	.83
	64	11	X64	109	.83
	4	176	X64	109	.83

*DIV represents the condition of the divide by 64/4 pin in the BRG Control Register.

Table 3-8 4.0 MHz Clock

RATE	DIV*	TIME CONSTANT IN DECIMAL	CLOCK MODE
1 M	4	1	X1
500 k	4	2	X1
333 k	4	3	X1
250 k	4	4	X1
200 k	4	5	X1
167 k	4	6	X1
143 k	4	7	X1
125 k	4	8	X1
111 k	4	9	X1
100 k	4	10	X1
62.5 k	4	16	X1
50 k	4	20	X1
33 k	4	30	X1
25 k	4	40	X1

*DIV represents the condition of the divide by 64/4 pin in the BRG Control Register.

Bus Interrupter Programming

The VMIVME-6015 SIO Board is designed with one Ei68C153 BIM that interfaces with the MK68564 integrated circuits to provide all interrupt logic necessary to support the interrupt modes of MK68564 SIO operation. The VMIVME-6015 uses two of the four channels available on the Ei68C153. Channel 3 of the BIM is used by the MK68564 SIO Channels 0 and 1, and Channel 2 of the BIM is used by the MK68564 SIO Channels 2 and 3. The BIM Control Registers must be programmed for external vectors because the MK68564 SIO integrated circuits generate interrupt vectors within the MK68564.

CHAPTER
4

Configuration and Installation

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RS-485 Token Passing Network Connections 87

Unpacking Procedures

CAUTION Some of the components assembled on VMIC'S products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. Unused boards should be stored in the same protective boxes in which they were shipped. When the board is to be laid on a bench for configuring, etc., it is suggested that conductive material be inserted under the board to provide a conductive shunt.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning disposition of the damaged item(s).

Physical Installation

CAUTION Do not install or remove boards while power is applied.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

Address Modifiers

The VMIVME-6015 is configured at the factory to respond to short supervisory I/O access. This configuration can be changed by installing jumper AM which enables the board to respond to short nonprivileged I/O access.

The address Dual-in-Line Package (DIP) switch and its use in the addressing scheme is shown in Figure 4-1. A base address of $FF00 (HEX) is shown as a typical selection.

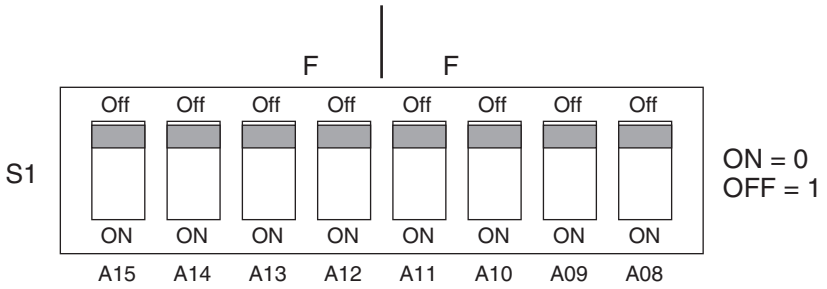


Figure 4-1 Board Address Selection

Cable Shield Grounding

The cable shield can be connected to chassis ground or it can be connected to pin 1 of the user connectors. If the cable shield is connected to pin 1, then the user has the option of installing the GND jumper to connect it directly to the board ground. If the GND jumper is not installed, then pin 1 is returned to ground through a 100Ω resistor, thus avoiding excessive ground currents.

Peripheral I/O Interface Configuration

Each of the channels can be independently configured for serial line signal compatibility with EIA RS-232, RS-422, RS-423 or RS-485. Terminating resistors, an RS-232 pull-up resistor and jumper pins are provided to allow the user to configure I/O signal conditioning options as required. Configuration details are provided in Figure 4-2 on page 74 through Figure 4-11 on page 83. Address switch and jumper locations are shown in Figure 4-12 on page 84.

Factory Configuration

The four channels on the VMIVME-6015 are configured at the factory and shipped as shown on the jumper and switch location diagram (Figure 4-12 on page 84). The jumpers provide the following configuration:

RS-232

Jumpers G0 through G3 are jumpered 1 to 2; Jumpers F0 through F1 are jumpered 2 to 3. This jumper configuration allows for RS-232 transmission.

Transmit and receive (TXD, RXD)

Jumpers B0 and B1 are configured as DTEs (see Figure 4-2 on page 74). Jumpers B2 and B3 are configured as DCEs (see Figure 4-4 on page 76).

Transmit and receive secondary (STXC, SRXD)

Jumpers A0 and A3 are configured as DTEs (see Figure 4-8 on page 80). Jumpers A1 and A2 are configured as DCEs (see Figure 4-7 on page 79). Jumper field Ax is provided for RS-422A, RS-423 or RS-485 transmission. Jumper Ax has no effect on RS-232 transmission. For RS-422A, RS-423 or RS-485, move Jumper Gx from 1 to 2 to 2 to 3 and move Jumper Fx from 2 to 3 to 1 to 2.

Request-to-send, clear-to-send (RTS, CTS)

Jumpers C0 and C1 are configured as DTEs (see Figure 4-2 on page 74). Jumpers C2 and C3 are configured for DCEs (see Figure 4-4 on page 76).

Transmit clock, receive clock (TXC, RXC)

Jumpers D0 and D1 are configured as DTEs (see Figure 4-5 on page 77). Jumpers D2 and D3 are configured for DCEs (see Figure 4-4 on page 76).

Clock driving

The board is configured with Hx 2 and Hx 3 installed. Hx 2 installed drives the internal TXC signal out to the connector (see Figure 4-5 on page 77). Hx 3 installed routes an external clock signal to the internal RXC (see Figure 4-4 on page 76). With Hx 2 installed, Hx 1 must be removed. With Hx 3 installed, Hx 4 must be removed.

Data terminal ready, Data carrier detect (DTR, DCD)

Jumpers E0 and E1 are configured as DCEs driving RI. Jumpers E2 and E3 are configured as DTEs receiving RI (see Figure 4-3 on page 75).

Remove resistors R1 through R6 and R8 through R13 for RS-232 operation. These resistors are installed on the board so that they are available for RS-422 and RS-485 configurations.

RS-232C Configuration

The RS-232C is the recommended standard where flat cable is used for the transmission of control signals and/or digital data. The maximum physical length is normally identified as 50 feet for RS-232C communication and no termination resistors are needed.

Jumpers and resistors should be installed as shown in Figure 4-2 on page 74 through Figure 4-6 on page 78. The jumper configuration selected will depend on whether the equipment must be configured for DCE or DTE and whether the equipment will need to drive or receive the DCD and clock signals.

RS-422 Configuration

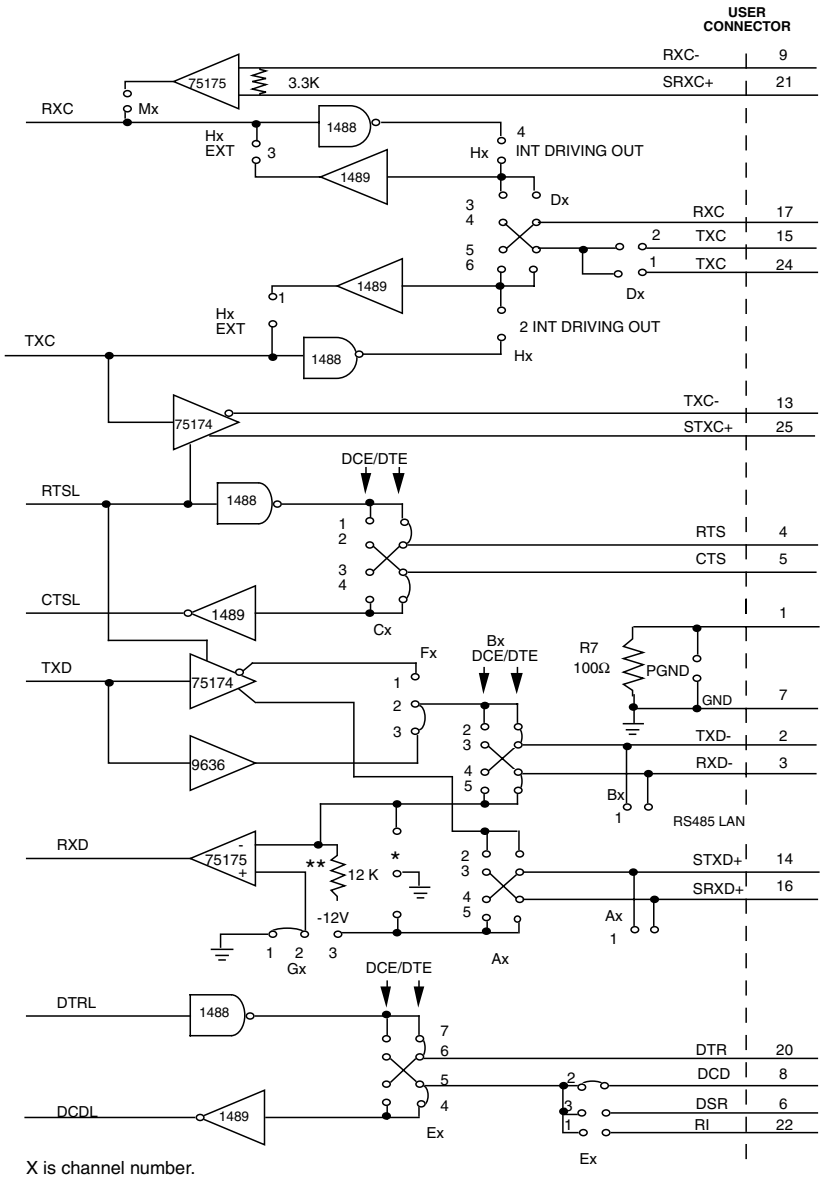
RS-422 is not an actual formal part of the EIA recommended standard. The maximum permissible length of cable separating the generator and load is a function of the data signaling rate and is influenced by the tolerable signal distortion. As the data signaling rate is reduced below 90 kbit/s, the cable length is limited to 4,000 feet, assuming a maximum allowable 6 dB signal loss. The VMIVME-6015 should be configured as shown for the RS-422 (Figure 4-7 on page 79 and Figure 4-8 on page 80). A 100Ω terminating resistor must be installed and the 12 K RS-232 pull-up resistor must be removed. This is shown in Figure 4-7 and Figure 4-8 for each channel being operated as RS-422.

RS-423 Configuration

RS-423 should be configured the same way as RS-422.

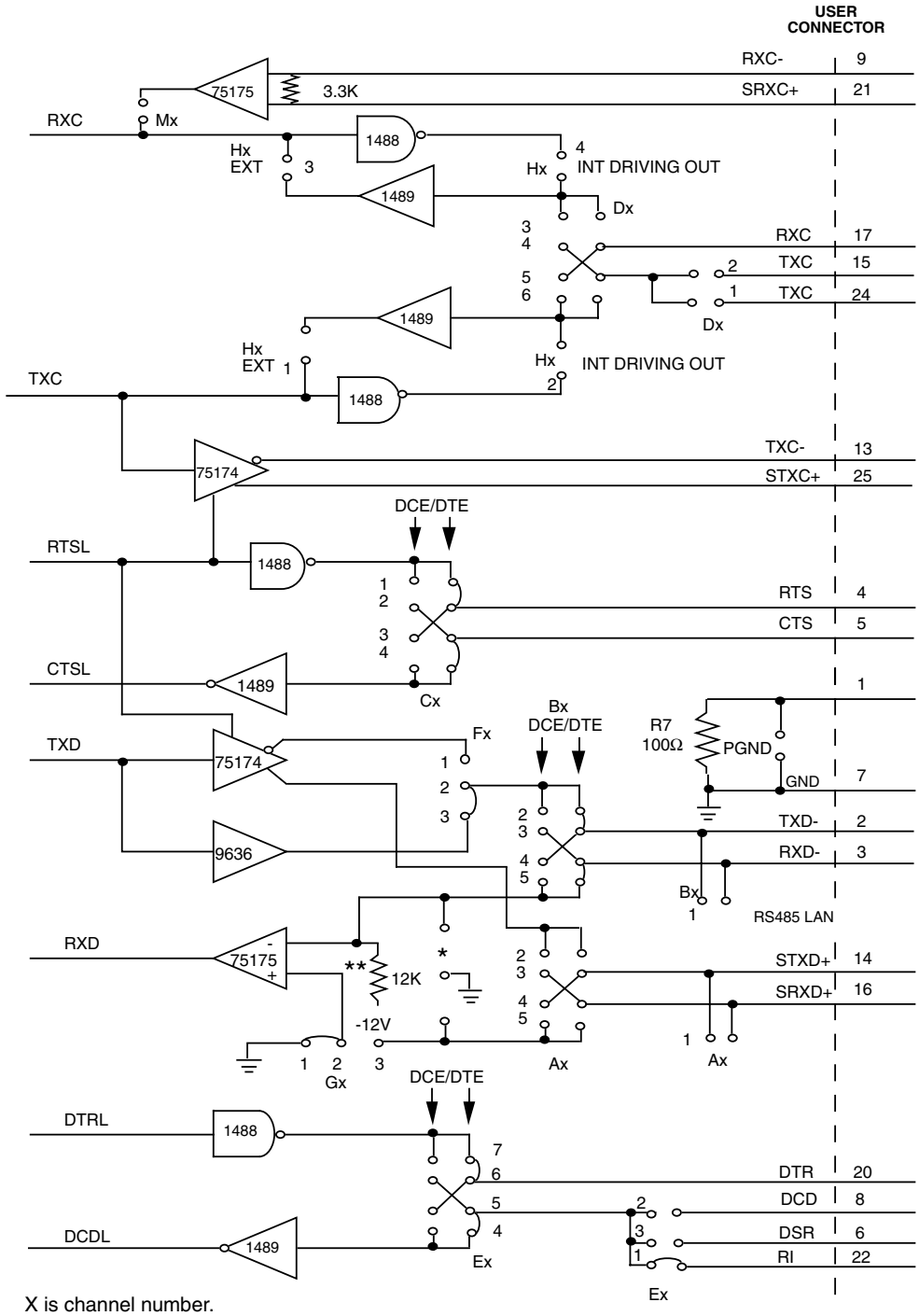
RS-485 Configuration

RS-485 is an EIA recommended standard. It allows for 32 drivable unit loads, plus two termination resistances of 60Ω each. The RS-232 pull-up resistor should be removed and the VMIVME-6015 should be configured as shown in Figure 4-9 on page 81, Figure 4-10 on page 82 and Figure 4-11 on page 83. A LAN configuration passing network is shown in Figure 4-13 on page 87.



X is channel number.
*Terminating resistors R1 through R6 and R8 through R13 should be removed.
**Install RS232 pull-up. R32= Channel 0, R31 = Channel 1, R21 = Channel 2, R20 = Channel 3.

Figure 4-2 VMIVME-6015 Configured for RS-232 ASYNC DTE Receiving DCD

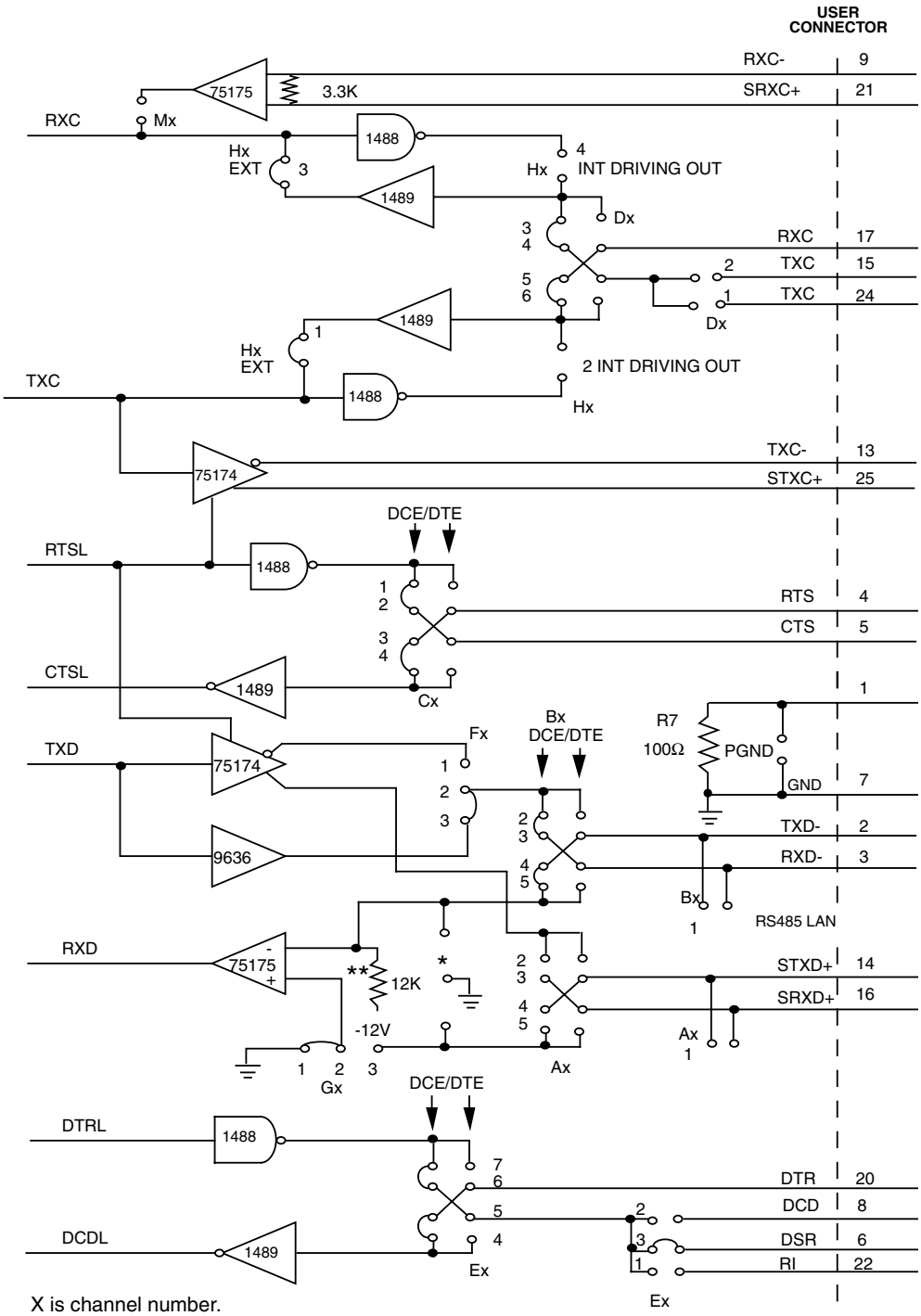


X is channel number.

*Terminating resistors R1 through R6 and R8 through R13 should be removed.

**Install RS232 pull-up. R32= Channel 0, R31 = Channel 1, R21 = Channel 2, R20 = Channel 3.

Figure 4-3 VMIVME-6015 Configured for RS-232 ASYNC DTE Receiving RI

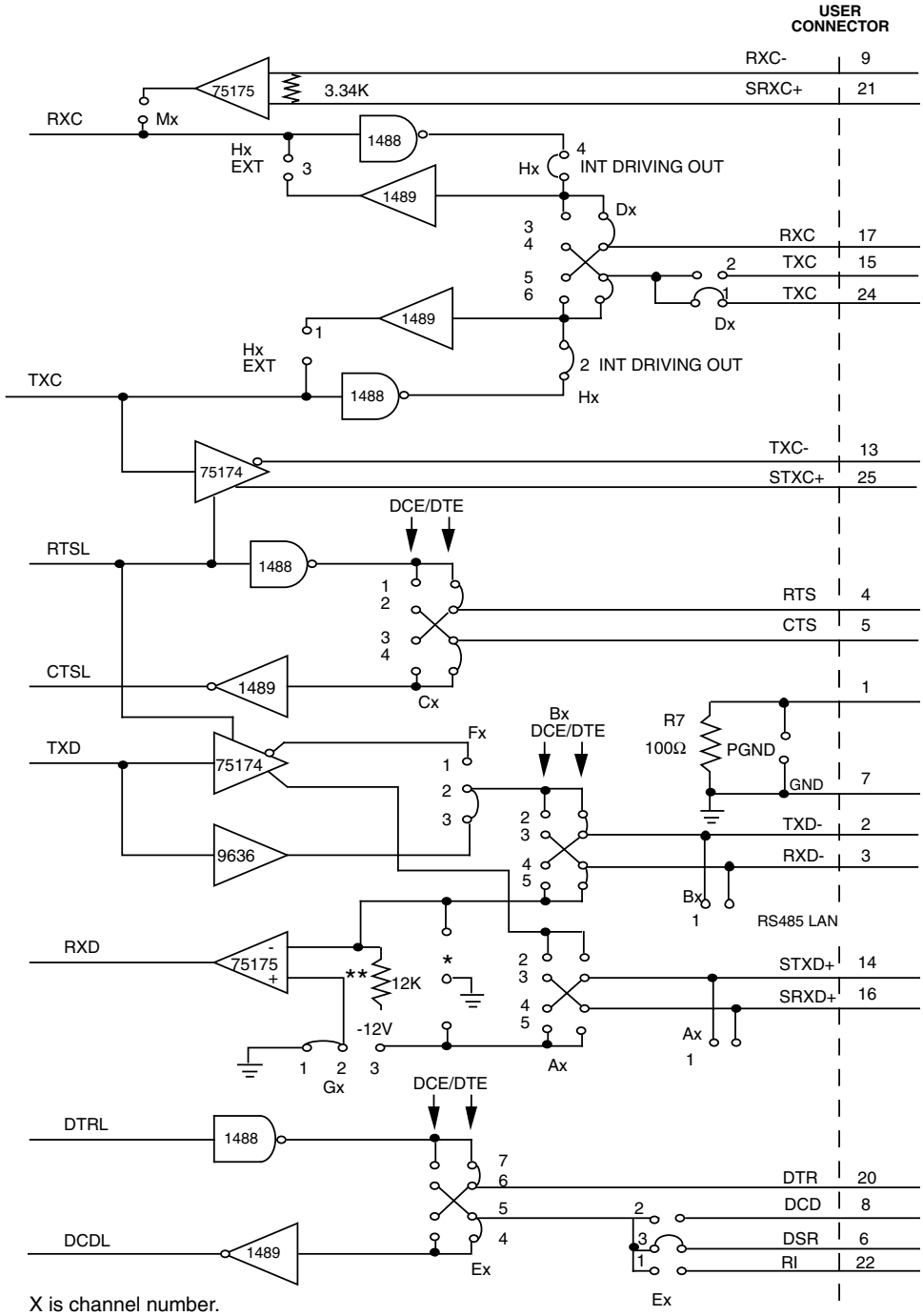


X is channel number.

*Terminating resistors R1 through R6 and R8 through R13 should be removed.

**Install RS232 pull-up. R32= Channel 0, R31 = Channel 1, R21 = Channel 2, R20 = Channel 3.

Figure 4-4 VMIVME-6015 Configured for RS-232 SYNC DCE Receiving External Clock

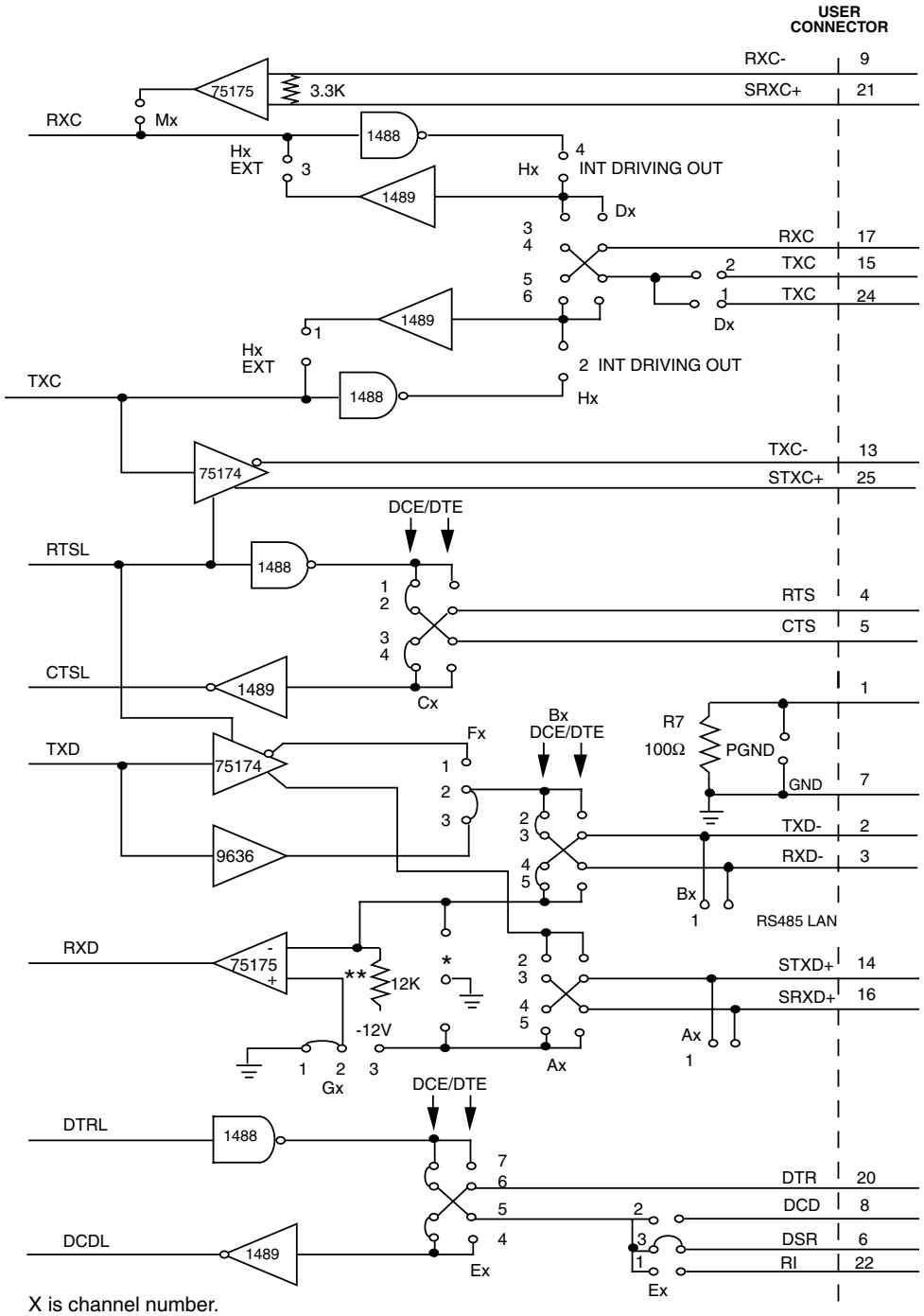


X is channel number.

*Terminating resistors R1 through R6 and R8 through R13 should be removed.

**Install RS232 pull-up. R32= Channel 0, R31 = Channel 1, R21 = Channel 2, R20 = Channel 3.

Figure 4-5 VMIVME-6015 Configured for RS-232 SYNC DTE Driving Clock

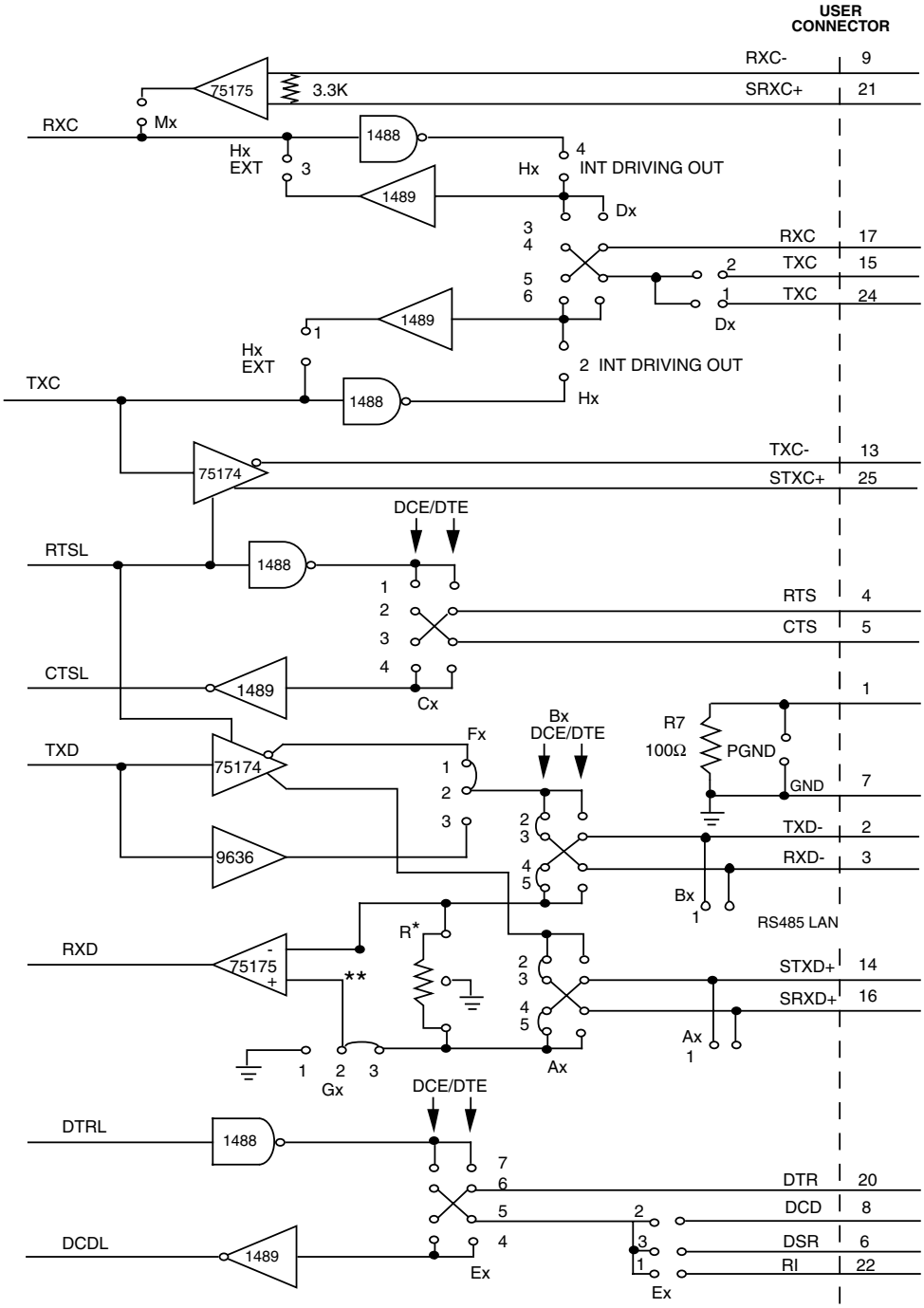


X is channel number.

*Terminating resistors R1 through R6 and R8 through R13 should be removed.

**Install RS232 pull-up. R32= Channel 0, R31 = Channel 1, R21 = Channel 2, R20 = Channel 3.

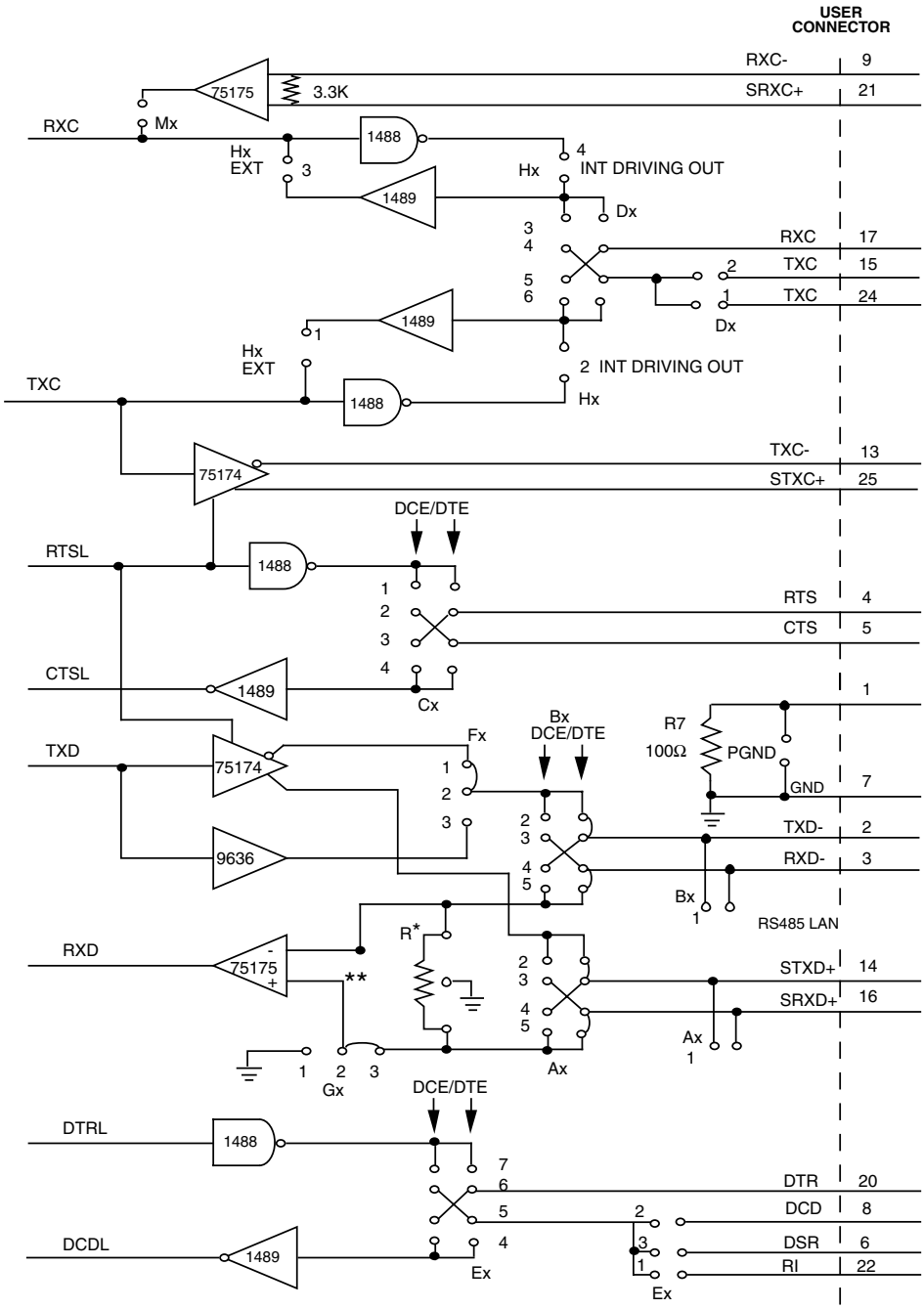
Figure 4-6 VMIVME-6015 Configured for RS-232 ASYNC DCE Driving DSR



X is channel number.
*R is R12 for CH0, R9 for CH1, R5 for CH2, and R2 for CH3. Terminating resistors R1, R3, R4, R6, R8, R10, R11, and R13 should be removed.

**Remove RS232 pull-up R32, R31, R21, and R20.

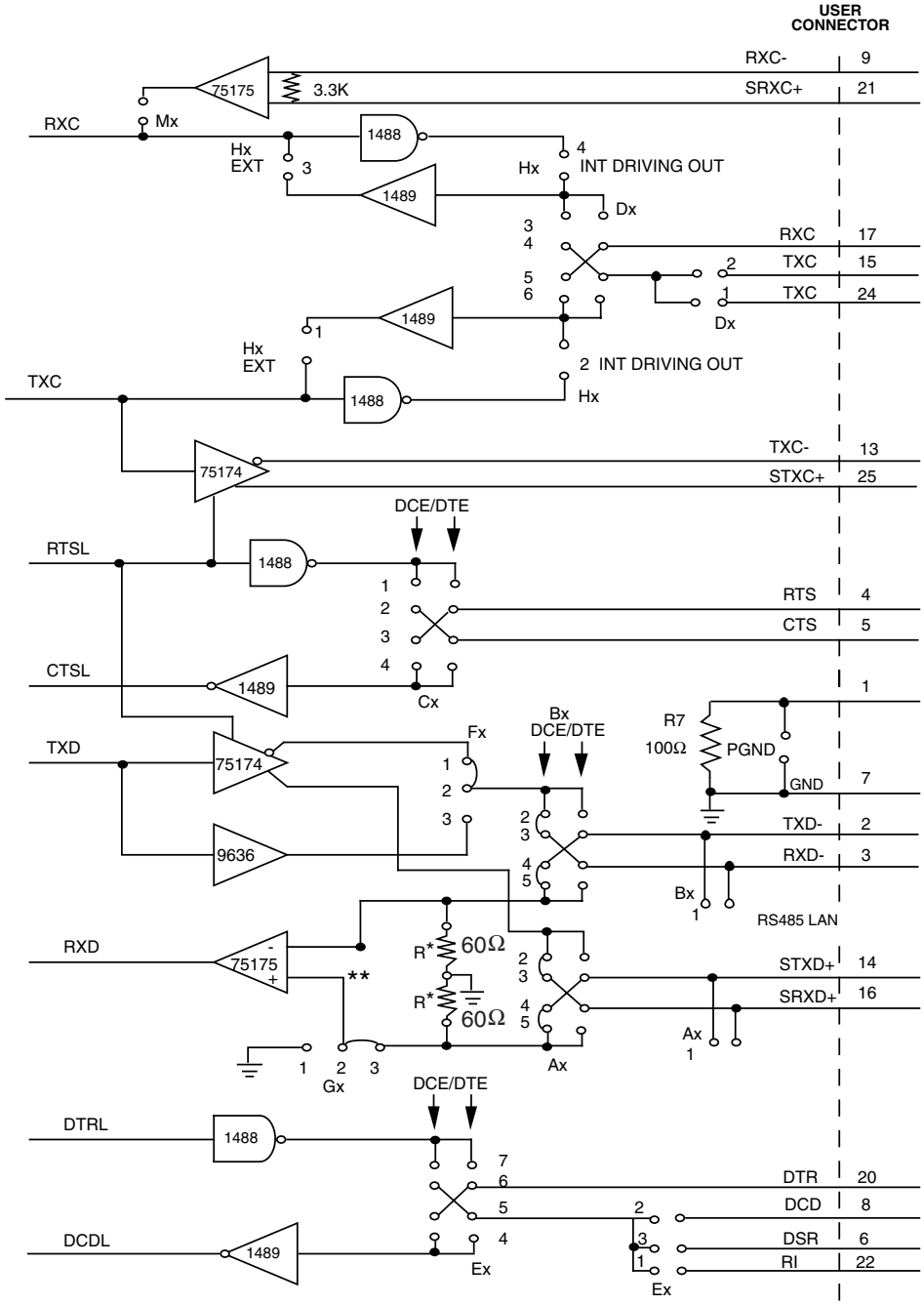
Figure 4-7 VMIVME-6015 Configured for RS-422A DCE



X is channel number.
*R is R12 for CH0, R9 for CH1, R5 for CH2, and R2 for CH3. Terminating resistors R1, R3, R4, R6, R8, R10, R11, and R13 should be removed.

**Remove RS232 pull-up R32, R31, R21, and R20.

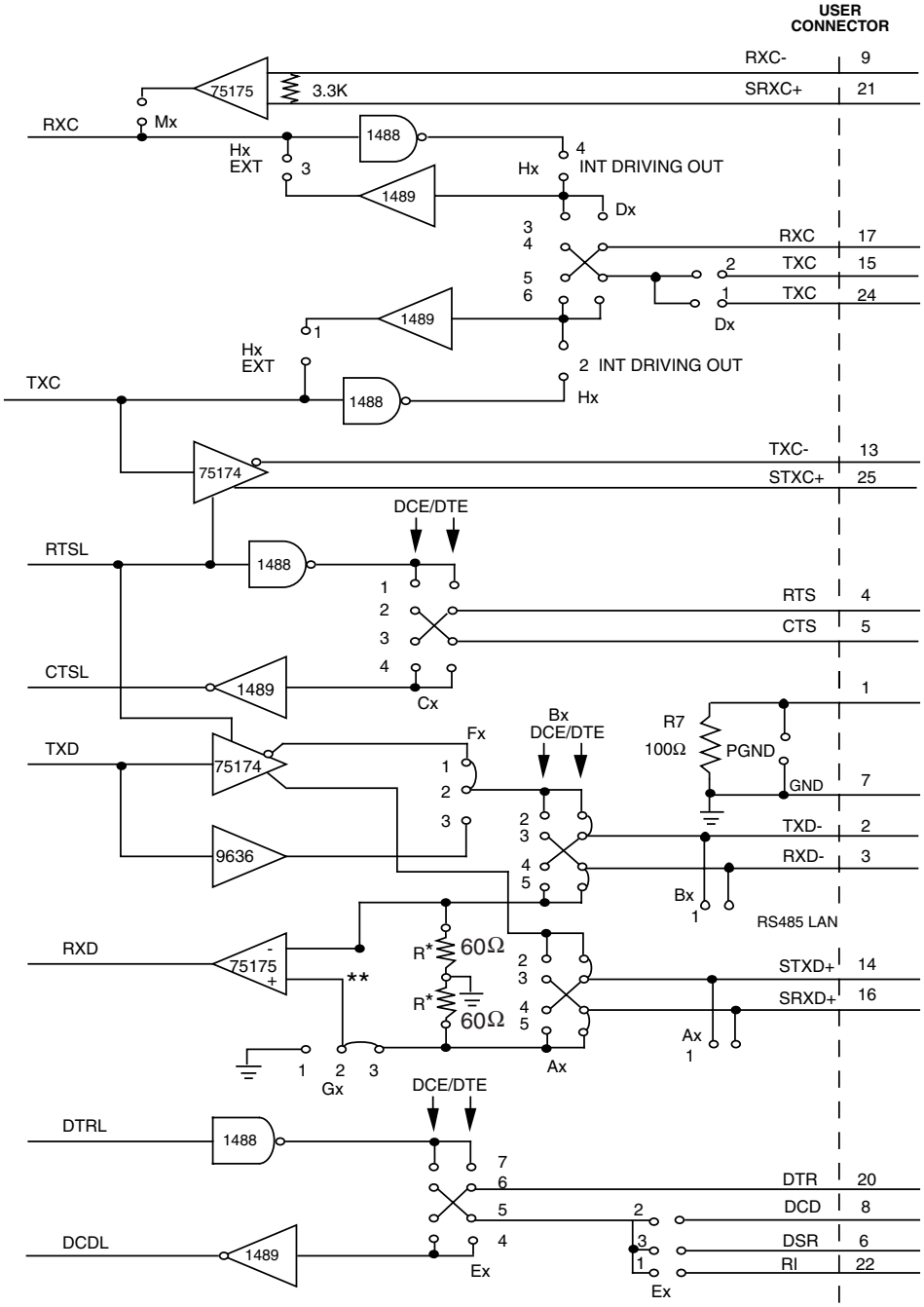
Figure 4-8 VMIVME-6015 Configured for RS-422A DTE



X is channel number.
*R represents the 60Ω pair R13; R11 for CH0, R8, R10 for CH1, R6, R4 for CH2, and R1, R3 for CH3. Remove terminating resistors R2, R5, R9 and R12.

**Remove RS232 pull-up R32, R31, R21, and R20.

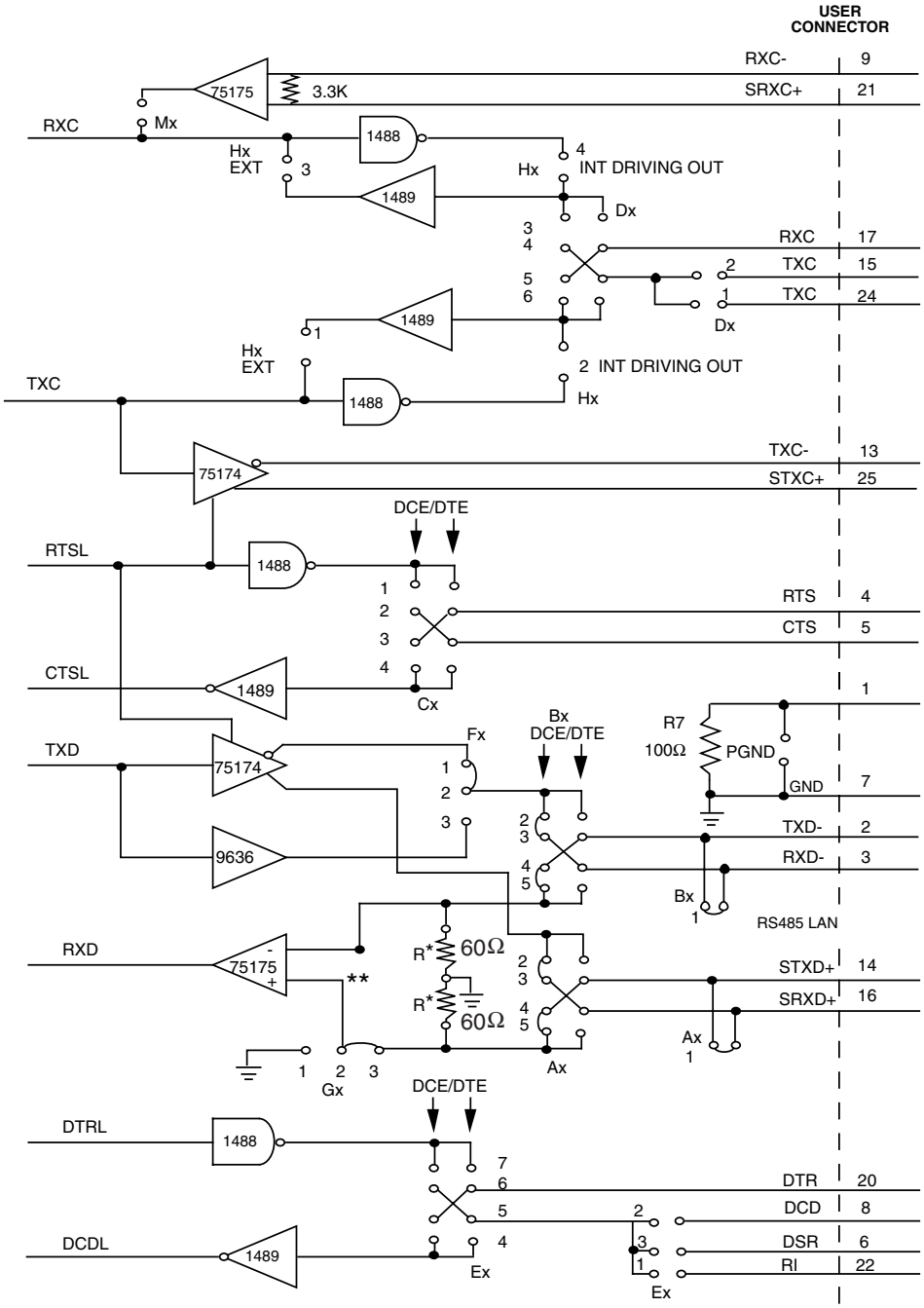
Figure 4-9 VMIVME-6015 Configured for RS-485 DCE



X is channel number.
*R represents the 60Ω pair R13; R11 for CH0, R8, R10 for CH1, R6, R4 for CH2, and R1, R3 for CH3. Remove terminating resistors R2, R5, R9 and R12.

**Remove RS232 pull-up R32, R31, R21, and R20.

Figure 4-10 VMIVME-6015 Configured for RS-485-DTE



X is channel number.
*R represents the 60Ω pair R13; R11 for CH0, R8, R10 for CH1, R6, R4 for CH2, and R1, R3 for CH3. Remove terminating resistors R2, R5, R9 and R12.

**Remove RS232 pull-up R32, R31, R21, and R20.

Figure 4-11 VMIVME-6015 Configured for RS-485 LAN

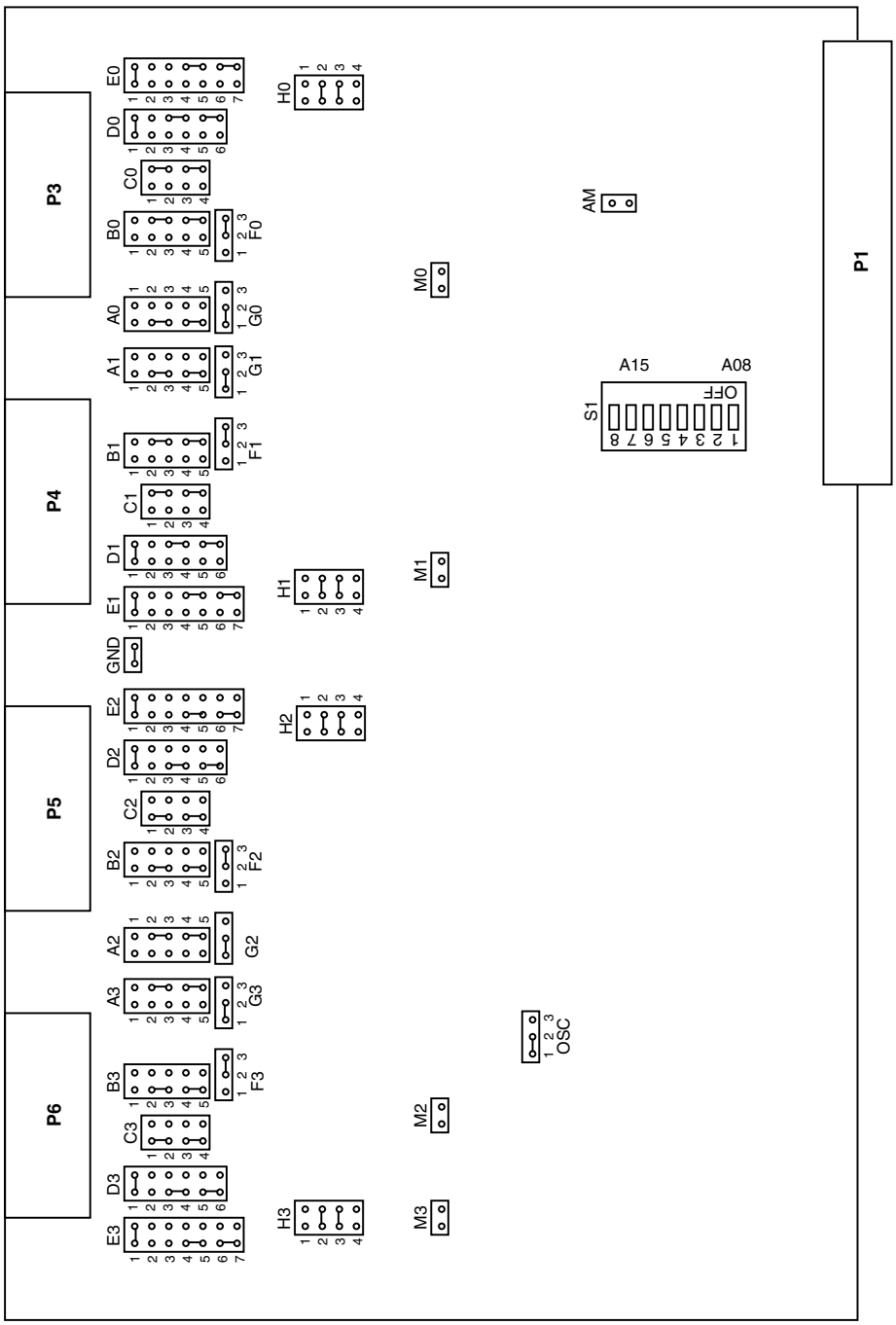


Figure 4-12 Switch and Jumper Locations (Factory Configuration Jumpers Shown)

Compatible Cable Connector

A compatible cable connector for the VMIVME-6015 is the AMP 747322-2 connector, strain relief kit (Type D). The part number of the header connector soldered to the PC board is AMP 206584-1.

Flat cable can be used for the RS-232 interface type. However, for other interface types the cable should be selected based on cable length and baud rate. Termination resistors should also be installed as shown in Figure 4-7 on page 79 through Figure 4-10 on page 82.

I/O Connector Pin Assignments

Serial I/O front panel connector pin assignments are shown in Table 4-1.

Table 4-1 Connector Signal Definitions for P3, P4, P5 and P6

PIN NO.	DESCRIPTION	MNEMONIC
1	Protective Ground	PGND
2	Transmit Data	TxD
3	Receive Data	RxD
4	Request to Send	RTS
5	Clear to Send	CTS
6	Data Set Ready	DSR
7	Signal Ground	GND
8	Data Carrier Detect	DCD
9	Mbit Clock Receiver	RXC
10	Not Used	
11	Not Used	
12	Not Used	
13	Mbit Clock Transmit	TXC
14	Secondary Transmit Data	STxD
15	Transmit Clock	TxC
16	Secondary Receive Data	SRxD
17	Receive Clock	RxC
18	Not Used	
19	Not Used	
20	Data Terminal Ready	DTR
21	Secondary Receive Clock	SRXC
22	Ring Indicator	RI
23	Not Used	
24	Transmit Clock (Alternate)	TxCA
25	Secondary Transmit Clock	STXC

RS-485 Token Passing Network Connections

The VMIVME-6015 may be configured in a low cost, token passing, network configuration as described in Section 3. The user must connect the on-board terminator resistor at the ends of the network, as shown in Figure 4-13.

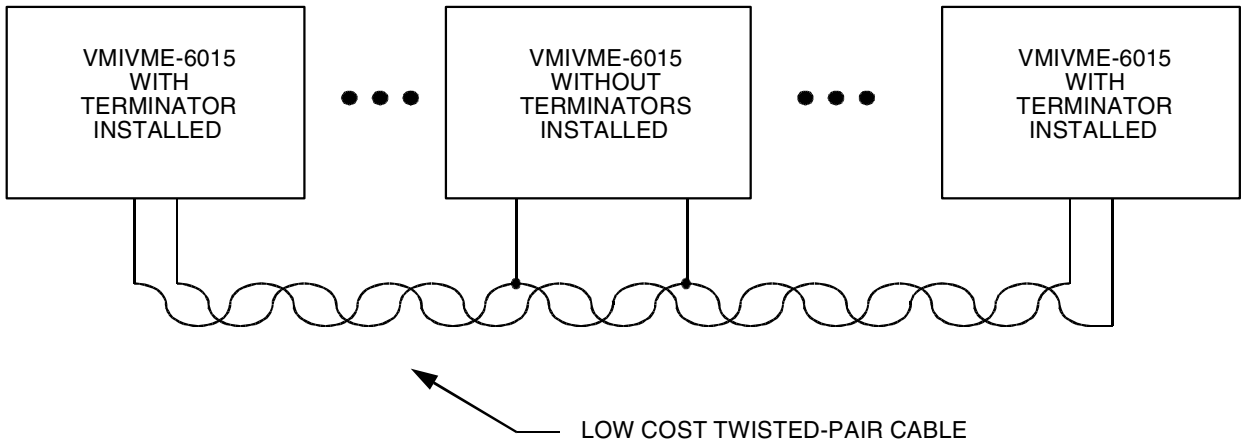


Figure 4-13 Token Passing Network System Configuration

Configurations for RS-485 are discussed in "Peripheral I/O Interface Configuration" on page 72. Termination resistors are socketed and must be installed by the user. For RS-485, the resistors are provided.

CHAPTER

5

Maintenance

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Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If the product must be returned, contact VMIC for a Return Material Authorization (RMA) Number. This RMA Number must be obtained prior to any return.

Maintenance Prints

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.