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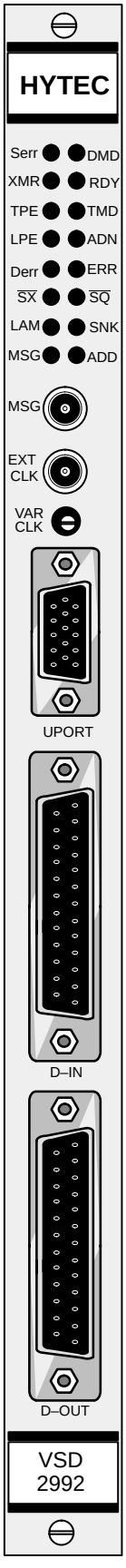

USER MANUAL

HYTEC VME/CAMAC SERIAL HIGHWAY DRIVER Type VSD 2992

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VSD2992/UTM/G/X/2.0

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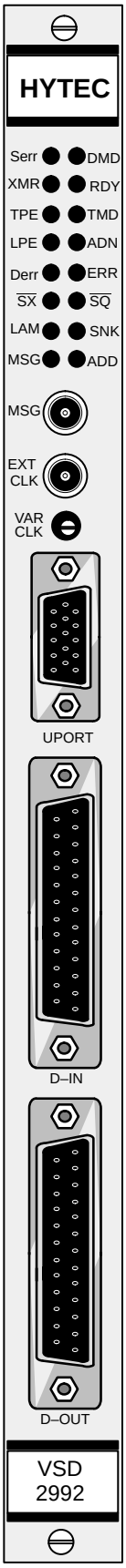
1.0 Product Summary



VME Serial Highway Driver Type VSD2992

Features

- *Operates as a VME Slave module A16/D16 D08(E0).*
- *Operates as a VME ROAK D08 Interrupter.*
- *Overall Interrupt Enable Bit.*
- *Interrupt Selectable 1–7 by Jumper.*
- *Vector Writable and Readable.*
- *Complies with CAMAC specification EUR6100E and I.E.E.E. 595.*
- *Bit Serial and Byte Serial Modes at up to 5MHz.*
- *Internal Crystal Controlled or Variable Clock source, or external clock input with comprehensive dividing network on selected source.*
- *Separate Reply Buffer.*
- *64 Word FIFO Demand Buffer.*
- *Lost Sync Indicator.*
- *12 Bit Maskable LAM Register with front panel display.*
- *Repeat Read Mode.*
- *Q–Scan Mode.*
- *Reply Timeout.*
- *Echo Mode.*
- *Readout of transmitted message.*
- *64 'Byte' Test Message Generator with facilities for forcing errors.*
- *Module Booking mechanism for multi–master working.*
- *Dump Store for message analysis.*
- *Drive for Hytec U–Port Adaptor.*
- *Readout of U–Port Setting & Main/Backup Loop States.*

Product Description

The Hytec VSD2992 is a single width 6U VME Module which transmits and receives signals on the CAMAC serial highway whilst being controlled via the VME BUS. Bit serial and Byte serial ports for data and clock are provided for the transmission of command and the acceptance of reply and demand messages. Serial messages are initiated by loading command and data registers via the VME bus using either D16 or DØ8(E0) mode. Incoming messages are checked for transverse and longitudinal parity. The serial clock can be controlled by a crystal source, variable frequency oscillator or an external source. The internal oscillators may be divided down from the sources to give approximately transmission rates of approximately 1kHz to 5MHz. The external source may range from slow frequencies to a maximum of 5MHz.

A twelve–bit "LAM" Status and "LAM" mask register–set provide a comprehensive interrupt system which has a separate overall allow interrupt bit. The Lam status register may be cleared or selectively cleared and the Lam mask register can be written, cleared, selectively set and selectively cleared. The mask and all control registers are cleared at power up or by a VMEbus reset.

Operational Features

Six registers provide communications between the VME BUS and the Serial Highway. Message transmission is initiated by:

1. Writing the command register with a serial Read or Command function or:–
2. Writing the Write Data register whilst the Command register contains a serial Write function.

Loading the Command register with a serial Write Command does not initiate transmission. The 24 Bit Serial Read Data may be read via the VME bus as two 16 Bit words after the reply message has been received.

Receipt of a reply or otherwise together with the state of the serial SX and SQ may be determined by reading the unit status register (offset – Ø4). The full status is obtained by reading offset 16. A new transfer should not be set–up until a reply has been received for the previous transmission.

Two bits are provided in the command register so that a Q–scan mode may be utilised if the basic parameters, function, crate are the same. The two bits are MQ and MR.

Two bits are provided in the command register so that a Q–scan mode may be utilised if the basic parameters, function, crate are the same. The two bits are MQ and MR.

If MR is set, then a 'Read" to the module initiates a repeat message. The serial Command sent, is identical if MQ=0, but is varied if MQ=1 depending on the state of the serial Q(SQ).

If SQ=1 then the serial address (SA) is incremented, whereas if SQ=0, SA is reset and the Serial station number (SN) incremented.

If SN increments beyond 24, then the crate address is cleared and the new transmission made with crate = 0. This gives address not recognised on receipt back at the VSD2992 which interrupts terminating the transfer.

Timeout

If 350mS elapses from the start of a message transmission and there has been no reply or unrecognised command message, the TIMEOUT signal is asserted which sets TMO LAM source. SHR also becomes true (SHR = RPL or TIMEOUT) and the RDY LAM source is set if/when CMD is true. Reply messages received after TIMEOUT is asserted are ignored.

Addressing the Module

The module has its addressing structure similar to the VXI system and as such is an A16/D16/D08(E0) device. The unit status register (Ø4) contains a booking bit, which is automatically set following a read, if previously unset.

D08 (E0) may only be used if the order of Byte transmission can be controlled, otherwise incomplete messages may be propagated as the message is started when the unit detects the least significant data has been loaded. The following table overleaf, gives the provisional register allocation:–

VME SHD 2992

PROVISIONAL REGISTER ALLOCATION

OFFSET	READ FUNCTION (16 BITS)	WRITE FUNCTION (16 BITS)
00	1111 REG A16 <3967> HYTEC ID	VECTOR 8BIT
02	MODEL CODE DEVICE TYPE 2992	NU
04	0 1 DMD SYN LAM SHR XMR INT EN SQ SX R 0 1 0 B	X X X X X X X X INT EN X X X X X X B
06	0	NU
08	0	NU
0A	RD LAM MASK 12 BITS	WRITE LAM MSK 12 BITS
0C	0 VECTOR 8BIT	CLR LMSK
0E	RD LAM STATUS 12 BITS	SELECTIVE CLR LAMS 12 BITS
10	0	CLR LAMS
12	0	SELECTIVE CLR LAM MSK 12 BITS
14	0	SELECTIVE SET LAM MSK 12 BITS
16	RD FULL STATUS 12 BITS	WRITE TX A, N, F, ETC 16 BITS
18	RD DMD STATUS 12 BITS	WRITE TX CRATE ADD 8 BITS
1A	RD RXD DATA BTM 16 BITS	WRITE TX DATA BTM 16 BITS
1C	RD RXD DATA TP 8 BITS	WRITE TX DATA TP 8 BITS
1E	RD DMPSTORE & INC PTR 8 BITS	ENABLE/DISABLE DUMPSTORE 1 BIT
20	RD DMPSTORE PNTR 10 BITS	WRITE DMPSTORE PNTR 10 BITS
22	RD UPORT SETTING 8 BITS	WRITE UPORT SETTING 3 BITS
24	0	WRITE FIFO 8 BITS
26	0	ENABLE/DISABLE LOOP/BACK 1 BIT
28	0	NU
2A	0	NU
2C	0	NU
2E	0	NU
30	RD TX CRATE ADD (IF L/B) 8 Bits	NU
32	RD TX N IF L/B 8 Bits	NU
34	RD TX A IF L/B 8 Bits	NU
36	RD TX F IF L/B 8 Bits	NU
38	RD TX D IF L/B 8 Bits	NU
3A	RD TX D IF L/B 8 Bits	NU
3C	RD TX D IF L/B 8 Bits	NU
3E	RD TX D IF L/B 8 Bits	NU

EXPANDED REGISTER DETAIL

– Regsiter Bits –

OFFSET	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0E	0	0	0	0	SERR	DMD	XMR	RDY	TPE	TMO	LPE	ADNR	DERR	ERR	$\overline{SX}$	$\overline{SQ}$	LAM STATUS
16	0	0	0	0	S. CRATE						M2	M1	DERR	SQ	SX	ERR	FULL STATUS
18	0	0	0	0	S. CRATE						M2	SGL					DEMAND
0A	–	–	–	–	$\overline{X}$	$\overline{X}$	$\overline{X}$	$\overline{X}$	$\overline{X}$	$\overline{X}$	$\overline{X}$	$\overline{X}$	$\overline{X}$	$\overline{X}$	$\overline{X}$	$\overline{X}$	LAM MASK
12	–	–	–	–	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	SEL/CLR LAM MASK
14	–	–	–	–	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	$\overline{1}$	SEL/SET LAM MASK
16	MQ	MR	N16	N8	N4	N2	N1	A8	A4	A2	A1	F16	F8	F4	F2	F1	WRITE N,A,F
18	–	–	–	–	–	–	–	–	–	–	CRATE						WRITE CRATE
1A	16 LOWER DATA BITS – READ or WRITE																
1C	–	–	–	–	–	–	–	–	8 HIGH (UPPER) DATA BITS – READ or WRITE								
24	–	–	–	–	–	–	–	–	PAR	DLIM	M2	M1	8	4	2	1	WRITE FIFO
1E	–	–	–	–	–	–	–	–	PAR	DLIM	M2	M1	8	4	2	1	READ DUMP STORE
30 > 3E	–	–	–	–	–	–	–	–	PAR	DLIM	M2	M1	8	4	2	1	READ TX N,A,F & DATA

2.0 Setting–up a System

2.1 Byte or Bit Serial

The selection of Bit or Byte Serial is dependant on the site circumstances. If the distances are great, then the cable costs and the interbit skew can be excessive, and therefore Bit Serial might be chosen. If distances are short, then normally Byte Serial would be chosen to increase the system speed. Other factors may govern the choice such as the use of U–Port Adaptors which may only operate in Bit Serial mode. Whatever the reason, the choice must be made, and the links can be set as follows:–

For Bit Serial connect LK1 Pins 2 to 3.
For Byte Serial connect LK1 Pins 1 to 2.

Note: All Serial Crate Controllers must also be set to the same mode.

2.2 Clock Selection

The choice is as follows:– Internal crystal clock.
Internal variable clock.
External clock.

Selection is by link on SW5 see FIG 1. And would normally be the crystal clock selection.

2.3 Clock Speed

The clock speed and hence the system speed is largely determined by setting the amount by which the selected clock is divided down. Selection is by links on SW4 and SW3, see FIG 1.

FREQUENCY		CRYSTAL	VARIABLE	EXTERNAL
SW4	SW3	SW5/3	SW5/2	SW5/4
2	2	–	–	Ext
3	2	5MHz	2–6Mhz	Ext Div by 2
4	2	2.5MHz	Div by 2	Div by 4
5	2	1MHz	Div by 5	Div by 10
3	3	500kHz	Div by 10	Div by 20
4	3	250kHz	Div by 20	Div by 40
5	3	100kHz	Div by 50	Div by 100
3	4	50kHz	Div by 100	Div by 200
4	4	25kHz	Div by 200	Div by 400
5	4	10kHz	Div by 500	Div by 1000
3	5	5kHz	Div by 1000	Div by 2000
4	5	2.5kHz	Div by 2000	Div by 4000
5	5	1kHz	Div by 5000	Div by 10000

2.4 Space Byte Insertion

2.4.1 Read/Write Functions

In order to allow for the serial crate controller to reply, sufficient time must be allowed for it to complete its in–crate or internal cycle. Hence the transmitted message is padded out with a number of space bytes. For normal data messages, the minimum suggested number is in the table that follows:–

Byte Rate Mbytes/Sec	Write/Test Function	Read Function
< 0.5 *	8	4
0.5 – 1.5	9	4
1.5 – 2.0	10	6
2.0 – 2.5	10	6
2.5 – 3.0	11	7
3.0 – 3.5	11	7
3.5 – 4.0	12	8
4.0 – 4.5	13	9
4.5 – 5.0 **	14	10

***** Note: All Bit Serial transfers are in this range.

****** Note: Correct SCC operation is not guarenteed above 5Mhz.

This is based on the formula given in EUR6100(1982); **S = N(OP) + N(REP) + 1** where N(OP) and N(REP) are the number of received space bytes required to cover the maximum dataway cycle time of the SCC and its reply. N(OP) is the next integer above T(OP) / T(byte) where T(OP) is the maximum data cycle time (assumed 1.2uS) and T(byte) is the minimum byte period of the system. Note that larger numbers may be safely used at the expense of the system speed. The relevant numbers are set in binary format on DIL Switch SW2, the maximum is 16, see FIG 1.

2.4.2 Control Function Space Bytes

Write control functions with N30 present act on the SCC itself, and may cause reconfiguration. This can typically take 100mS. Provision is made to extend the number of space bytes to those contained in 120mS if it is required to await a true reply, rather than accept the longer time–out period. The decision is made by changing LK17 as follows. (See FIG 1.)

LK17 1 to 2 Delay OUT
LK17 2 to 3 Delay IN

2.5.0 VME Base Address

The unit responds to Address Modifiers 29_{16} or $2D_{16}$ together with a base address selected from the top 4k of the A16 address space. For example $C000_{16}$ to $FFC0_{16}$. This is set as 0 to 255 on SW1, see FIG 1.

2.6 VME Interrupt Line

The unit may be set to interrupt on any one of the 7 interrupt lines. It is set by selecting one of the links LK3 – LK9 corresponding to Interrupt 1 – 7. The adjacent links LK10 – LK16 should also be selected to inform the control stage which interrupt acknowledge to reply to.

2.7 External Connections

2.7.1 Serial Highway Connections

The unit may operate with one of three configurations illustrated in FIG 2.

(a) Two cable Byte mode:–
This may be considered the normal mode.
A 12 pair cable runs from the output 'D' connector to the first SCC input 'D' connector.
A 12 pair cable runs from the output 'D' connector of the SCC, either to another SCC input 'D', or back to the input 'D' connector of the SHD unit, ie, the final SCC output returns to the SHD unit.

(b) Two cable Bit mode:–
As above but the cable may be reduced to 2 pairs for economy.

(c) Single cable with a minimum of four pairs:–
In this case a change–over plug is inserted in the output plug of both the last SCC and the SHD unit, the remote clock and data return down the same cable.

2.7.2 U–Port Connector

The unit may be used to control and monitor a HYTEC UPA 0542 Master Fibre Optic U–Port Adaptor, detailed data sheets are available by request. This is accomplished via a 15 way socket labelled 'U–Port'. Note that U–Ports may be manually set and may still form part of the Serial Highway system without being controlled from the SHD unit.

2.7.3 Message Started

A pulse is available at the 'MSGSTD' front panel LEMO connector, when a message is initiated. This may be used as a test facility or as an input to any other device in the system.

3.0 Using the VSD 2992

3.1 Insertion into the Crate

The unit should be plugged into a VME crate with either other cards between it and the master unit, or with links completing the interrupt 'IACK IN' and 'IACK OUT' chains. Otherwise there will be no interrupts serviced by the unit. This is normal VME Crate interrupt daisy chain set–up procedures.

3.2 Initial State

With the unit plugged in, cables attached to all units in the serial loop and all units powered, the 'SYCH' LED on the front panel should be lit. All other LEDs should normally be 'OUT', an exception could be the 'DMD' LED if demands are enabled somewhere in the serial loop without software initialisation being required. If the 'SYNC' LED is not lit, then no clock is being received if in byte mode, or no 'wait' bytes are being detected if in serial mode.

Check:– External clock is present if this option was selected.
All cables are present.
All units are powered.
All units are set to the same mode.
The clock frequency is slow enough for the size of loop. It would be advisable to start with a slow clock speed on new installations.

3.3 The Registers

The following assumes a working unit together with working modules in association. Fault finding and test procedures are delt with later in this document. All offsets are from the base register address.

Control Registers offset 00_{16} – 14_{16} and register 22_{16} may be considered as control registers. The most important of these is 04_{16}, this contains various fixed bits plus a booking bit (bit 0) useful for multiuser environments; the interrupt enable bit (bit 7), and copies of the most important of the LAM Status bits. The unit may thus be operated on interrupts or by looping on this address until the required condition arises. All these control registers may be read or loaded DO8(E0), however, upper byte writes do not occur in real–time but are stored and actioned with the lower byte.

3.3.1 Register 04 Condition Bits

Bit 0 = 1 BUSY Set after read if not set, cleared by Bit 0 = 1. (Module booking kit).
Bit 4 = 1 RDY Complementary to BUSY.
Bit 5 = 1 X response of last CMD.
Bit 6 = 1 Q response of last CMD.
Bit 7 = 1 Overall interrupt enable set by write Bit 7 = 1, Cleared by interrupt reply.
Bit 8 = 1 XMR, CMD has transmitted, cleared by new command.
Bit 9 = 1 SHR, XMR present and reply or time–out received, cleared by new command.
Bit 10= 1 LAM, 1 or more masked LAMs is set, cleared when OE is cleared, or when OA is cleared.
Bit 11= 1 SYNC, sync was lost for a minimum of 4 bytes, cleared by resync.
Bit 12= 1 DMD, a DMD message received, cleared by 0E writes.

3.3.2 Register 0A 12–Bit LAM Mask

Set and cleared by 0A, 0C, 12 and 14 writes. This register determines which of the 12 LAM Status

bits is allowed to generate an interrupt, assuming the overall interrupt enable is set.

3.3.3 Register 0E 12–Bit LAM Status

These bits are allowed to set interrupts if the corresponding bit in 0A is set.

Bit 0 = 1 $\overline{SQ}$, the Q response to the last serial command was 0.
Bit 1 = 1 $\overline{SX}$, the X response to the last serial command was 0.
Bit 2 = 1 ERR, an error was detected in the last command by an addressed SCC. Usually /SQ and /SX will also be set as no dataway cycle will have taken place.
Bit 3 = 1 DERR, indicates that an error was detected by the addressed SCC in the previous message addressed to it.
Bit 4 = 1 ADNR, indicates that the crate address was not recognised by any SCC on the Serial Highway. It is detected by the VSD 2992 detecting an output message with /M1 and /M2 both present at its input socket.
Bit 5 = 1 LPE, indicates that a linear parity error was a detected in the reply message.
Bit 6 = 1 TMO, indicates that no reply message was received in the 350mS since the last command message was sent.
Bit 7 = 1 TPE, indicates that a transverse parity error occurred on an incoming message. Wait byte TPE are ignored.
Bit 8 = 1 RDY, indicates that a command sequence has completed, ie, a good reply has been received, a time–out has occurred or the command has returned as address not recognised.
Bit 9 = 1 XMR, indicates that the unit has finished transmitting the last command.
Bit 10= 1 DMD, indicates that a demand message has been received since the status was last cleared.
Bit 11= 1 SERR, indicates that the unit lost synchronisation for at least four byte times.

Note: All of the above bits are bit cleared or cleared by writing register 0E or 10.

3.3.4 Interrupt Vector

The 8 bit vector used when replying to interrupt acknowledges is loaded by writing to the lower byte of register 00. It may be examined by reading register 0C.

3.3.5 U–Port Settings

Register 22 controls and monitors the state of a Hytec U–Port Adaptor if fitted. A write of register 22 lower four bits sets the available modes. A read of register 22 confirms the current settings as written and also monitors the three lines which describe the actual connection state at the adaptor, ie, MAIN LOOP Operable, BACK–UP Operable and internal or external clock. For full information as to the use of these lines, please refer to the Hytec U–Port Adaptor manuals.

Note: All of the above registers may be operated D08(E0) with read and write although upper byte writes only occur when the lower byte write is received. *It is imperative therefore, the upper byte is set–up first, otherwise the current contents will be written incorrectly.*

Data Registers: Registers 16–1C may be considered data registers and are concerned with the transmission and reception of messages and data on the Serial Highway. They must be read and written in the correct sequence of high bytes first as all changes occur when the lower byte

is actioned. The crate address is considered the high byte of the 24 bit serial C, N, A and F definition. Note that the read and write functions are not compatible.

3.3.6 Crate Address (Register 18 Write)

The 6 bit crate address is loaded by a write to register 18. The register is part of the command sequencer and is not readable under normal operation. See Test Facilities.

3.3.7 Command Register (Register 16 Write)

This 16 bit register is split into sections as follows:–

Bit 0 – 4	Function F1, F2, F4, F8 and F16 of the CAMAC Command to be used in the remote crate.
Bit 5 – 8	Subaddress A1, A2 ,A4 and A8 of the CAMAC Command to be used in the remote crate.
Bit 9 – 13	Station number N1, N2, N4, N8 and N16 of the CAMAC Command to be used in the remote crate.
Bit 14	MR, this is a special bit which when set causes an automatic repeat of the current read command (if any) immediately following a read of the lower byte of register 1A. A block read is thus possible on the same location.
Bit 15	MQ, this is a special bit which when set in conjunction with MR, causes an automatic repeat read with the Subaddress advanced by one if the received Q=1. If Q=0, then the Subaddress is cleared to zero and the station number advanced by 1 before doing a repeat read. This forms the Q–Scan of the crate. When the station has incremented to 24, then the crate address is made zero which returns as ADNR and terminates the transfers.

Note: 1 If MR and MQ are both zero then only a single transfer takes place.

Note: 2 If the Function specified is a read then the message is transmitted on receipt of the lower byte of register 16, ie, when the Function is loaded. If the Function is a write, then the message is transmitted when the lower byte of data has been loaded.

Note: 3 Like the crate address, the register forms part of the message sequence so that the data can not be read back under normal operation.

3.3.8 Transmit Data Top (Register 1C Write)

Bits 0 – 7 of register 1C form bits 17 – 24 of the CAMAC data to be sent to the remote crate. It is not readable under normal operation. No transfer is initiated when this data is loaded.

3.3.9 Transmit Data Bottom (Register 1A)

Bits 0 – 15 of register 1A form bits 1 – 16 of the CAMAC data to be sent to the remote crate. If a write command is present in register 16 then transmission commences on receipt of the bottom byte bits 0 – 7. Note, a block transfer to the same CAMAC location therefore only requires the data to be loaded. The command information may be re–used.

Serial Highway Status: Registers 16 and 18 are status registers containing information read from the Serial Highway. They must be used in conjunction with the LAM Status Register (0E) and/or the Device Status Register (04) in order to confirm whether they are valid.

3.3.10 Full Status Register (Register 16 Read)

This register contains the status information which was received in the last reply message from the last addressed SCC. It is only valid after the setting of RDY in the LAM Status Register (OE), but remains true until a new command is issued. It is necessary therefore, to ensure that RDY is cleared prior to issuing a new command or initiating one if in repeat mode.

Bits 6 – 11	Crate address of replying SCC.
Bit 0 = 1	ERR, an error was detected in the command message just terminated.
Bit 1	SX, X response to the command just terminated, always 0 if ERR set or M1 = M2 = 0.
Bit 2	SQ, Q response to the command just terminated, always 0 if ERR set or M1 = M2 = 0.
Bit 3	DERR, SCC had an error in the previous command addressed to it.
Bit 4 & 5	M1 and M2 copy of the command/reply definition bits received in the second byte of the serial reply message.

3.3.11 Demand Status (Register 18 Read)

This register (18) contains the demand information received from the Serial Highway via an unsolicited demand originating in one of the possible 64 crates. It is not a true register, but is the current output from a 64 word FIFO memory. Because of this, the data may only be read once and is only valid if DMD is set in the LAM Status or Unit Status. It must not be read on the fly, but only in answer to a DMD being set. This DMD should be cleared before reading the DMD status. Reading the DMD status clears the current information and will reset DMD if a further DMD is outstanding.

Bits 6 –11	Crate address of the originating SCC.
Bits 0 – 4	Graded LAM describing the source of the interrupting device.
Bit 5	M2 as received, should be 1 for a true DMD message.

Received Data: Registers 1A and 1C contain the data received from the addressed crate for the last transmitted Serial Highway command. The data is only valid if the last command has terminated and a reply has been received, ie, RDY has been set. The data remains valid until a new command starts to transmit. It is therefore essential that the RDY status is cleared before issuing a new command or reading the registers if MR is set, as the readings of the lower byte of 1A triggers the new command.

3.3.12 Read RXD Data Top (1C)

This register contains the top 8–bits of data (17–24) received from the remote crate during the last command sequence. It is only valid if RDY has been set, after being reset prior to the command being issued.

3.3.13 Read RXD Data Bottom (1A)

This register contains the bottom 16–bits of data (1–16) received from the remote crate during the last command sequence. It is only valid if RDY has been set, after being reset prior to the command being issued. It may be read as two lots of 8–bits in D08(E0) mode, but care must be taken to read the lower byte last. This is because the reading of the lower 8–bits triggers a new command if MR is set.

3.4 Test Facilities

The following facilities have been added to aid testing and fault finding:–

a) Comprehensive LED indication of LAM Status and operating state.

b) A loop–back facility to by-pass the external Serial Highway.

c) Read back of command and data 6–bit bytes with the corresponding parity and delimiter bit, ie, 8–bits.

d) A 64 byte command generator FIFO store.

e) A 1kbyte DUMP store which can be set to monitor the incoming 6–bit data patterns received by the unit.

3.4.1 LED Indicators

Sixteen LED indicators have been provided to enable the operator to visually observe the operation of the unit, they are as follows:–

a) All 12–bits of the LAM Status Register are displayed.

b) The LAM LED indicates that at least one of the LAM status bits, with its LAM mask set is present.

c) SYNC monitors the state of synchronisation of the unit. If present, it indicates that the unit is receiving clock pulse if in Byte–Mode or detecting 'wait' bytes or synchronised data if in Bit–Mode.

d) MSG indicates that a serial command has commenced transmission. It is present for approximately 100mS following the first byte of the command sequence.

e) ADD indicates that the unit is being addressed from the VMEbus. Each access results in the LED being illuminated for approximately 100mS.

3.4.2 Loop–Back Facility

NB: UNIT SHOULD BE SET TO BYTE MODE. With so many units possibly connected on a Serial Highway, it is necessary to confirm that the fault, if any, is within the VSD2992 or external to it. A facility to externally exclude the Serial Highway and the drivers and receivers of the VSD2992 has been provided. The loop–back (LB) is made by connecting the internal source of signals to the received signals path without going via any cables. The facility is activated by writing bit 0 = 1 in register 26 and cleared by writing bit 0 = 0. In this mode any command will be returned as if the external crate did not recognise the crate address, ie, ADNR will be set. The facility becomes extremely powerful when used with the following facilities.

3.4.3 Transmitted Command and Data Registers

The command data and write data when loaded is split up into the sequencing registers in the 6–bit bytes to be transmitted. These are only allowed on to the internal bus at the correct time as the bus is normally transmitting wait byte in the quiescent state. Any switching whilst in the normal operating mode would therefore create errors all around the serial loop. The facility to read back this data in the form in which it would be transmitted is therefore limited to the LB state. With the unit set to Loop–Back (LB) then the 8–bit pattern which would be transmitted may be selected as follows:–

Register 30 **Rd Tx Crate Address**

Bit 0 – 6	Crate Address.
Bit 7	Delimiter bit should be 0.
Bit 8	Transverse parity bit making odd parity.

Register 32 **Rd Tx N**

Bit 0 – 4	N – Station number in the remote crate.
Bit 5 = 1	Always 1.
Bit 7	Delimiter bit should be 0.
Bit 8	Transverse parity.

Register 34 **Rd Tx A**

Bit 0–3	A – Subaddress in the remote crate.
Bit 4 = 0	Message identifier M1 = 0 for command.
Bit 5 = 0	Message identifier M2 = 0 for command.
Bit 7	Delimiter bit should be 0.
Bit 8	Transverse parity.

Register 36 **Rd Tx F**

Bit 0 – 4	F – Function to be used in the remote crate.
Bit 5 = 1	Always 1.
Bit 6	Delimiter bit should be 0.

Register 38 **Rd Tx Data 19 – 24**

Bit 0 – 5	Tx Data bits 19–24 for the remote crate.
Bit 6	Delimiter bit should be 0.
Bit 7	Transverse parity bit.

Register 3A **Rd Tx Data 13 – 18**

Bit 0 – 5	Tx Data bits 7 – 12.
Bit 6	Delimiter bit should be 0.
Bit 7	Transverse parity bit.

Register 3E **Rd Tx Data 1 – 6**

Bit 0 – 5	Tx Data bits 1 – 6.
Bit 6	Delimiter bit should be 0.
Bit 7	Transverse parity bit.

3.4.4 Command FIFO

A 64–byte 8–bit Command FIFO is available for generating test message which may be set up containing errors if required. The FIFO is arranged to substitute for the message command and data registers, and because it changes over without discontinuities, it can be used either on LB or with the serial interface complete. Messages not normally issued by the Serial Highway driver can thus be sent around the loop; ie, commands, demands, truncated commands, replies, wait bytes with parity errors or incomplete messages. The FIFO is set up as follows:–

Register 24 write, each 8–bit Serial Highway byte of the required message until complete. See formats in FIGs 4 – 9 in the appendix. The final byte for a command message must be correct longitudinal parity followed by as many space bytes as required plus at least two wait bytes (one is the end byte). For other messages at least one wait byte should be located following the delimiter byte. When complete, the FIFO contents are transmitted by writing zero or any other read to register 16. No crate address is required as the information is not used. The FIFO will then take over and release when transmission is complete. Note that only one command message should be loaded if correct operation is required.

3.4.5 Dump Store

Another facility is a 1kbyte Dump Store which may be set up to receive up to 1k worth of the 8–bit bytes received from the Serial Highway for analysis. The store only collects non–wait bytes except for the wait byte immediately following a message sequence. It is set up by writing the address pointer to zero. Write register 20 = 0, and then the store is started by Enable Dump Store Register 1E bit 0 = 1. Collection is stopped by writing register 1E bit 0 = 0. The pointer should then be read by register 20 read, and the number stored. This represents the valid number of entries for the sequence. The pointer should then be reset, register 20 = 0, and the store read and the pointer incremented by register 1E read for valid number of entries. The Dump Store may be used at any time.

4.0 Appendix Figures 1 to 9

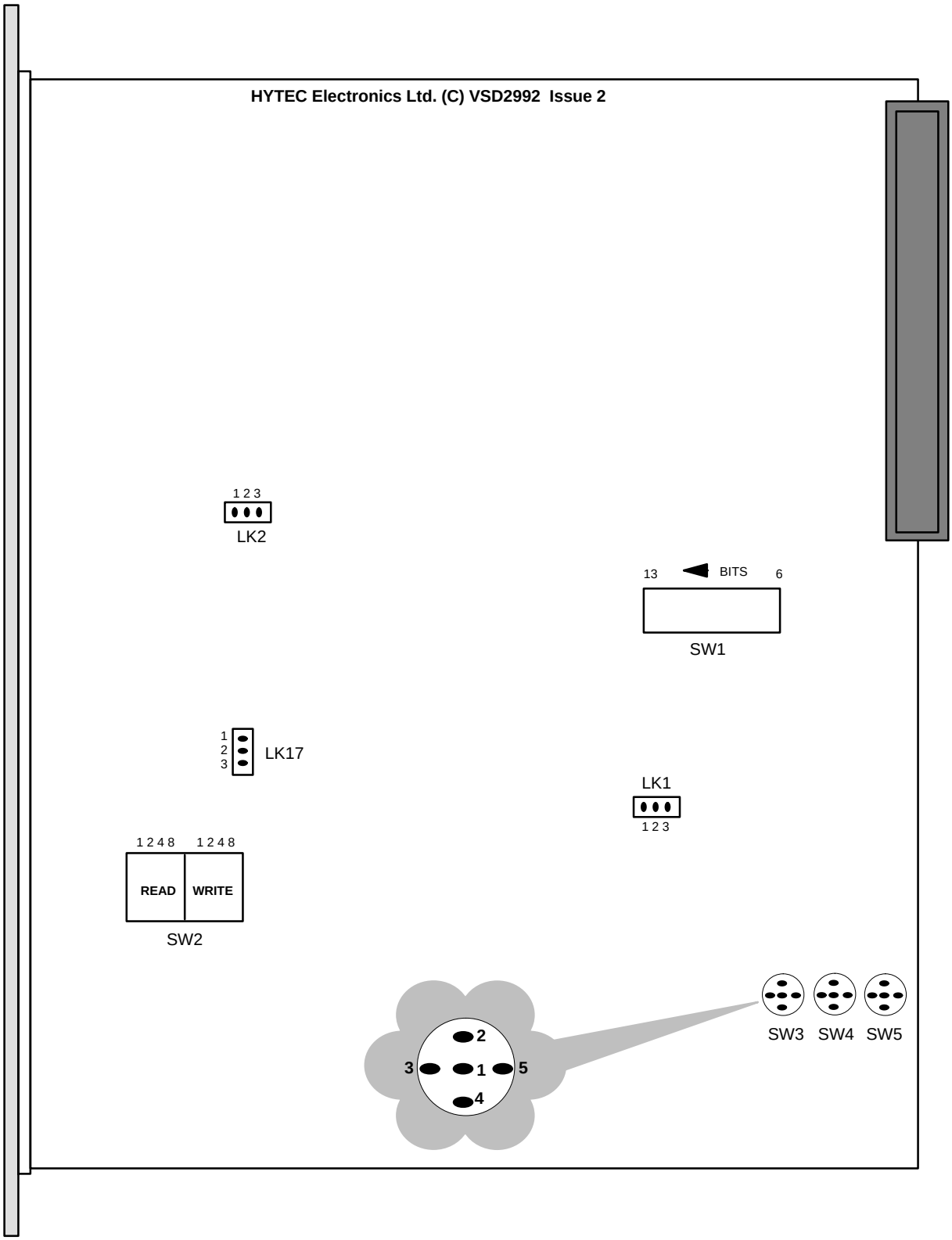


Fig 1.

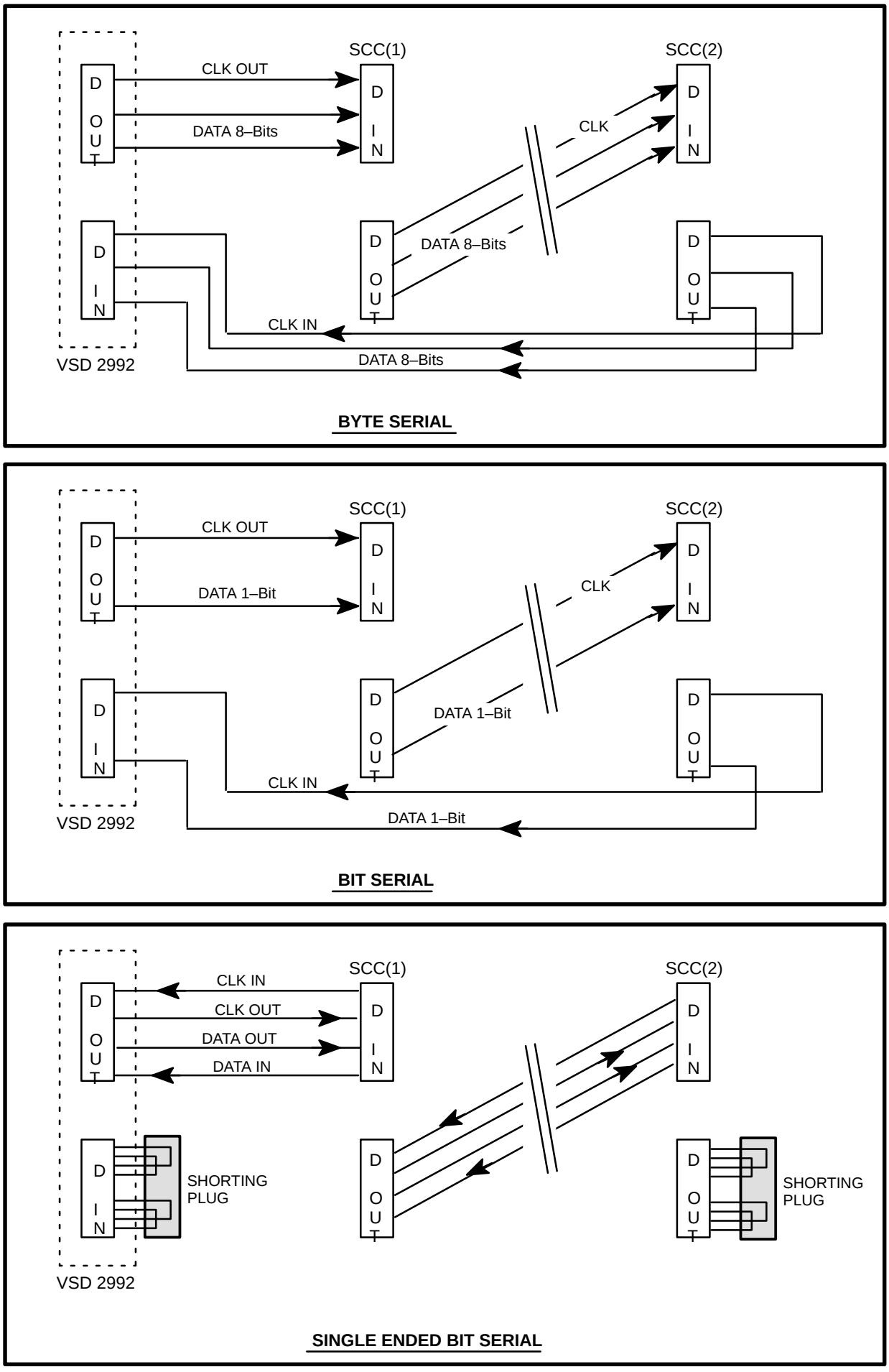

SCC(1)
SCC(2)
CLK OUT
DATA 8–Bits
CLK
DATA 8–Bits
CLK IN
DATA 8–Bits
VSD 2992
BYTE SERIAL
SCC(1)
SCC(2)
CLK OUT
DATA 1–Bit
CLK
DATA 1–Bit
CLK IN
DATA 1–Bit
VSD 2992
BIT SERIAL
SCC(1)
SCC(2)
CLK IN
CLK OUT
DATA OUT
DATA IN
SHORTING PLUG
SHORTING PLUG
VSD 2992
SINGLE ENDED BIT SERIAL

FIG 2.

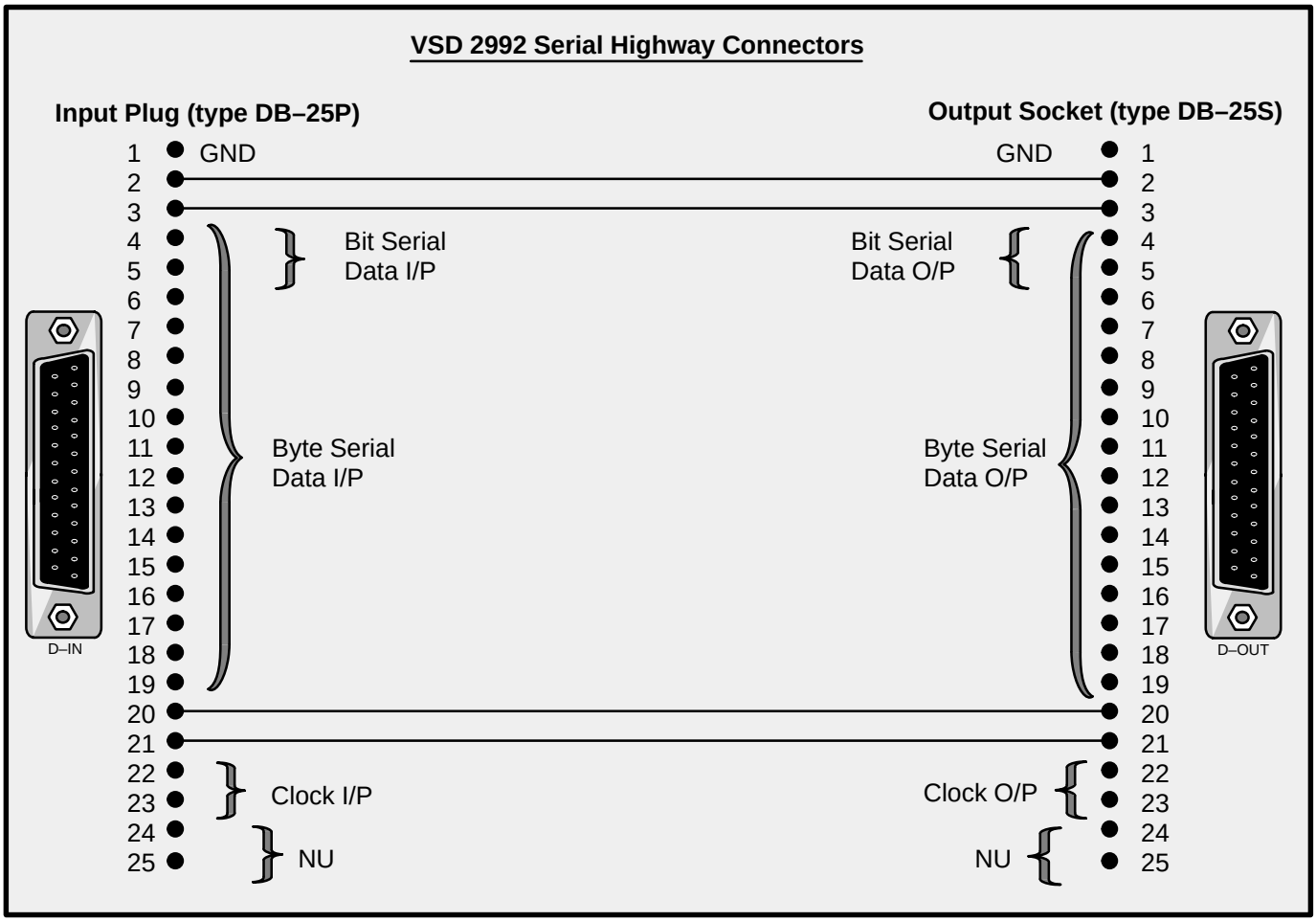

VSD 2992 Serial Highway Connectors
Input Plug (type DB–25P)
Output Socket (type DB–25S)
GND
GND
Bit Serial
Data I/P
Bit Serial
Data O/P
Byte Serial
Data I/P
Byte Serial
Data O/P
Clock I/P
Clock O/P
NU
NU
D–IN
D–OUT

Fig 3.

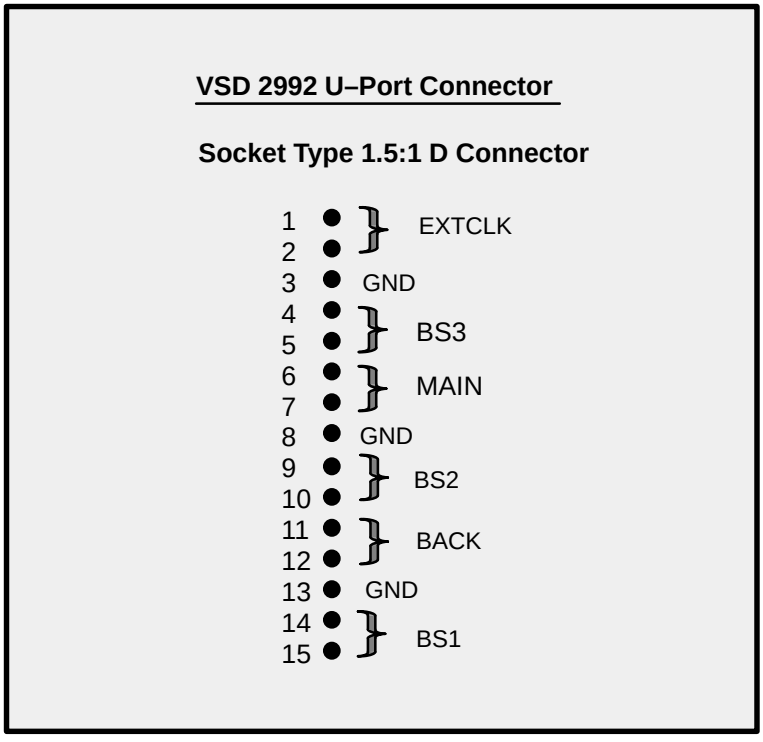

VSD 2992 U–Port Connector
Socket Type 1.5:1 D Connector
EXTCLK
GND
BS3
MAIN
GND
BS2
BACK
GND
BS1

Fig 4.

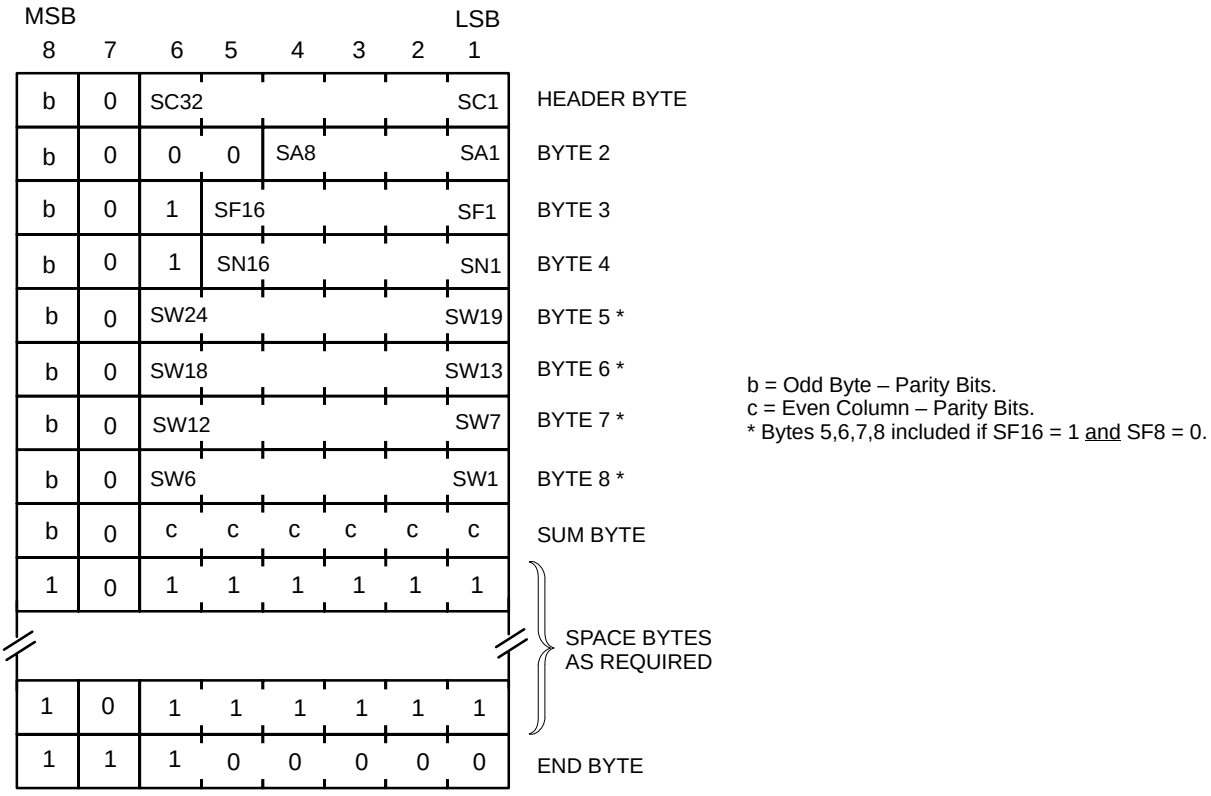
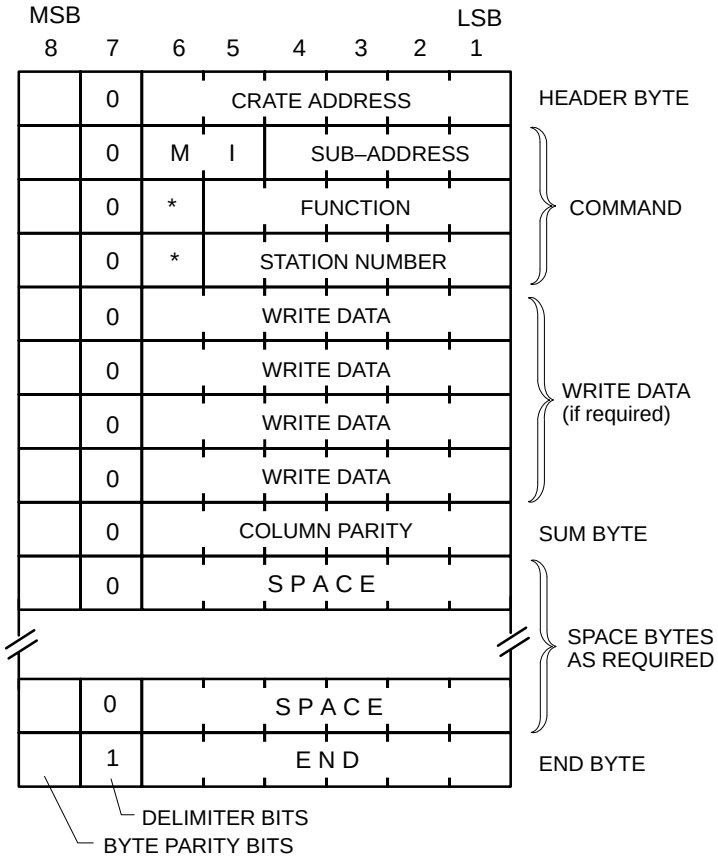
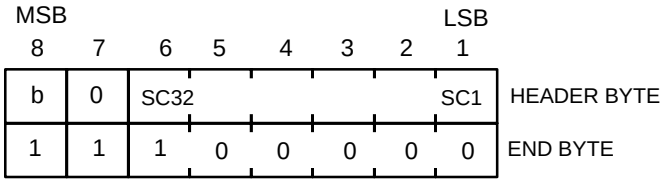


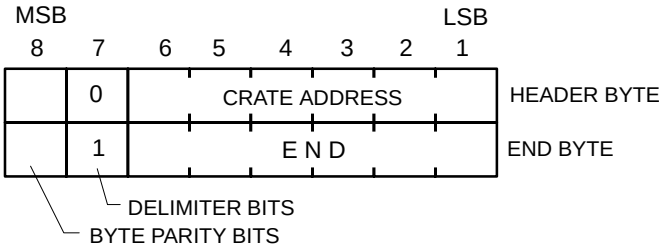
Fig 5. Command Message: Bit Assignments



* Reserved Bits.
MI = Message Identifier Field.

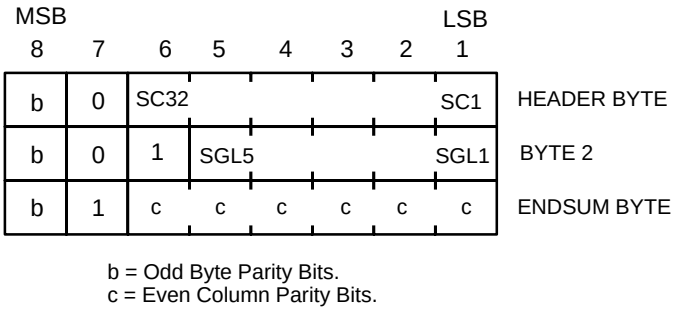


Truncated Command Message: Bit Assignments

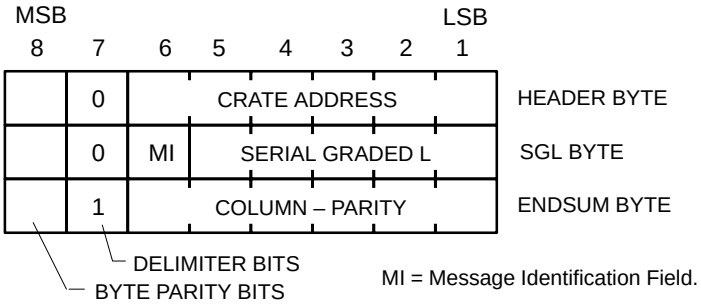


Truncated Command Message: Field Assignments

Fig 6. Command Message: Field Assignments



Demand Message: Bit Assignments



Demand Message: Field Assignments

Fig 7.

Table: Length of Command/Reply Transactions

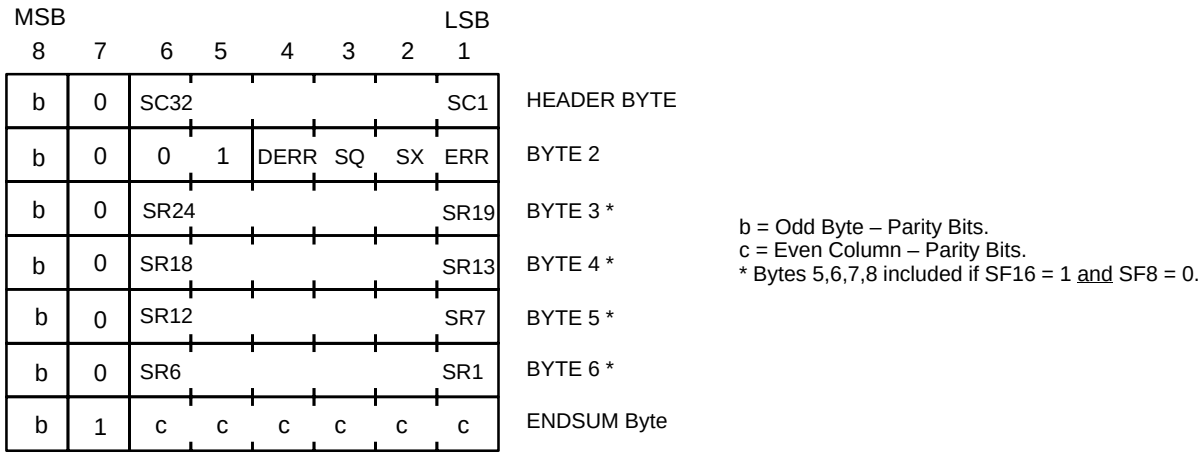
Operation	Function Field		Number of Bytes		
	F16	F8	Command from Header to SUM Inclusive	Reply from Header to ENDSUM Inclusive	Command/ Reply Transaction
Read	0	0	5	7	12*
Control	0 1	1 1	5	3	8*
Write	1	0	9	3	12*

* Minimum length, assuming that Reply Header is transmitted by SCC as first SPACE byte is received, and ENDSUM is transmitted as END byte is received.

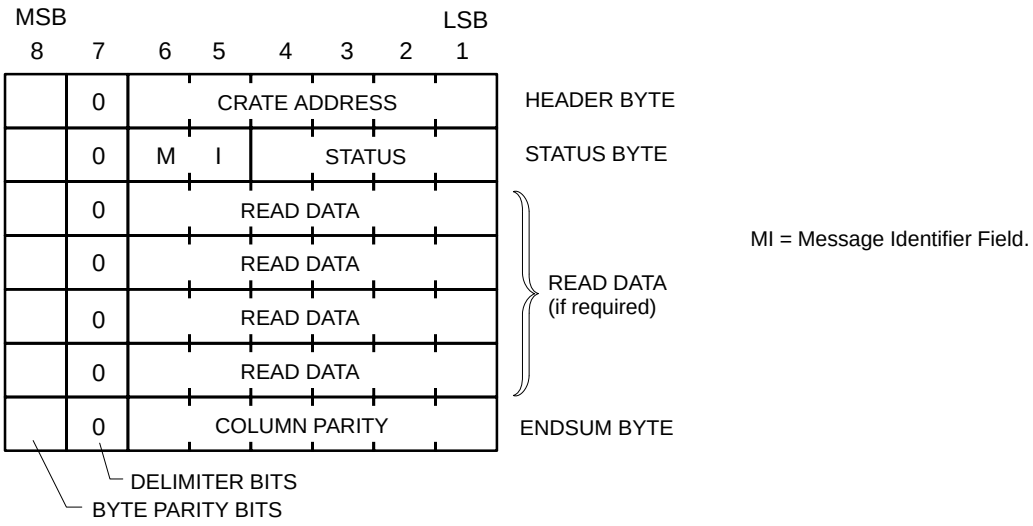
Table: Contents of Message Identification Field

Message	MI–Field	
	M2	M1
Command	0	0
Reply	0	1
Demand	1	–

FIG 8.



Reply Message: Bit Assignments



Reply Message: Field Assignments

Fig 9.

5.0 References

EUR4100 CAMAC Specification 1969.

EUR6100 Serial Highway and Serial Crate Controller Type L–2.

HYTEC Serial Crate Controller SCC 2401.

HYTEC Master Dual Fibre–Optic U–Port Adaptor UPA542.

HYTEC Slave Dual Fibre–Optic U–Port Adaptor UP541.

HYTEC Serial Highway Driver SHD 992 (CAMAC : CAMAC).

IEEE 595

VSD 2992 ADDENDUM

6.0

6.1

The following function has been added to units, serial number 106 onwards:–

Reset Non–Control

This function resets all the non–control aspects including the FIFOS and the DUMPSTORE. It is most useful for clearing out any accumulated DEMANDS during program testing stage.

It is activated by writing to the UPORT control with Bit 7=1.
NB: if UPORT is in use bits 0–3 must be set correctly as well.

6.2

The following function has been added to units serial number 183 onwards:–

Reset Repeat

This function has been included to enable the repeat function ie. MR bit set, to be cancelled.

To use: following the last but one read required,

a) send a write to the UPORT control with bit 15=1.
NB: if UPORT is in use bits 0–3 must be set correctly as well.

b) read the last data, this will be obtained without a further read of the serial highway.