Hall-B Photon Tagger
T-Counter Programmable "OR" Logic

Manual

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Overview

The T-Counter Programmable "OR" Logic board is used to construct the Hall-B Photon Tagger detector logic. The Tagger detector consists of 61 "T-Counter" scintillators and 384 "E-Counter" scintillators. The E-counter signals are arranged in 24 groups with 16 channels per group. The purpose of the OR-logic is to trigger a specific E-counter group based on the location of T-counter events.

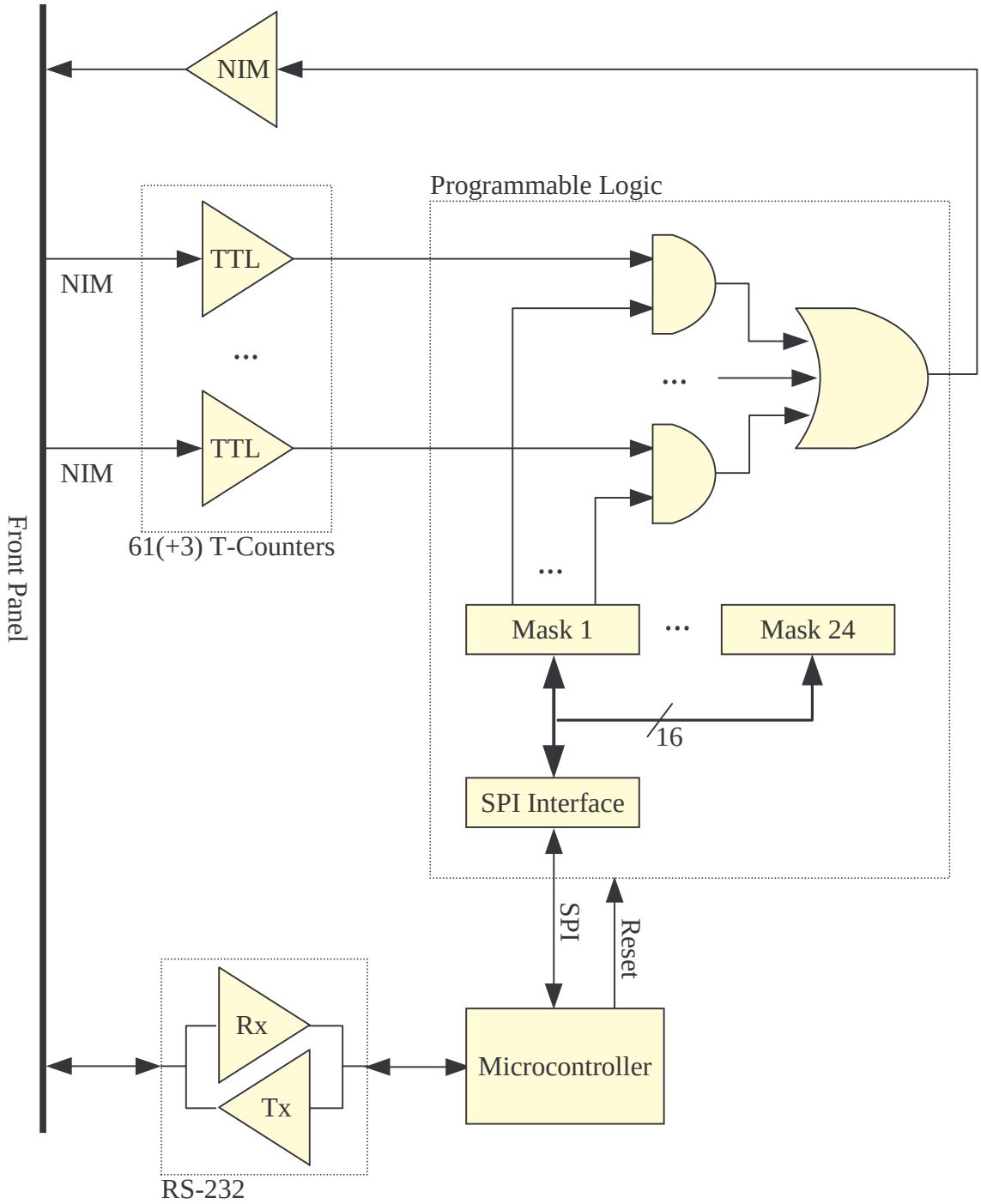
The 64 (61 used) NIM-level inputs are discriminator pulses from T-counter scintillators. The 24 NIM-level outputs correspond to the E-counter groups. Each output is a logical OR of a specific group of T-counters. T-counters can be included in the OR function by setting mask bits in internal registers. There is one mask register associated with each output. The T-counter groups are described in the T-to-E mapping table. Note that many T-counter groups overlap resulting in some input channels triggering more than one output.

There are four NIM-level master-OR outputs that are an OR of all 64 inputs. Note that since there are only 61 T-counters, input channels 62→64 participate only in master-OR.

Since this is a combinatorial OR logic circuit, the output pulse width is defined by the pulse timing and widths of the participating input channels.

The mask registers can be accessed through an RS-232 serial port (9600, N, 8, 1). An on-board microcontroller manages the communication between the serial port and the OR-logic. It also monitors logic voltages, manages a watchdog, and reports the cause of controller reset (watchdog, brownout, etc).

T-Counter “OR”-Logic
Block Diagram



Specifications

General		
Power Supply Requirements	+5V, 0.7A;	-5V, 1.9A
Fuses	+5V, 1.6A;	-5V, 3.1A
Chassis Fuses (3AG)	+5V, 3/8A;	-5V, 3/8A
Chassis Dimensions	EIA 19” wide, 2U high, 8” deep	
LEDs	Green: +5V, -5V; Yellow: controller status, logic status	
I/O Connectors	Logic Input:	64 LEMO
	OR Output:	24 LEMO
	Master OR Output:	4 LEMO
	RS-232:	Female 9-Pin D-Sub
On-board Connectors	Power:	3-pin screw-terminal
	RS-232	3-pin screw-terminal
Input logic level	NIM	
Output logic level	NIM	
Propagation Delay	16nS→20nS	
Microcontroller	Microchip: PIC16F876-20/SP	
Host Communications	RS-232 (9600, N, 8, 1)	
Registers	41 16-bit I/O registers; 16 16-byte EEPROM registers	
Watchdog	Microcontroller resets if inactive for more than 150mS	
	Timeout can be forced by accessing register 0x29	
Reset Condition	All mask bits are set “on” after power-up or reset.	

Registers / T-E Mapping

Register	Description	Mask Bits Used	Range	Input Group
0x00	Status	N/A	N/A	N/A
0x01	Output 1 Mask	b0000000001111111	6..0	7→1
0x02	Output 2 Mask	b0000000001111111	6..0	9→3
0x03	Output 3 Mask	b0000000001111111	6..0	12→6
0x04	Output 4 Mask	b0000000001111111	6..0	15→9
0x05	Output 5 Mask	b0000000111111111	8..0	20→12
0x06	Output 6 Mask	b0000000001111111	6..0	21→15
0x07	Output 7 Mask	b0000000000001111	3..0	22→19
0x08	Output 8 Mask	b0000000000000111	2..0	23→21
0x09	Output 9 Mask	b0000000000000111	2..0	24→22
0x0A	Output 10 Mask	b0000000000001111	3..0	26→23
0x0B	Output 11 Mask	b0000000000001111	3..0	27→24
0x0C	Output 12 Mask	b0000000000001111	3..0	29→26
0x0D	Output 13 Mask	b0000000000001111	3..0	30→27
0x0E	Output 14 Mask	b0000000000001111	3..0	32→29
0x0F	Output 15 Mask	b0000000000011111	4..0	34→30
0x10	Output 16 Mask	b0000000000011111	4..0	36→32
0x11	Output 17 Mask	b0000000000011111	4..0	38→34
0x12	Output 18 Mask	b0000000000111111	5..0	41→36
0x13	Output 19 Mask	b0000000000011111	4..0	43→39
0x14	Output 20 Mask	b0000000001111111	6..0	47→41
0x15	Output 21 Mask	b0000000001111111	6..0	50→44
0x16	Output 22 Mask	b0000000011111111	7..0	54→47
0x17	Output 23 Mask	b0000000011111111	7..0	58→51
0x18	Output 24 Mask	b0000000001111111	6..0	61→55
0x19	Master OR 1 Mask 63..48	b1111111111111111	15..0	64→49
0x1A	Master OR 1 Mask 47..32	b1111111111111111	15..0	48→33
0x1B	Master OR 1 Mask 31..16	b1111111111111111	15..0	32→17
0x1C	Master OR 1 Mask 15..0	b1111111111111111	15..0	16→1
0x1D	Master OR 2 Mask 63..48	b1111111111111111	15..0	64→49
0x1E	Master OR 2 Mask 47..32	b1111111111111111	15..0	48→33
0x1F	Master OR 2 Mask 31..16	b1111111111111111	15..0	32→17
0x20	Master OR 2 Mask 15..0	b1111111111111111	15..0	16→1
0x21	Master OR 3 Mask 63..48	b1111111111111111	15..0	64→49
0x22	Master OR 3 Mask 47..32	b1111111111111111	15..0	48→33
0x23	Master OR 3 Mask 31..16	b1111111111111111	15..0	32→17
0x24	Master OR 3 Mask 15..0	b1111111111111111	15..0	16→1
0x25	Master OR 4 Mask 63..48	b1111111111111111	15..0	64→49
0x26	Master OR 4 Mask 47..32	b1111111111111111	15..0	48→33
0x27	Master OR 4 Mask 31..16	b1111111111111111	15..0	32→17
0x28	Master OR 4 Mask 15..0	b1111111111111111	15..0	16→1
0x29	Force Watchdog Timeout	N/A	N/A	N/A

Register Format

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register																
Status	--	--	--	--	--	--	--	--	--	--	3.3	2.5	--	BO	WD	PO
All Others	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Notes:
"--" = Unused bit read as 0, ignored when written
Any access to register 0x29 will force a watchdog timeout and restore power-up reset conditions.

Bit	If Set	Severity
3.3	3.3V Logic Supply OK	Error if clear
2.5	2.5V Logic Supply OK	Error if clear
PO	Power-On Reset	Normal
BO	Brown-Out Reset	Error if set
WD	Watchdog Reset	Error if set
D	Data	N/A

Serial Communications

Write Command: RR=DDDD\r
Read Command: RR\r
Where: RR = ASCII hex register address; DDDD = ASCII hex data; \r = CR

Write Example:	03=000F\r	(sets register 3 masks bits 3..0 on)
	OK\r\n	(response)
Read Example:	03\r	(reads register 3)
	000F\r\n	(response – mask bits)

Guidelines

- All numbers are represented in ASCII hexadecimal format.
- Register addresses must be exactly two digits and upper-case.
- Data must be exactly four digits and upper-case.
- White spaces are permitted – they are ignored by the microcontroller.
- All transactions must be terminated by CR.
- Write transactions always return "OK" or "ERROR".
- Read transactions return data or "ERROR".
- Invalid addresses return "ERROR".
- All registers can be read.
- A write to a read-only register will return "ERROR".
- A write to the STATUS register clears processor reset status bits. Write data is ignored.
- The STATUS register should be monitored periodically to identify a microcontroller reset or supply regulator failure.

Terminal Block TB1

Pin	Function	To
1	+5V Power	Chassis +5V supply
2	GND	±5V COM / chassis GND
3	-5V Power	Chassis -5V supply

Terminal Block TB2

Pin	Function	To
1	RS-232 Tx (to host)	DB9F:2
2	RS-232 Rx (from host)	DB9F:3
3	GND	DB9F:5