PRODUCT DATA

DVME-621

4-Channel Isolated Power Analog Output Board for VMEbus Computers

FEATURES

- **4 isolated output channels**
- **Voltage mode or current loop**
- **Active mode 160mA loop output**
- **12-bit D/A resolution**
- **Selectable output ranges per channel**
- **For servos, controls, motors**
- **Industrial current loops**

Intended for industrial and medium current test systems, DATEL's model DVME-621 is a four channel power analog output board configured on a 6U VMEbus outline. Up to 100mA is available in voltage mode while current loops may be powered up to 160mA

The DVME-621 is ideal for direct drive of servo amplifiers, small motors, deflection coils, actuators, power amplifiers, lamps, low power heaters and industrial controls. Other applications include robotics, power supply testers, programmable amplifier loads and semiconductor screening systems.

Each output channel features dual isolation from adjacent channels and from the VMEbus. This offers freedom from ground loop problems and provides user safety and equipment protection. The 500V rms isolation is achieved with individual DC/DC power converters for each analog channel. Fast optoisolators buffer digital data and the channel logic is double buffered to eliminate data loading transients.

For maximum flexibility, each channel may be individually selected for current or voltage mode, unipolar or bipolar operations. The voltage output ranges are 0 to +11V or ±11V.

Full scale current ranges are 0 to +160mA or 0 to ±160mA. Analog connections use a single front panel 25-pin connector. For accurate load voltage which is not affected by long power leads, all channels include sense inputs.

The DVME-621 appears as four VME memory locations in 24-bit standard address space. The board will accept 16-bit memory reference instructions in any computer language using any operating system. Data is stable within 11 micro-seconds after data write. User software may read back each channel to verify proper data loading and for board test. Very high speed memory loads may use DMA or block transfers from the host computer.

The DVME-621 uses one VME slot and has a 6U "double height" outline. All power is supplied from the +5V and +12V VMEbus power connections.

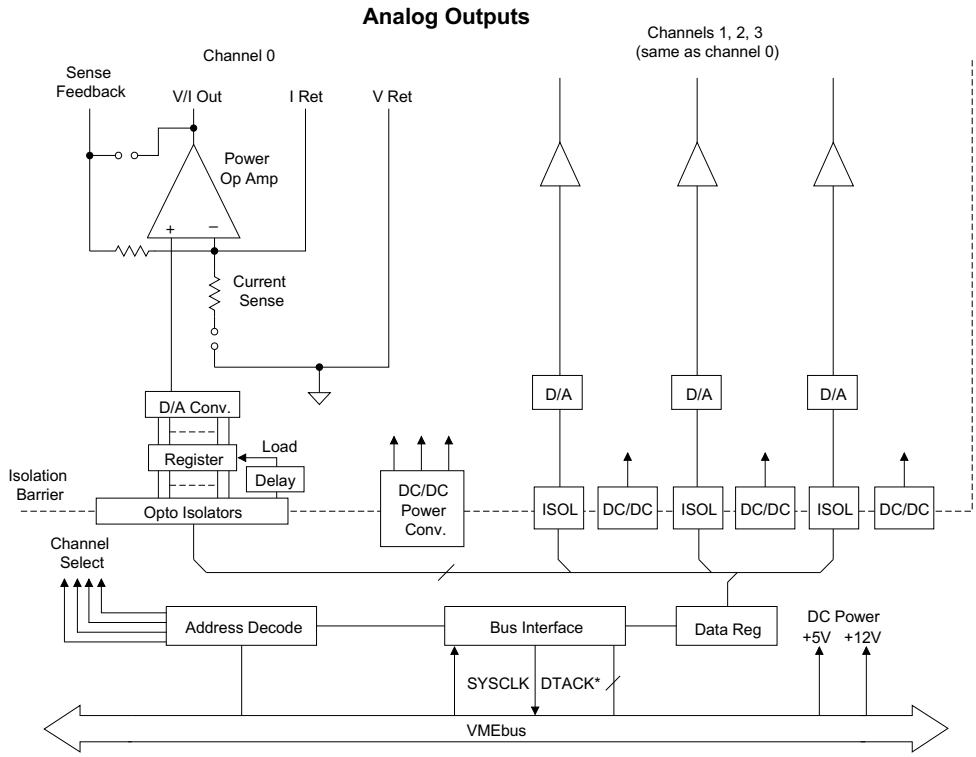


Figure 1. DVME-621 Simplified Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C unless otherwise noted)

ANALOG INPUTS	
Number of Channels	Four
Output Configuration	Single-ended, isolated per (See Technical Note 3) channel
Modes	Current or voltage source, individually selected per channel
Full Scale Voltage Range	0 to +11V or -11 to +11V at 0 to 100 mA max. per channel.
Full Scale Current Range	0 to +160 mA (source only) (See Technical Note 1) or -160 to +160mA (source or sink)
Current Mode Load	3 Ohms min. to 45 Ohms max. for full scale range.
Output Current Limit	±175 mA max.
Output Impedance	500 milliohms max.
Output Protection	Short circuit recovery and open circuit voltage protection.
Overvoltage Protection	±14V max. (no damage). Reactive loads should externally clamp voltage spikes.
Stability	Stable for capacitive loads up to 0.1 µF per channel
D/A Digital Inputs	Double buffered to prevent output transients during data transfers.
D/A Resolution	12 bits resolution, 1 part in 4096. (Bipolar configuration uses 11 data bits and one polarity bit).
Input Data Coding	Straight binary (unipolar) and offset binary (bipolar), right justified.

ISOLATION	
Channel-to-channel Isolation	500V rms sustained
Channel-to-VME bus Isolation	500V rms sustained
Channel-to-channel Leakage	10 µA
Isolation Capacitive Coupling	25 pF per channel to non -isolated ground.

PERFORMANCE	
Monotonicity	No missing codes
Linearity Error	±0.1% of Full Scale Range
Zero Temp. Coefficient	±10 ppm of FSR/°C
Offset Temp. Coefficient	±20 µV/°C (after calibration)
Settling Time to 0.1% of FSR	11 microseconds max.
Slew Rate	1 Volt/microsecond min.

CONFIGURATION	
Channels may be individually selected for current or voltage mode, unipolar or bipolar.	
Data Readback	Any D/A channel may be read back immediately after writing channel data. Only the last channel written may be read back.
Feedback Control	Current and voltage sense feedback control is provided. Remote load sense is included for voltage mode.

VME BUS INTERFACE	
Standards Compliance	IEEE P1014/D1.0
Architecture	Memory mapped in four contiguous words in the bottom of a 256 location memory block. A24:D16 slave.
Memory Mapping	Decodes memory address lines A23 through A01 plus six address modifiers, AM5 - AM0.
Address Modifier Codes	39h or 3Dh, user selectable, "standard I/O" access. (Short I/O is also selectable).
Data Bus	SYSCLK to generate DTACK* with selectable delay. Note: The 16 MHz SYSCLK signal is required.
Interrupts	None

MISCELLANEOUS	
Analog Section Adjustments (See Technical Note 2)	Full scale and zero or offset multi-turn precision potentiometers are provided for each DAC channel. Recalibration is recommended every 90 days in stable conditions.
Analog Connector	One 25-pin DB-25S female mounted on front panel.
VME bus Connector	96-pin DIN connector. Uses P1 only. (P2 is not installed).
Operating Temp. Range	0 to +40°C. Forced cooling is (continuous) required at full power and maximum temperature. Operation may be linearly derated to zero power at +60°C.
Storage Temp. Range	-25 to +85°C
Thermal Shock	±5°C change per minute max.
Relative Humidity	0% to 90% non-condensing
Altitude	0 to 10,000 feet (0-3048m). Forced cooling is required at high altitude and full power output.
Weight	1 Kilogram
Power Supply	+5V, ±% at 3.75A max. +12V, ±5% at 1.5A max. Both are supplied by VME bus.
Power Supply Input Regulation	±0.1% max.
Input Ripple and Noise	50 mV rms below 10MHz
Reflected Switching Noise	45 mA max. reflected back to VME bus from DC/DC converters.
Outline Dimensions	Double height 6U VME outline, one slot wide 9.19"W x 6.3"D x 0.6"H (233,5 x 160 x 15,24mm)

TECHNICAL NOTES

1. All current mode excitation is internally supplied via VME bus. This is also referred to as "active" mode.
2. All DAC input registers are reset to zero or half scale (0800 hex) at power up or VME bus reset depending on the unipolar/bipolar jumper selection. In either case, the output voltage is set at zero volts.
3. Since each output is isolated, they may be connected to either single-ended or differential receivers.

REGISTER MEMORY MAPPING

The memory base address may be selected anywhere using 24-bit addressing up to FFFF00h. 16-bit memory reference word instructions much be used. The registers may be programmed in any sequence and will accept host DMA or block transfer operations for highest speed. In readback mode, only the last register written will be returned. Read a DAC channel immediately after writing it to test each data load. In readback mode, bits 15-12 will always be logic "1".

Address (hex)	Direction	Description
BASE + 0	Write	Load DAC0 data register
BASE + 0	Read	Readback DAC0 data
BASE + 2	Write	Load DAC1 data register
BASE + 2	Read	Readback DAC1 data
BASE + 4	Write	Load DAC2 data register
BASE + 4	Read	Readback DAC2 data
BASE + 6	Write	Load DAC3 data register
BASE + 6	Read	Readback DAC3 data

DATA REGISTER FORMAT

15	14	13	12	11 - - - 0
x	x	x	x	MSB data LSB

On write, "x" bits 15-12 are "don't care". On readback, bits 15-12 will always be logic "1". In bipolar mode, the Most Significant Bit (MSB), bit 11, indicates polarity (0 = negative, 1 = positive).

MEMORY SIZING

Standard I/O addressing — Install E8 (standard)
Short I/O addressing — Install E7

OUTPUT POLARITY

Unipolar: Install E2
Bipolar: Install E1 (standard)

MEMORY BASE ADDRESS SELECTION

The 24-bit base address consists of three bytes. The top two most significant bytes are decoded by two DIP switches, SW1 and SW2. Address bits 7 through 3 should be set to zero. Address bits 2 and 1 are decoded for the DAC data registers. The standard factory setting is FA0000 hex.

Upper byte:

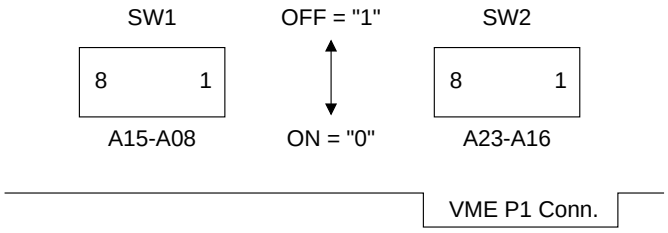
Address bit	A23	A22	A21	A20	A19	A18	A17	A16
DIP Switch SW2	8	7	6	5	4	3	2	1

Lower byte:

Address bit	A15	A14	A13	A12	A11	A10	A09	A08
DIP Switch SW1	8	7	6	5	4	3	2	1

Example: For a Base address of 10 0000h, turn off switch SW2-8 and leave all others on.

Switch location and orientation



OUTPUT RANGE SELECTION

Important: Connect only the jumpers shown. Leave all other jumpers open.

Output Range*	DAC0	DAC1	DAC2	DAC3
±11V Bipolar	J3 2-3 J4 2-3 J2 2-3 J1 2-3 J5 1-2	J8 2-3 J9 2-3 J7 2-3 J6 2-3 J10 1-2	J13-2-3 J14 2-3 J12 2-3 J11 2-3 J15 1-2	J18 2-3 J19 2-3 J17 2-3 J16 2-3 J20 1-2
±160mA Current Loop Bipolar	J3 2-3 J4 2-3 J2 2-1 J1 2-1 J5 3-2	J8 2-3 J9 2-3 J7 2-1 J6 2-1 J10 3-2	J13 2-3 J14 2-3 J12 2-1 J11 2-1 J15 3-2	J18 2-3 J19 2-3 J17 2-1 J16 2-1 J20 3-2
0 to + 11V Unipolar	J3 2-1 J4 2-1 J2 2-3 J1 2-3 J5 1-2	J8 2-1 J9 2-1 J7 2-3 J6 2-3 J10 1-2	J13 2-1 J14 2-1 J12 2-3 J11 2-3 J15 1-2	J18 2-1 J19 2-1 J17 2-3 J16 2-3 J20 1-2
0 to + 160mA Current Loop Unipolar (source only)	J3 2-1 J4 2-1 J2 2-1 J5 3-2	J8 2-1 J9 2-1 J7 2-1 J10 3-2	J13 2-1 J14 2-1 J12 2-1 J15 3-2	J18 2-1 J19 2-1 J17 2-1 J20 3-2

*±10V and 0 to +10V ranges are available on each channel by removing J5, J10, and J20 respectively. Alternate output ranges are available on special order.

ANALOG OUTPUT CONNECTOR (P2)

(connector is shown as viewed from front panel)

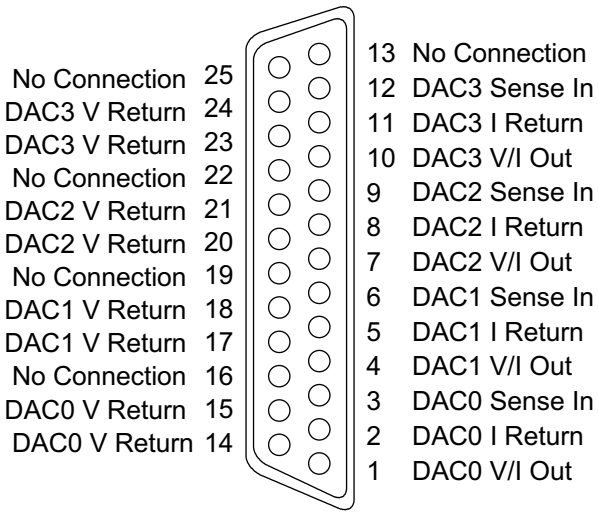


Figure 2. Isolated Analog Output

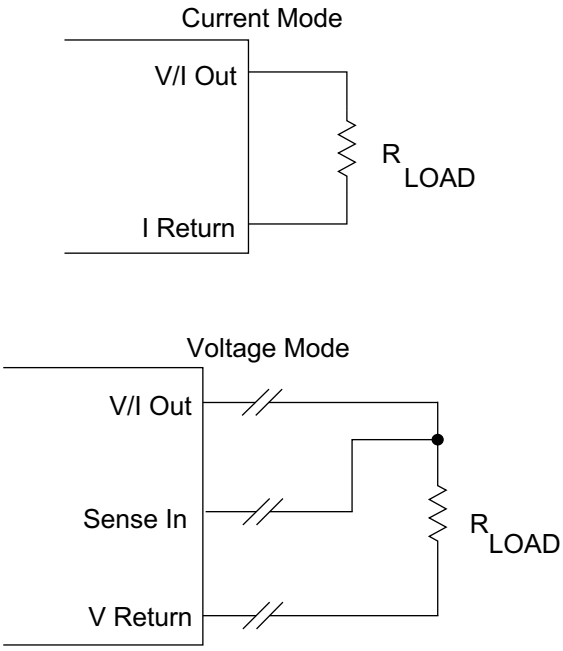


Figure 3. Output Connections

PROGRAMMING EXAMPLE

The DVME-621 requires simple memory reference instructions in any language. 16-bit word operations should be used. Certain systems may require modification using a function which allows accesses to real physical memory from virtual memory. The following example in the "C" language loads the data channels:

```
/* 28jan93 ldc */
#include <stdio.h>
#define BASE 0xFA0000 /* change this for your system!! */

main ( ) {
/* set up pointers to data registers. basptr is the base address of the board. */

unsigned short   *basptr, /*BASE address */
                 *chan0, /* DAC channel 0 */
                 *chan1, /* DAC channel 1 */
                 *chan2, /* DAC channel 2 */
                 *chan3, /* DAC channel 3 */

/* Initialize pointers */

    basptr = ( unsigned short *) BASE;
    chan0 = basptr + 0;
    chan1 = basptr + 2;
    chan2 = basptr + 4;
    chan3 = basptr + 6;

/* Now load -full scale, half scale, + 1 count and +full scale values into 4 channels. */

    *chan0 = 0x0000;  /*-FS */
    *chan1 = 0x0800;  /* half scale */
    *chan2 = 0x801;   /* +1 LSB */
    *chan3 = 0x0FFF;  /* +FS -1 LSB */

} / * end of program */
```

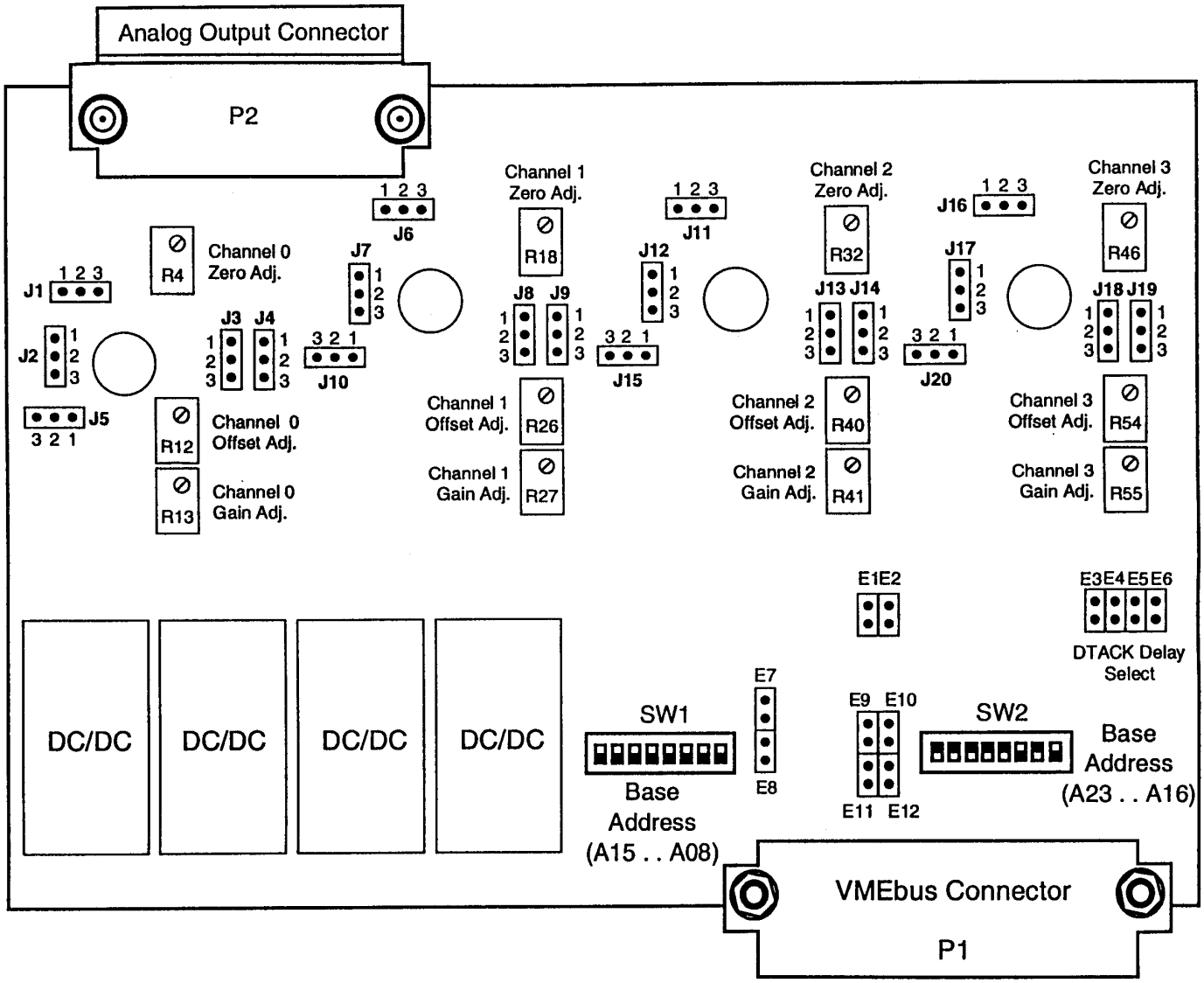
ADDRESS MODIFIER SELECTION

Address Modifier	Function	Jumper
2D hex	Short I/O supervisory access	E9
29h or 2Dh	Short I/O non-privileged or supervisor access	E10
3D hex	Standard I/O supervisor access	E11
39h or 3Dh	Standard I/O non-privileged or supervisor access	E12

ORDERING INFORMATION

MODEL	DESCRIPTION
DVME-621	4-channel VMEbus power output analog board.
DVME-691D	19" rack mount screw terminal adapter and cabling

Alternate output ranges are available on special order.



DVME-621 Board Layout