Technical Information Manual

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MOD. C 894

16 CHANNEL LEADING EDGE DISCRIMINATOR

NPO:
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1. Description

1.1. Functional Description

The CAEN Model C894 is a 16 CHANNEL LEADING EDGE DISCRIMINATOR housed in a single width CAMAC module. The module accepts 16 negative inputs (positive on request) and produces 16 differential ECL outputs with a fan-out of two on two front panel header connectors (a functional block diagram is shown in Fig. 1.1).

The pulse forming stage of the discriminator produces an output pulse whose width is adjustable in a range from 5 ns to 40 ns via CAMAC.

Each channel can work both in Updating and Non-Updating mode according to on-board jumpers position.

The discriminator thresholds are individually settable in a range from -1 mV to -255 mV (1 mV step), via CAMAC through an 8-bit DAC.

VETO and TEST inputs are available on the back panel.

A Current Sum output, available on the front panel, generates a current proportional to the input multiplicity, i. e. to the number of channels over threshold, at a rate of -1.0 mA per hit ±20%.

A "MAJORITY" output on a back panel connector provides a NIM signal if the number of input channels over threshold exceeds the MAJORITY programmed value.

Several C894 boards can be connected in a daisy chain via the Current Sum output: in this case, by switching the Majority logic to “External”, it’s possible to obtain a Majority signal when the number of over threshold channels in the daisy chained modules exceeds a global Majority level.

An "OR" output on a front panel connector provides a global OR of the output channels. The relevant "OR" LED lights up if at least one of the unmasked channels is over threshold.

The module's operations are completely controlled via software for each channel through the CAMAC bus. The most important are:

- Setting of the discriminator thresholds (8 bit data) from -1 to -255 mV.
- Setting pattern of Inhibit; each channel can be turned "ON" or "OFF" by using a mask register.
- Setting output width in a range from 5 to 40 ns.
- Setting of the Majority threshold value.
- Common TEST.

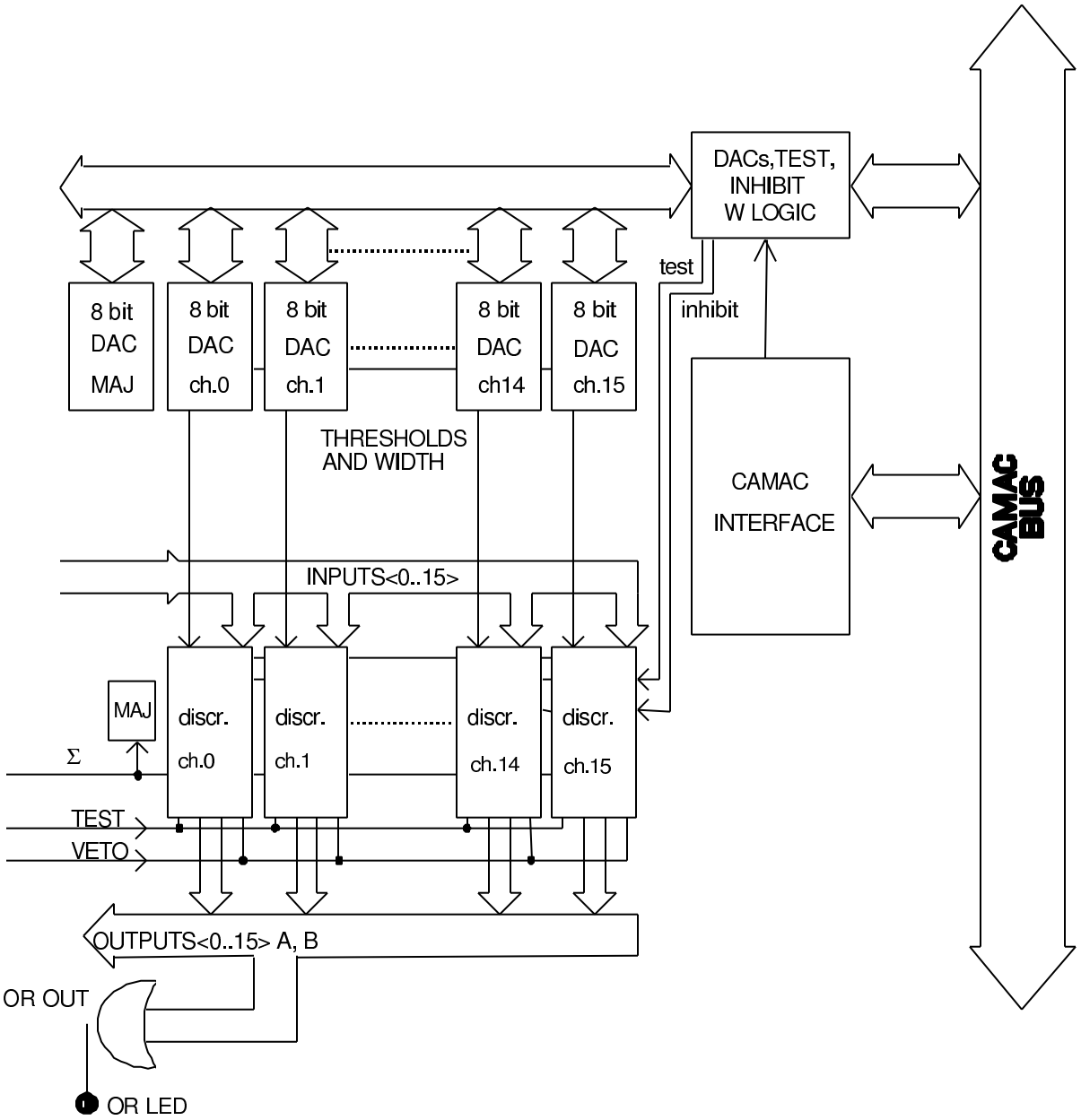


Fig. 1.1: C894 Block Diagram

2. Specifications

2.1. Packaging

1-unit wide CAMAC module.

2.2. External Components

(Refer To Fig. 2.3)

CONNECTORS:

- N. 16, "IN", LEMO 00 type (front panel); input signals connectors from CH0 to CH15.

- N. 1, "CURRENT SUM", LEMO 00 type (front panel); it provides an output current proportional to the output multiplicity, i.e. to the number of input signals over threshold (rate: -1 mA per hit).

- N. 1, "OR", LEMO 00 type (front panel); it is the global OR of the outputs.

- N. 2, "OUTPUT 0...15 A, B", Header 3M 3431-5202 type (front panel), 17+17 pins.

- N. 1, "MAJORITY", LEMO 00 type (rear panel); a standard NIM output signal present when the "CURRENT SUM" output is over a Majority threshold level set via CAMAC.

- N. 2, "VETO", LEMO 00 type (rear panel); two bridged connectors (for daisy chaining). A standard NIM signal is accepted to inhibit all channels simultaneously.

- N. 2, " TEST", LEMO 00 type (rear panel); two bridged connectors (for daisy chaining). A standard NIM pulse allows to trigger all the unmasked channels at once.

DISPLAYS:

- No 1, "OR" green LED; it lights up if at least one output signal is present.

2.3. Internal Components

JUMPERS:
(Refer To Fig. 2.3)

N. 16, for Updating or Non-Updating selection (N.1 jumper for channel).
N. 1, for External or Internal Majority selection.

2.4. Characteristic Of The Signals

INPUTS

Channels: Negative polarity, 50 Ohm impedance; maximum input frequency:

- 140 MHz (updating)
- 80 MHz (non updating)

DC coupling; input range: -5 mV ÷ -5 V; input offset: ±5 mV; reflections: ≤ 4% for 2 ns risetime input pulses.

VETO: standard NIM logic signal, high impedance, 15 ns minimum FWHM. Leading edge of the VETO signal must precede of at least 8 ns the leading edge of the input and overlap completely the input signal (ref. Fig. 2.1).

N.B.: the VETO doesn't act on the TEST input

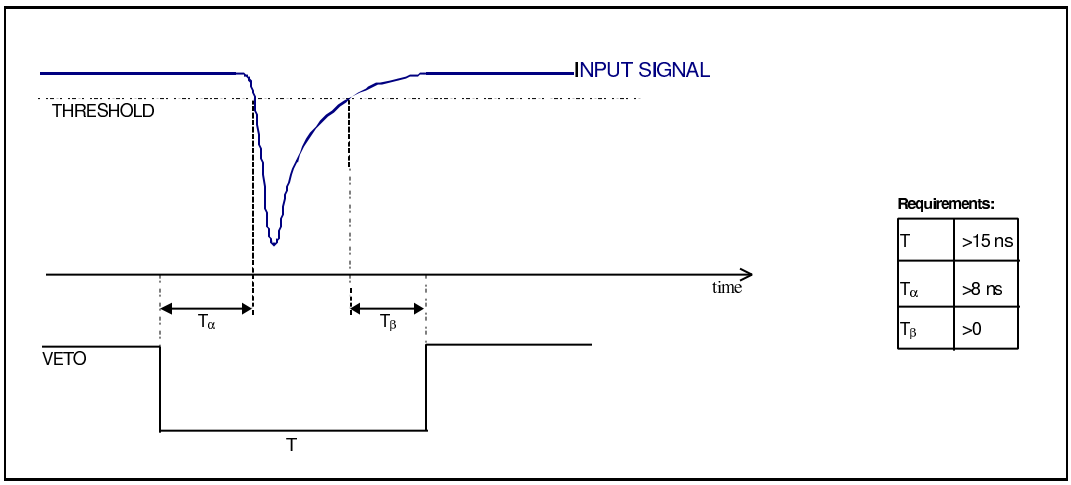


Fig. 2.1: Veto signal

TEST: standard NIM logic signal, high impedance, 5 ns minimum FWHM, 30 MHz maximum input frequency.

OUTPUTS

Outputs: Differential ECL level on 110 Ohm impedance. Pulse width adjustment: from 5±1 ns to 40±5 ns FWHM. Outputs pulses can be programmed either in Updating or Non-Updating mode (Refer to section 3.7). Output pulse rise/fall time: <3 ns.
Input-output delay: 17.5±1.5 ns.

OR: standard NIM logic signal on 50 Ohm; maximum output frequency: 30 MHz; 4 ns rise/fall time.

CURRENT SUM: high impedance with rate of -1 mA per hit (±20%); maximum output frequency: 25 MHz; 8 ns rise/fall time.

MAJORITY: standard NIM logic signal on 50 Ohm.

2.5. *Technical Specifications Table*

Table 2.1: Technical Specifications Table

General	
Packaging	1U-wide CAMAC unit
Power requirements	Refer to § 2.6
Threshold range	-1 mV to -255 mV (1 mV step)
Input Signals	
Inputs Channels	16 inputs negative polarity DC coupling
Inputs Impedance	50 Ω
Reflections	<4% for input pulses of 2 ns risetime
Input range	-5 mV ÷ -5 V
Input offset	±5 mV
Max input frequency	140 Mhz (Updating mode) 80 Mhz (Non Updating mode)
Double Pulse Resolution	7 ns (Updating mode) 12 ns (Non Updating mode)
Test Input	NIM logic signal High impedance Min. FWHM: 5 ns Max. frequency: 30 Mhz
Input /Output delay	17 ± 1.5 ns
Veto Input	NIM logic signal High impedance Min. FWHM: 15 ns

Output Signals	
Outputs	16 ECL outputs with a fan-out of two
Outputs Impedance	110 Ω
Output Width	5±1 ns to 40±5 ns FWHM
Output Rise/Fall Time	<3 ns
Input/Output delay	17.5 ± 1.5 ns
Crosstalk	<47 dB
Majority Output	NIM logic signal 50 Ω impedance
Or Output	NIM logic signal 50 Ω impedance Max. frequency: 30 MHz
Σ Output	-1 mA ± 20% per hit High impedance Max. frequency: 25 MHz

2.6. Power Requirements

Voltage	Current
+ 6 V	600 mA
- 6 V	3.5 A
+ 24 V	70 mA (NB: requires Y2 rail connected in parallel to +6 V rail on CAMAC Crate).
-24 V	40 mA (NB: requires Y1 rail connected in parallel to -6 V rail on CAMAC Crate).

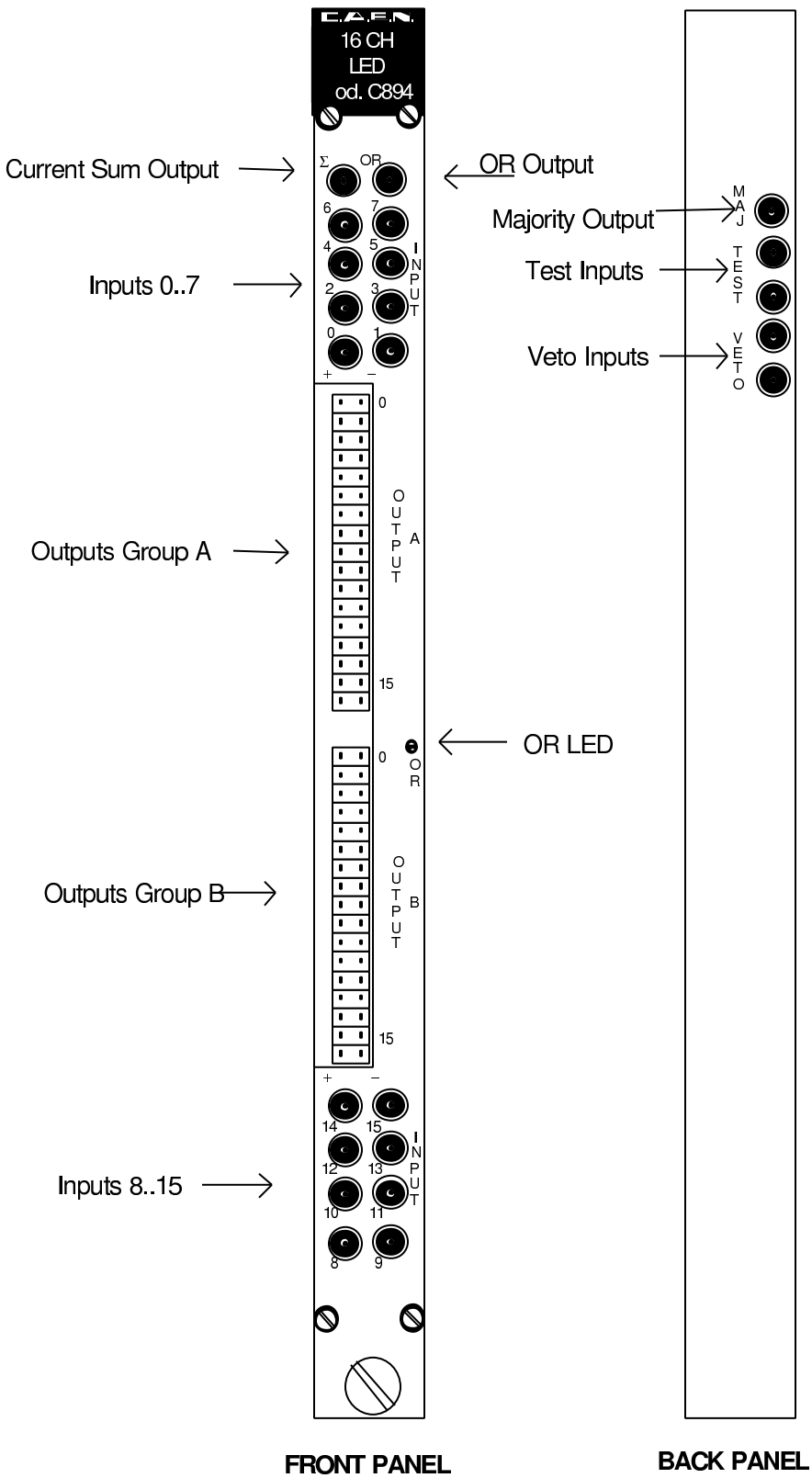


Fig. 2.2: C894 Front and Back Panels

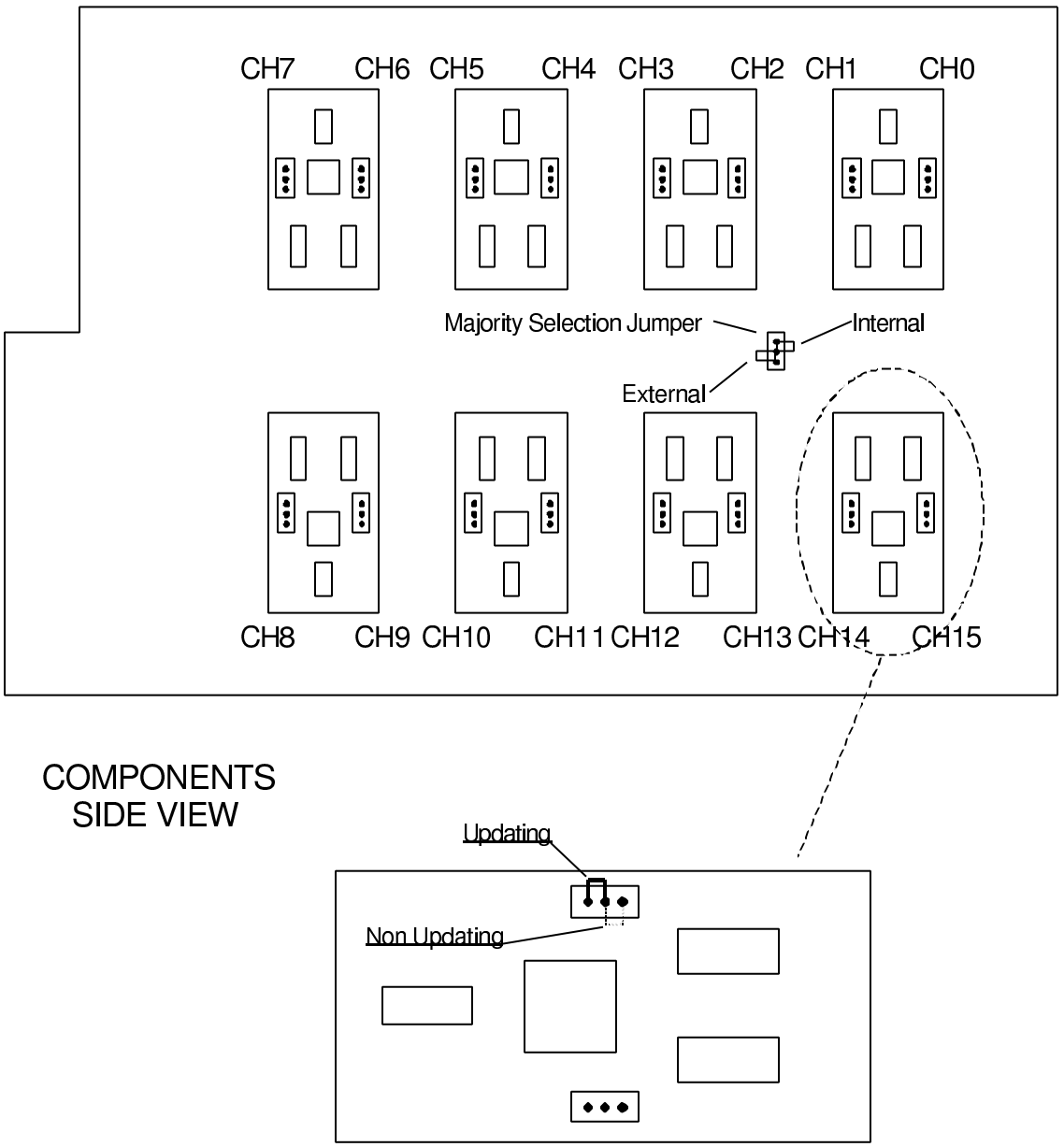


Fig. 2.3: C894 Jumpers Location

3. Operating mode

3.1. Mod. C894 Power-On

At Power-On the contents of all the module's registers are not determined. A setting of the registers must be performed before any other operation.

3.2. Enabling/Disabling of the channel

The User can enable or disable each of the 16 channels via CAMAC by performing a F(17) N A(0) CAMAC function with the Write Lines W1-W16 set to 1 or 0 according to the chosen configuration (16 bit pattern of inhibit). A channel is enabled if the corresponding bit of the Pattern is high.

Example:
If we have a C894 in slot 8 of a crate and we want to disable discriminator channel 2 and 3, we have to perform a CAMAC write function with the following parameters:

Function	F=17
Station Number	N=8
Sub Address	A=0
Write Line	W16 – W1 = 1111111111110011 (bin)

It is also possible to inhibit all channels via a CAMAC I command.

3.3. Test, Veto and Or signals

Some operations can be performed by sending two external NIM signals:

- **TEST**: an input signal sent through this connector triggers all the enabled channels at once. This useful feature allows a check of the module as well as to generate a pattern of pulses suitable to test any following electronics.
- **VETO**: (Ref. Fig.2.1) an input signal sent through this connector allows to inhibit all channels simultaneously. Its leading edge must precede the input leading edge by at least 8 ns and overlap completely the input signal.

  N.B.: the VETO doesn't act on the TEST input

Note: TEST and VETO are high impedance inputs and each one is provided with two bridged connectors for daisy chaining (the chain has to be terminated on 50 Ohm on the last module).

- An OR output connector provides also the logical OR of the output channels. The relevant "OR" LED lights up if at least one of the unmasked channels is over threshold. The OR signal has 4 ns rise/fall time

3.4. Channel Test

It is possible to test all channels by:

- sending a NIM pulse through one of the two "TEST" connectors located on the back panel.
- performing a F(25) N A(0) CAMAC Function.

3.5. Threshold Setting

For each channel of the C894 there is an 8 bit DAC for the threshold setting. The threshold value can be programmed in a range from -1 mV to -255 mV with 1 mV steps (set values: 1 to 255).

In order to write the threshold for each channel, the User must perform an F(16) N A(0-15) CAMAC Function.

Example:
If we have a C894 in slot 8 of a crate and we want to set channel 2 threshold at –10 mV, we have to perform a CAMAC write function with the following parameters:

Function	F=16
Station Number	N=8
Sub Address	A=2
Write Line	W8 – W1 =10 (dec)

3.6. Output Pulse Width Setting

The output pulse width is adjustable from 5 to 40 ns. It's possible to set pulse width for groups of channels (i.e. group from ch. 0 to ch. 7 and group from ch. 8 to ch. 15) and not for each channel independently.

F(18) N A(0)	sets output width for channels 0 to 7
F(18) N A(1)	sets output width for channels 8 to 15

Valid data for the write line are 8 bit integer where:

0	leads to	5 ns
…		
255	leads to	40 ns

with a non-linear interpolation for intermediate values.

Example:
If we have a C894 in slot 8 of a crate and we want to set output pulse width at 5 ns for channel from 8 to 15, we have to perform a CAMAC write function with the following parameters:

Function	F=18
Station Number	N=8
Sub Address	A=1
Write Line	W16 – W1 = 0

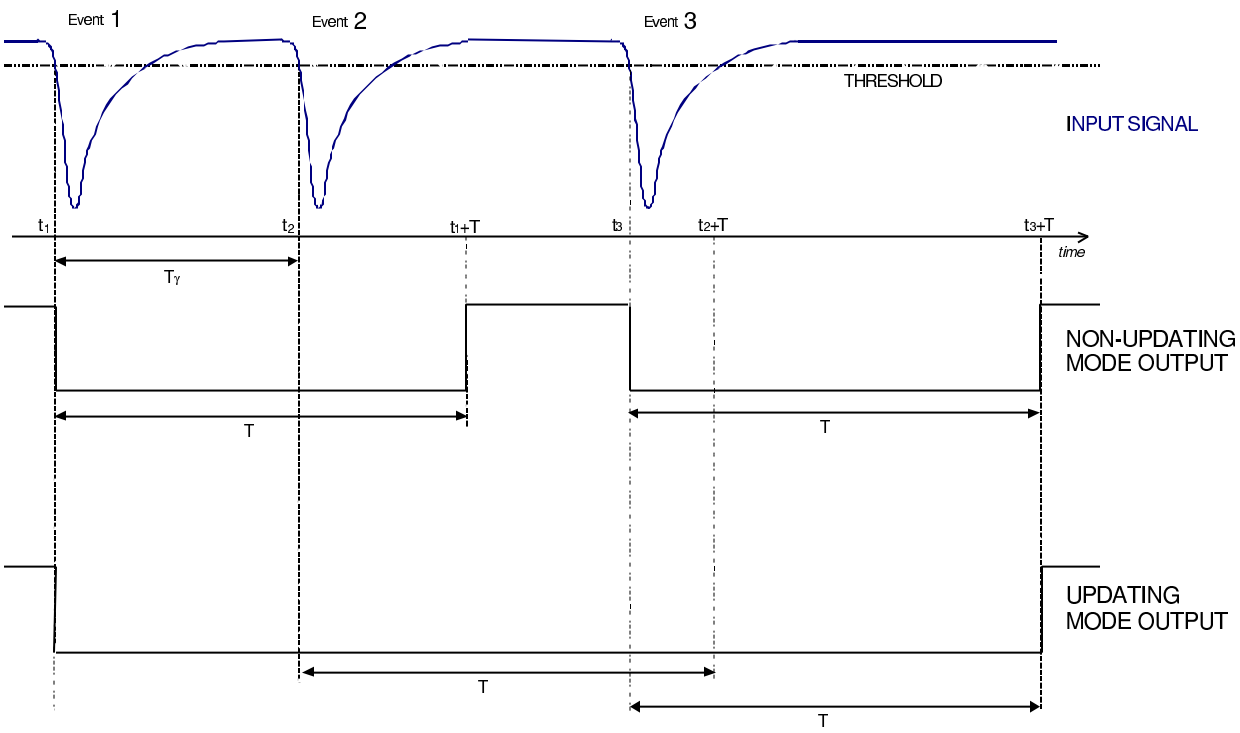
3.7. Updating and Non-Updating Mode Setting

Each channel of C894 may be individually set to provide an Updated (retriggerable) or a Non-Updated (not retriggerable) output. Output modes can be selected through the use of jumpers as shown in Fig 2.2.

Non-Updating output mode: an input pulse over threshold at instant t_1 (event 1 in fig. 3.1) sets the channel output active for the programmed time T (T=5÷40 ns, see § 3.6). Any event over threshold at a generic instant t, where $t_1<t<t_1+T$, will be ignored (will not trigger).

Updating output mode: input pulse over threshold at instant t_1 (event 1 in fig. 3.1) sets output active for the programmed time T (T=5÷40 ns, see § 3.6). Any input event over threshold for $t_e<t_1+T$, will restart the pulse former stage forcing the output to active value until instant t_e+T.

An example of C894 output timing is shown in fig 3.1.



T	5÷40 ns	(programmable)
T_γ min	7 ns	(Updating Mode)
	12 ns	(Non Upd. Mode)

Fig. 3.1: C894 Update/Non-Update mode

3.8. Current Sum signal

The **Current Sum (Σ)** output connector generates a current proportional to the input signal multiplicity, i.e. to the number of channels over threshold, at a rate of -1.0 mA per hit (-50 mV per hit into a 50 Ohm load) ±20%. The Current Sum output has 8 ns rise/fall time.

Note: The Σ output requires a 50 Ohm termination for a correct operation of the Majority logic.

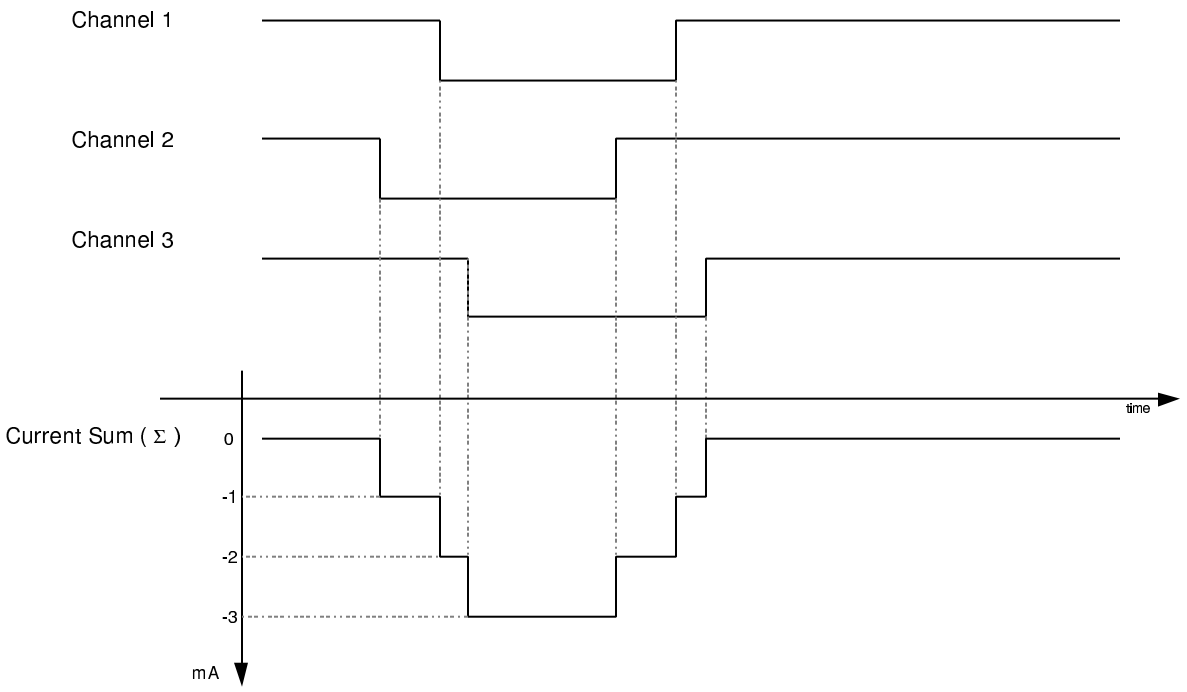


Fig. 3.2: Current Sum signal

3.9. Majority Setting

Majority output provides a NIM signal if the number of over threshold channels exceeds the programmed majority level (MAJLEV).
To set a valid Majority level, the User must perform an F(20) N A(0) CAMAC function with a proper value (MAJTHR) in the WRITE lines W1..W8 (set values: 0 to 255).
MAJTHR can be calculated according to the following relation:

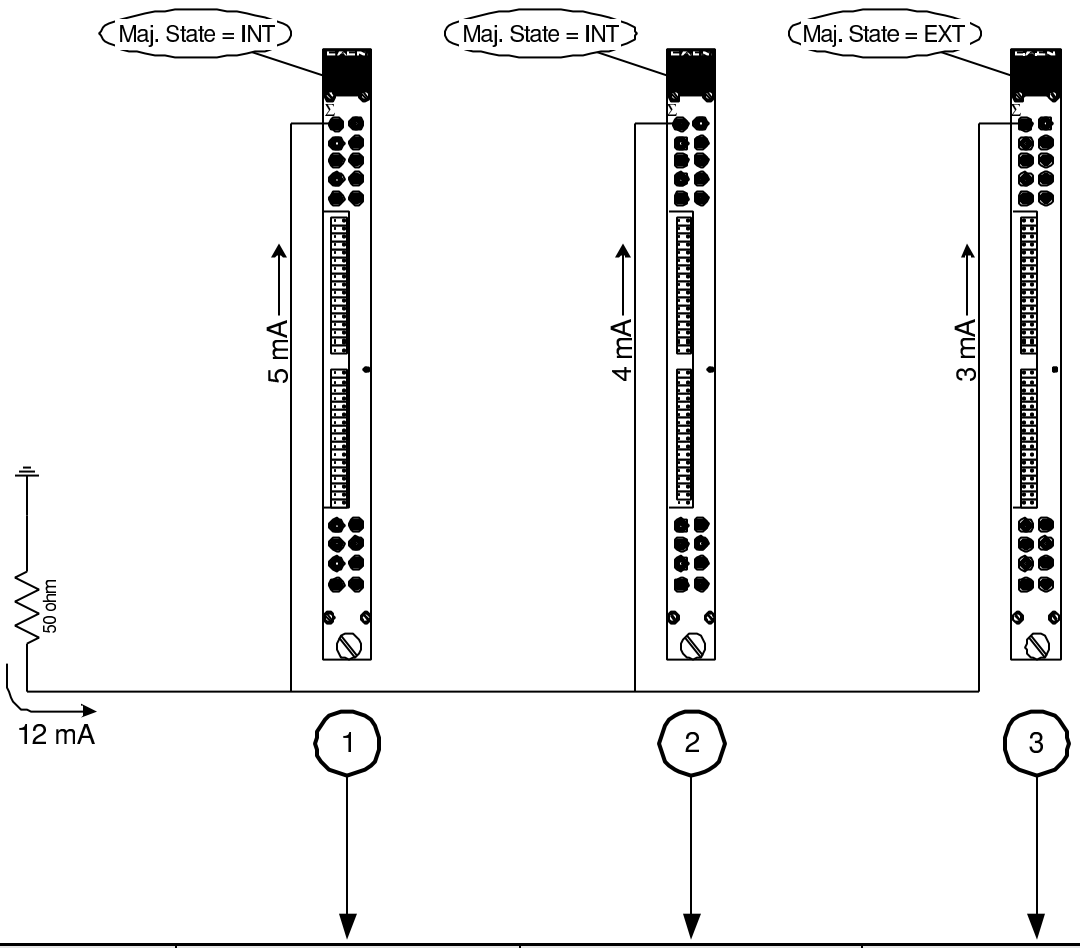
MAJTHR = NINT [(MAJLEV*50 -25)/4], where NINT is the Nearest Integer function.

MAJLEV	MAJTHR	MAJLEV	MAJTHR
1	6	11	131
2	19	12	144
3	31	13	156
4	44	14	169
5	56	15	181
6	69	16	194
7	81	17	206
8	94	18	219
9	106	19	231
10	119	20	244

Table 3.1: Majority Level setting values

The Majority logic can be switched from an "Internal" to an "External" position by means of an internal jumper (see Fig. 2.3).

- **Internal**: With the jumper on the "Internal" position Majority output provides a NIM signal if the number of over threshold channels of the module exceeds or is equal to the programmed majority level (MAJLEV). In this case valid values of MAJLEV are from 1 to 16
- **External**: If desired, more than one module can be connected in daisy chain via the Σ outputs. In this case, by setting the Jumper to the "External" position, the Majority logic will act on the sum of the Σ outputs of the connected modules. So a Majority NIM signal will indicate if the number of over threshold channels in the daisy-chained modules exceed the programmed "External" MAJLEV. (An example with three chained modules is shown in Fig. 3.3). The User must take care of terminating on 50 Ohm the Σ outputs line.



Module Number	1	2	3
Majority State	INT	INT	EXT
Majority Level (MAJLEV)	2 (referred to internal over th. channel)	5 (referred to internal over th. channel)	10 (referred to all over th. channels)
Number of Module's active Channels	5	4	3
Majority Output	ACTIVE (5 > MAJLEV)	NON Active (4 < MAJLEV)	ACTIVE (5+4+3 > MAJLEV)

Fig. 3.3: Example of three C894 in daisy chain

4. Camac Functions

The standard CAMAC functions listed in Table 4.1 allow the User to perform the required control and readout operations on the C894 module.

X response is generated for each valid function.

Q response is generated for each valid function unless otherwise specified.

Table 4.1: Mod. C894 CAMAC Functions

F(16) N A(0..15)	Writes Discriminator Threshold on W1..W8.
F(17) N A(0)	Writes Pattern of Inhibit on W1..W16 (1=enabled).
F(18) N A(0)	Writes Output Width on W1-W8 for channels 0 to 7.
F(18) N A(1)	Writes Output Width on W1-W8 for channels 8 to 15.
F(20) N A(0)	Writes Majority Threshold on W1-W8.
F(25) N A(0)	Common Test.

4.1. F(16) N A(0-15) Function (Write Disc. Threshold)

This CAMAC function writes on 8 bit the threshold values. The threshold values can be programmed (set values: 0 to 255) in a range from -1 mV to -255 mV with 1 mV steps; the channel thresholds are individually settable: Subaddresses 0 through 15 select the desired channel.

4.2. F(17) N A(0) Function (Write Pattern of Inhibit)

This CAMAC function writes the pattern of inhibit (W1..W16), a 16 bit register that contains information on which channels are enabled/disabled (bit=1 ⇒ Ch. enabled). channel 0 refers to W1, and channel 15 refers to W16.

4.3. F(18) N A(0) Function (Write Output Width Ch. 0 to 7)

The output width value is settable with this CAMAC function. W1 through W8 are used to set the chosen value adjustable in a range of 5 ns to 40 ns (set values: 0 to 255). The value is valid for channels 0 to 7. The set value corresponds to the width as follows: 255 leads to an 40 ns value, 0 leads to a 5 ns value, with a non-linear relation.

4.4. F(18) N A(1) Function (Write Output Width Ch. 8 to 15)

The output width value is settable with this CAMAC function. W1 through W8 are used to set the chosen value adjustable in a range of 5 ns to 40 ns (set values: 0 to 255). The value is valid for channels 8 to 15. The set value corresponds to the width as follows: 255 leads to a 40 ns value, 0 leads to a 5 ns value, with a non-linear relation.

4.5. F(20) N A(0) Function (Write Majority Threshold)

With this CAMAC function the ser can select the Majority threshold value (W1..W8) with a resolution of 8 bit (set values: 0 to 255). See § 3.9. for details.

4.6. F(25) N A(0) Function (Common Test)

This CAMAC function generates a test pulse on all output channels.

4.7. I Command (INHIBIT)

This CAMAC command inhibits all channels.