ATLAS NSW Electronics Specifications

Component: VMM3a

VMM is the front end ASIC to be used in the front end electronics readout system of both the Micromegas and sTGC detectors of the New Small Wheels Upgrade project.

Version: v1.0

Abstract

The VMM is a custom Application Specific Integrated Circuit (ASIC). It is intended to be used in the front end readout electronics of both the Micromegas and sTGC detectors of the New Small Wheels Phase I upgrade project. It is being developed at Brookhaven National Laboratory by Gianluigi de Geronimo and his microelectronics design group. It is fabricated in the 130 nm Global Foundries 8RF-DM process (former IBM 8RF-DM). The 64 channels with highly configurable parameters will meet the processing needs of signals from all sources of both detector types:

- Negative anode strip signals from the Micromegas detectors.
- Negative wire-group signals from the sTGC detectors.
- Positive cathode strip signals from the sTGC for precision spatial reconstruction.
- Positive cathode pad signals used in the sTGC trigger.

To accomplish this the VMM has four independent data output paths:

- Precision (10-bit) amplitude and (effective) 20-bit time stamp read out at Level 0 accept.
- A serial out Address in Real Time (ART) synchronized to a 160 MHz clock which is used for the Micromegas Trigger.
- Parallel prompt outputs from all 64 channels in a variety of selectable formats (including a 6-bit ADC) for the sTGC trigger.
- Multiplexed analog amplitude and timing outputs will not be used in the NSW but can be valuable in development and debugging.

Version 3a, to be submitted on September 2017 in a dedicated run, has all the design contains all the features that are needed for the ATLAS NSW upgrade and in addition contains bug fixes form the Version 3 that are described in this document. The device will be packaged in a Ball Grid Array with outline dimensions of $21 \times 21\,\mathrm{mm}^2$.

Revision History

Rev. No.	Proposed Date Approved Date	Description of Changes (Include section numbers or page numbers if appropriate)	Proposed by: author Approved by: author
v1.0	P: 20/08/2017 A:	Initial Draft	**P:** Polychronakos V., Iakovidis G., De Geronimo G. A:

Contents

1 Conventions and Glossary

ADC Analog to Digital Converter.

ART Address in Real Time.

ASIC Application-Specific Integrated Circuit.

BGA Ball Grid Array.

CA Charge Amplifier.

CMOS Complementary Metal Oxide Semiconductor.

DAC Digital to Analog Converter.

DDF Delayed Dissipative Feedback.

DDR Double Data Rate.

DICE Dual Interlocked Cells.

EAR Export Administration Regulations.

ENC Equivalent Noise Charge.

ESD Electrostatic Discharge.

FIFO First In First Out.

LSB Least Significant Bit.

Micromegas Micro Mesh Gaseous Structure.

MO Monitoring Output.

MOSFET Metal Oxide Semiconductor Field Effect Transistor.

MSB Most Significant Bit.

NSW New Small Wheel.

PDO Peak Detector Output.

PtP Pulse at Peak.

PtT Peak to Threshold.

ROC Read Out Controller.

SEU Single Event Upset.

SLVS Scalable Low Voltage Signaling.

SPI Serial Peripheral Interface.

sTGC small strip Thin Gap Chambers.

TAC Time to Amplitude Converter.

TDO Time Detector Output.

TDS Trigger Data Serializer.

TID Total Ionizing Dose.

TMR Triple Modular Redundancy.

ToT Time over Threshold.

TtP Threshold to Peak.

2 Related Documents

The VMM interfaces directly with 3 custom ASICs and indirectly with one. A brief description of the functionality of these ASICs and the relevant printed circuit boards, the specifications documents, as well as links to these document are provided below.

2.1 ASICs other than VMM and related items

1. The ReadOut Controller (ROC) ASIC. It reads data out of up to 8 VMM chips and provides all interface readout control signals:

https://edms.cern.ch/file/1470540/1/NSW_VMM3_ROCReviewFeb2015_PDR_20150507.pdf
https://svnweb.cern.ch/cern/wsvn/NSWELX/ReadOutController/Documentation/VMM3_ROCspecMar2016/VMM3_ROCspec.pdf
https://indico.cern.ch/event/647424/contributions/2630995/attachments/1482889/2300520/ROC_Review_June17_-_ePLL.pdf

2. The Slow Control Adapter (SCA). Used for configuration and monitoring of the VMM: https://espace.cern.ch/GBT-Project/GBT-SCA/default.aspx

3. The Trigger Data Serializer (TDS). It is used to handle the prompt signals (ToT and strips) used in the sTGC trigger:
https://indico.cern.ch/event/327350/contribution/2/attachments/635918/875421/sTGC_Review_largerfigures.pdf
https://indico.cern.ch/event/647424/contributions/2630955/attachments/1482851/2300304/TDS_followup_20170626.pdf

4. The Front End Card with 8 VMM (MMFE-8), is the front end card with 8 VMM chips: (512 channels) used by the Micromegas Detectors https://edms.cern.ch/file/1470529/1/NSW_MMFE-8-Specification-020515_PDR.pdf

5. NSW sTGC FEB Design Note and Specification: the front end card that is designed for the sTGC detectors: (512 channels) used by the Micromegas Detectors https://edms.cern.ch/file/1470532/1/NSW_sTGC_FEB_Design_Review_20150130_PDR.docx

6. The Address in Real Time (ART) ASIC receives synchronously with the BC clock the ART signals from up to 32 VMM, encodes the strip address of those VMM with a hit, appends the BCID and transmits the data to the MM trigger processor: https://edms.cern.ch/file/1472976/1/NSW_ART_ASIC_specs_PDR_2015_2.docx
https://indico.cern.ch/event/647424/contributions/2630940/attachments/1482366/2300256/art_review_june17.pdf

7. The ART Data Driver Card (ADDC) is the PCB housing the ART ASIC and GBT chipset: https://edms.cern.ch/file/1470535/1/NSW_ADDC_document_v1.0_PDR_2_2015.pdf

8. sTGC Analog Requirements for the New Small Wheel VMM3 ASIC : https://edms.cern.ch/file/1536160/1/VMM3_Analog_Requirements_sTGC_EDMS_SpecsDocument_20150814.docx

2.2 VMM Progress reports

In addition there are some critical presentations that show the progress and review of the VMM3:
NSW ASIC Review on 27th of April 2017:
https://indico.cern.ch/event/631131/contributions/2561765/attachments/1450861/2237123/VMM_Update_Apr_2017_fin.pdf
NSW ASIC Review on 26th of June 2017:
https://indico.cern.ch/event/647424/contributions/2630999/attachments/1482862/2300769/VMM3a_status_Jun_2017.pdf

3 Description of the VMM

The VMM is composed of 64 linear front-end channels. A block diagram of one of the identical channels is shown in Figure 1. Each channel integrates a low-noise charge amplifier (CA) with adaptive feedback, test capacitor, and adjustable polarity (to process either positive or negative charge). The input MOSFET is a p-channel with gate area of L × W = 180 nm × 10 mm (200 fingers, 50 µm each) biased at a drain current ID = 2 mA; this corresponds to an inversion coefficient IC ≈ 0.22, a transconductance g_m ≈ 50 mS, and a gate capacitance C_g ≈ 11 pF. The filter (shaper) is a third-order (one real pole and two complex conjugate poles) designed in delayed dissipative feedback (DDF) [1], has adjustable peaking time in four values (25, 50, 100, and 200 ns) and stabilized, band-gap referenced, baseline. The DDF architecture offers higher analog dynamic range, making possible a relatively high resolution at input capacitance much smaller than 200 pF. The gain is adjustable in eight values (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC).

Next to the shapers are the sub-hysteresis discriminators [2] with neighbor enabling logic, and individual threshold trimming, the peak detector, and the time detector. The sub-hysteresis function allows discrimination of pulses smaller than the hysteresis of the comparator circuit. The threshold is adjusted by a global 10-bit Digital to Analog Converter (DAC) and an individual channel 5-bit trimming DAC. The neighbor channel logic forces the measurements of channels neighboring a triggered one, even those channels did not exceed the set threshold. The neighbor logic extends also to the two neighboring chips through bidirectional IO. The peak detector measures the peak amplitude and stores it in an analog memory. The time detector measures the timing using a time-to-amplitude converter (TAC), i.e., a voltage ramp that starts either at threshold crossing or at the time of the peak and stops at a clock cycle of the BC clock. The TAC value is stored in an analog memory and the ramp duration is adjustable in four values (60 ns, 100 ns, 350 ns, 650 ns). The peak and time detectors are followed by a set of three low-power ADCs (a 6-bit, a 10-bit, and a 8-bit), characterized by a domino architecture [3] but of a new concept. These ADC are enabled depending on the selected mode of operation.

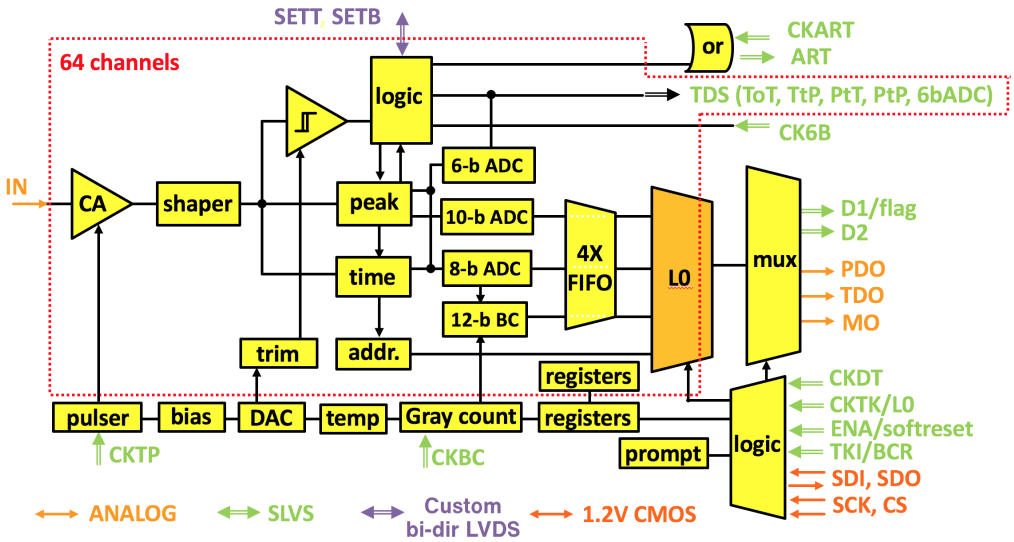

Figure 1: Architecture of VMM3.

The ASIC can operate in either a two phase analog mode (not used in NSW), or in a continuous, simultaneous read/write mode. In the two phase mode data are registered while the VMM is in acquisition mode and then read out, after the system is switched to the read out mode. Acquisition is re-enabled after the readout phase is completed. In continuous mode the simultaneous read/write of data assures dead-timeless operation that can handle rates up to the maximum of 4 MHz per channel (1 MHz expected at the NSW). The ASIC has four independent output data paths:

1. Multiplexed analog amplitude and timing.
2. Digitized (10-bit amplitude, 20-bit vernier time stamp) in a 2-bit (DDR readout) digital multiplexed mode in either a short four-word buffer or with a deeper buffer sufficient for the expected Level-0 latency with the associated control logic.
3. Address in Real Time (ART) used in the Micromegas trigger schema.
4. Direct SLVS-400 outputs of all 64 channels in parallel in one of five selectable formats, used in the sTGC trigger.

The ASIC includes global and acquisition resets and an adjustable pulse generator connected to the injection capacitor of each channel, adjustable with a global 10-bit DAC, and triggered by an external clock. A global threshold generator adjustable with a 10-bit DAC, a band-gap reference circuit, a temperature sensor complete the basic features of the VMM. Finally, it integrates analog monitor capability to directly measure the global DACs, the band-gap reference, the temperature sensor, the analog baseline, the analog pulse, and the channel threshold (after trimming).

The overall connection scheme of these data paths with the rest of the NSW readout and trigger components is shown in Figure 2 and a detailed description of all modes of operation will be described in Section 11.

3.1 Issues addressed from the previous prototype, corner cases simulation and unresolved issues

Several issues have been identified on VMM3. All of them have been addressed on VMM3a. Figure 3 shows the summary of them along with fixes implemented and the simulation status. Essentially all known VMM3 issues have been addressed and simulated for all process corners. There is no known remaining unresolved issue.

4 Signal Processing requirements

Both Micromegas and sTGC chambers of the NSW Upgrade will use the VMM as their front end processing ASIC. In this section the analog requirements for the VMM of both detectors are specified.

4.1 MicroMegas Detectors

The Micromegas signals from the anode strips (negative polarity signals) depending on the chosen gas gain and shaper integration time can be up to a maximum 250 fC, but typically

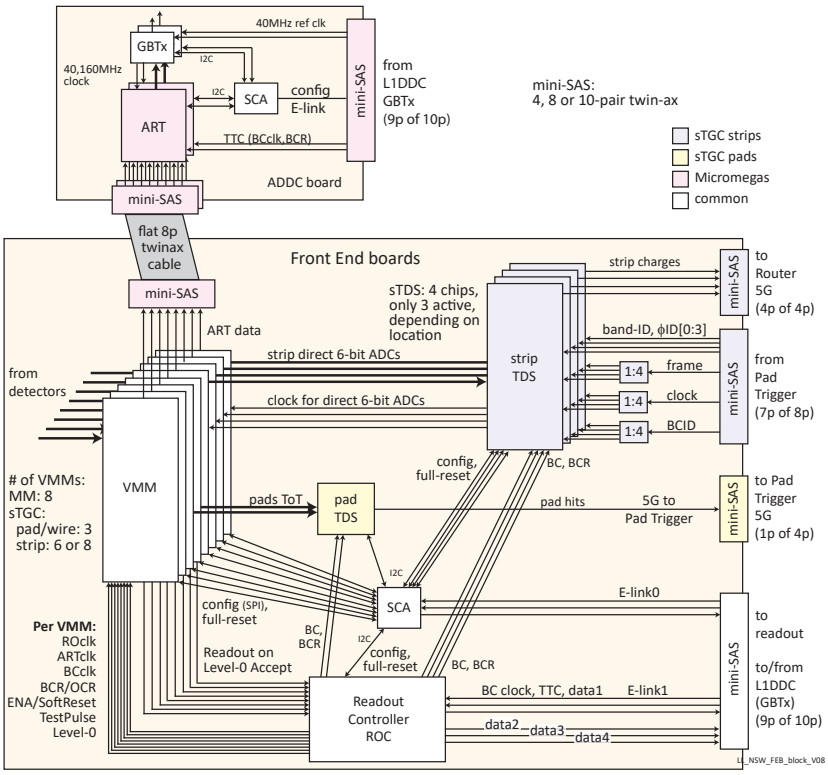

Figure 2: Overall connection diagram of the VMM.

half or even one fourth of the maximum. The simulated input current waveform is shown in Figure 4.

The fast electron current is followed by the positive ion current. One can notice two features. Since the ions are moving in a constant electric field the current is constant. Because of the short distance to the wire mesh (128 µm) the total signal duration is ∼200 ns [4]. In addition to the current waveform and maximum input charge, the other relevant parameter is the electrode (anode strip) capacitance which varies from about 50 to 200-300 pF depending on the length of the strips.

4.1.1 Dynamic Range and Noise Requirements

The dynamic range for the Micromegas detectors is determined by the maximum primary ionization charge, the fraction collected, and the maximum operating gas gain. Assuming a maximum gas gain of 40,000, the dynamic range is 320 fC. The noise is determined by the requirement of single primary electron detection with a threshold 5 times the RMS noise, a gas gain of 30,000, collecting half of the charge, and the maximum possible electrode capacitance of 200 pF. These conditions determine the required noise level to be at 0.5 fC or about 3,000 electrons RMS.

Fix		Detail	Simulation Result
ADC	linearity	• filter ADC bias lines	• periodic non-linearity removed • probability of substantial improvement in yield
	yield	• improve bias matching for uniformity, all ADCs • fix saturation overshoot in output peak current, all	• gain and saturation uniformity strongly improved
Reset		• add soft reset to soft-reset register • merge reset paths in channel discriminator	• soft-reset at ENA low now properly generated • no locking occurs for any configuration, verified
SFM		• add full-mirror to third stage • add two bits (SLH SLXH) for additional high-bias	• no failing channels at all process corners in SFM mode
Baseline	stlc	• remove MA bridge and add MOSCAP for Antenna ratio	• no failing channels at all process corners in 256 MC passes
	yield	• use PMOS bias in second stage of amplifier • increase drive in third stage of shaper	• no failing channels at all process corners in 256 MC passes
Trim DAC		• double driver size in trimming amplifier • improve matching in trim current source	• VMM3a will cover > 32mV at all process corners
Startup		• add soft reset to stop register	• VMM3a won't need startup/register sequence
DRC, LVS		• locals in progress, chip-level queued	

Figure 3: VMM3a: Status of fixes implemented from VMM3 and simulation updates.

4.2 sTGC Detectors

For the sTGC chambers, there are 3 different types of active elements on a detector: strips, wires, and pads. All the three are read out via the VMM. Strips provide the precision coordinate measurement for track reconstruction, wires for the second coordinate, and pads are used for triggering purposes requiring a 3 out of 4 coincidence between the signals of pads in consecutive layers. The wire signals are negative while both the strip and pad signals are positive. Hence the need for the VMM to handle both polarities. A typical simulated current waveform from an sTGC detector is shown in Figure 5. The total charge and the long ion tail impose specific requirements on the processing of the sTGC signals and are outlined below. **However VMM3a simulations and updated sTGC requirements will be presented during the review.**

4.3 Wire Signals

1. The VMM should recover from wire signals of $< Q_w >= 6\,\text{pC}$ within $200\,\text{ns}$.
2. The linearity is not a critical factor here; however it is desirable for the linearity up to $2\,\text{pC}$ to be known in order to apply offline corrections.

4.4 Pad Signals

1. In ADC mode, the VMM should recover from pad signals of $< Q_p >=< Q_w > /2 = 3\,\text{pC}$ within $250\,\text{ns}$.
2. The linearity is not a critical factor here; however it is desirable for the linearity up to $2\,\text{pC}$ to be known in order to apply offline corrections.

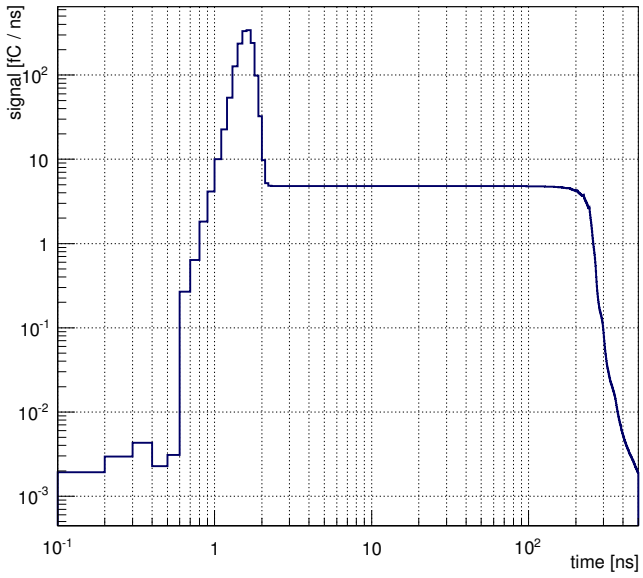

Figure 4: Simulated current induced by the motion of electrons and positive ions during the avalanche formation within the 128 µm amplification region of micromegas detector (the actual input to the VMM is of negative polarity).

3. In direct-timing-only mode (Time-over-Threshold and 6-bit ADC):
   (a) if the pulse charge is less than 6 pC , the dead time shall be 60 ns after the trailing edge of the ToT pulse or 60 ns after the readout of the last bit.
   (b) if the pulse charge is more than 6 pC , the dead time increases with the charge and at 50 pC is expected to reach ≈ 1 µs from the peak.

4.5 Strip Signals

1. The VMM should recover from strip signals of $< Q_s >=< Q_w > /6 = 1$ pC within 200 ns . The factor of 6 comes from the assumption that the signal will be distributed over three strips on average.

2. Linearity within ±2% up to 2 pC is required.

4.6 Input Capacitance and Rate per VMM

1. The capacitance of the largest pad on sTGC detectors will be 2 nF or less, defining the maximum capacitance the VMM must work within the requirements set out in the preceding sections, in particular in terms of dead time and recovery time.

2. The expected/estimated maximum rate at luminosity of 7×10^{34} is 0.8 MHz per VMM channel for pads and 0.9 MHz per VMM channel for strips. An average strip multiplicity of 4.7 is assumed in this, including from neighbor-on mode.

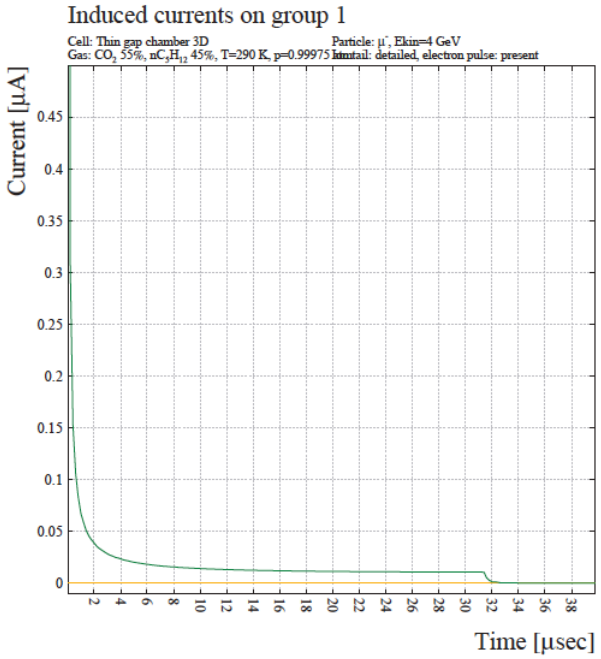

Figure 5: Simulated current induced by the motion of electrons and positive ions in an sTGC detector.

4.7 Input DC Current VMM channel

DC current in the input of a channel should not exceed 100 nA if the current is of the same polarity as the signal, or 1 nA for a DC current of opposite polarity.

4.8 Dynamic Range and Noise Requirements

As mentioned in the previous sections the sTGC signals span a very large range from 1 pC on a given strip to about 50 pC on a pad. The dynamic range for the precision strip measurement is 2 pC . Assuming that one wants to measure 2.5% of this charge with a 2% resolution and a 200 pF electrode capacitance, the required noise level for a 25 ns integration time should be about 1 fC , or 6250 electrons. The noise for the digital signals from the pads with much larger capacitance (up to 2 nF) will be substantially higher, increasing at about 8 electrons per pF.

5 Physical Description of the VMM and Layout recommendations

The VMM is a fully custom ASIC fabricated in the 130 nm Global Foundries 8RF-DM process (former IBM 8RF-DM). In this section the VMM3a is described. It should be noted that the pin assignment and layout are identical to those of the VMM3 version. In Table 3 the Input/ Output signals will be described.

The VMM3a will be packaged in a 400 ball, 1 mm pitch BGA. The device size is $21 \times 21\,\mathrm{mm}^2$ consistent with the pitch of the Micromegas detectors. The VMM3 layout size is $15.308 \times$

307 $8.384\,\mathrm{mm}^2$ and the die size $15.308 \times 8.464\,\mathrm{mm}^2$. The die layout and size of the VMM3 is shown
308 in Figure 6. The ball assignment is shown in Figure 7, and the detailed pin list and their
309 functions in Table 1.

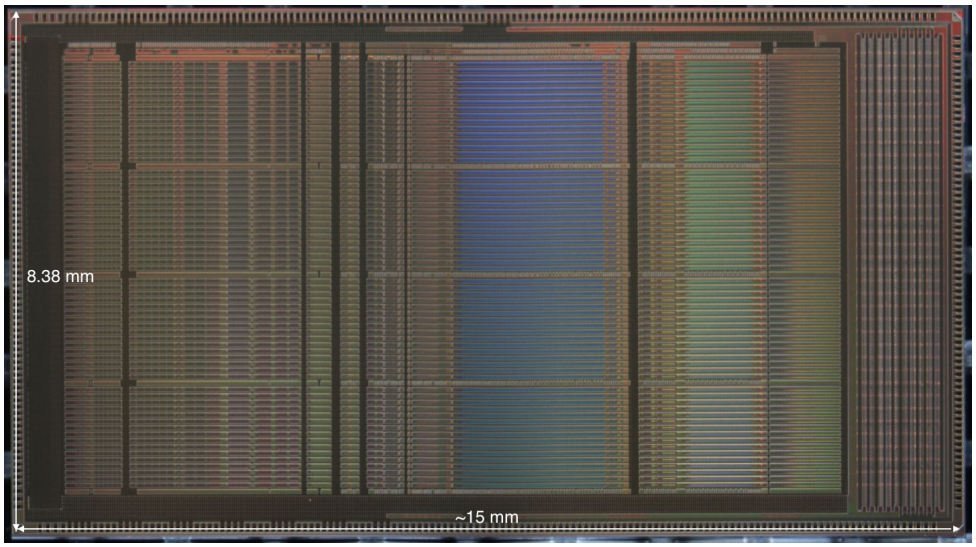

Figure 6: VMM3a die layout

Figure 7: VMM3a pinout (top view)

5.1 Layout recommendations and requirements

User should consult with MMFE8, pFEB, sFEB and VMM designers. The layout has undergone several upgrades and it is still in progress, and there is no comprehensive document at this time.

6 Manufacturer

6.1 Wafer Processing

The VMM will be fabricated in the Global Foundries (former IBM) 130 nm 8RF-DM CMOS process through MOSIS. Because of its size it is more economical to be submitted in a custom dedicated run even for prototypes. The wafers will be thinned to 0.010" (250 µm), diced, inspected, and sorted to waffle packs.

6.2 Packaging

As mentioned in Section 5 the VMM3a will be packaged in a 400 ball BGA with 1 mm pitch. The design of the new substrate will start immediately after the layout is completed in consultation with the groups designing the front end cards, and the packaging house. We are in contact with three new packaging vendors, IMEC, NOVAPACK, and Signetics. All three have agreed to accept the project in spite of the low (by industry standards) volume of 50,000 chips at production.

6.3 Export License Issues

The design includes PROMPT circuit. The appropriate office at BNL has determined that the VMM does not need Export Administration Regulations (EAR) license and, therefore, it can be freely distributed to all of our NSW collaborators.

7 Power

The VMM is designed to operate at a nominal voltage of 1.2 V . It requires four different supplies in order to minimize the contribution to the Equivalent Noise Charge (ENC) of the digital and mixed analog-digital circuits. These four power supplies are:

- **Vddp:** Charge amplifier supply connected to the sources of the p-channel input MOSFETs
- **Vdd:** Powers all other analog circuits
- **Vddad:** Mixed Analog–Digital (ADC)
- **Vddd:** Supplies the digital circuits and SLVS drivers

Table 2 summarizes the requirements and tolerances for the four supplies. The power dissipation depends on the selected functionality and mode of operation. It ranges from 500 mW to 800 mW. For example the SLVS outputs can be disabled when not needed, e.g., in Micromegas operation or the wire readout in the sTGC detectors.

Table 1: Pad/Pin Assignment/Function

BGA Ball Function	
Ball/Pin name	**Description-Comments**
Vdd,Vss	Analog supplies 1.2 V and grounds 0 V – 123 pins total, max current 400 mA
Vddad, Vssad	Mixed-signal (ADC) supplies 1.2 V and grounds 0 V – 16 pins, max current ∼200 mA
Vddd, Vssd	Digital supplies 1.2 V and grounds 0 V 22 pins
Vddp	Charge amplifier supplies 1.2 V 12 pins, max current ∼150 mA
i0-i63	Analog inputs ESD protected
mo	monitor multiplexed analog output
pdo	Peak Detector multiplexed output (not used in NSW).
tdo	Time detector multiplexed analog output (not used by NSW).
SETT	Ch 0 neighbor trigger, Custom LVDS - Bi-directional (chip-to-chip)
CKBC	Bunch Crossing clock, SLVS input, Advances 12-bit Gray-code BC counter
CKTP	Test Pulse Clock, SLVS input
SDI	Configuration SPI data input, 1.2 V CMOS
SDO	Configuration SPI data output, Tristated if chip is not selected , CMOS
CS	Configuration SPI chip select, CMOS
SCK	Configuration SPI clock, CMOS
TKI	BCR/OCR. SLVS input, Token input in analog mode
TKO	Token output SLVS output, Used in analog mode only

ENA	Acquisition start/stop and provides acquisition reset at falling edge:
	• ENA high: acquisition is enabled
	  • internally enabled after 40 ns from ena high
	  • in two-phase (analog) mode is acquisition
	  • in continuous (digital) mode is acquisition and readout

CK6B	6-bit direct output clock, SLVS input
CKTK	Level-0 accept (L0). Token clock (non-NSW use), SLVS input
DT0	First data line in digital DDR mode L0, Data 1 in continuous mode (flag and address in analog mode), SLVS output
DT1	Second data line (first bit) in digital DDR mode L0, Flag and Data 0 line in continuous mode, SLVS output
CKART	Address in Real Time (ART) clock, SLVS input
ART	ART output, SLVS output
CKDT	Data clock SLVS input
ttp0–ttp63	Direct digital outputs, SLVS output
SETB	ch63 neighbor trigger (see SETT)

Table 2: VMM Power Supply Requirements

Supply	Voltage[V]	Ripple	Max Current [mA]
Vddp	$1.2 \pm 5\%$	$< 10\,\mu$V rms , 1–10 MHz	150
Vdd	$1.2 \pm 5\%$	$< 100\,\mu$V rms , 1–10 MHz	400
Vddad	$1.2 \pm 5\%$	$< 100\,\mu$V rms , 1–10 MHz	200
Vddd	$1.2 \pm 5\%$	< 1 mV rms, 1–10 MHz	150

8 Cooling

As mentioned already the VMM power dissipation depends on the features used with a maximum of ~ 1 W . Although not excessive, enclosed in a Faraday cage in the high density environment of the NSW (especially in the case of Micromegas detectors), cooling of the VMM chips is mandatory. A system with water as coolant is being designed by the teams working on the detectors.

The IBM CMOS8RF Design Manual specifies the operating temperature range to be from -55 °C to 125 °C. However device life time degrades rapidly at high temperatures. The case temperature should be kept below 50°C and preferably in the range 30–40 and should be verified and compared to the junction temperature provided by the VMM ASIC. The VMM includes a temperature sensor which can be read out by appropriately programming the monitor output and digitized by the SCA setting (in configuration mode) scmx = 0, sm5–sm0 = 000100 (see Table 6). The die temperature is approximately given by:

$$^{\circ}\mathrm{C} = \frac{725 - V_{\mathrm{sensor}}}{1.85}$$

where V_{sensor} is the temperature sensor reading in mV. The case temperature of a single-chip

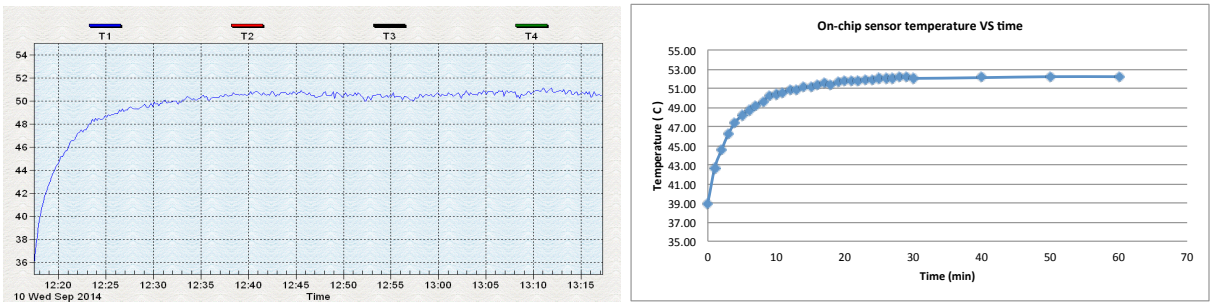

Figure 8: Left plot, the VMM case temperature. Right plot, the junction temperature as a function of time after turn-ON

board was measured from turn ON until thermal equilibrium and was compared with the die temperature. The results are shown in Figure 8. The difference of about 2 °C is consistent with the typical junction to case thermal resistance for BGA devices of similar size, $\sim 1\,^{\circ}$C/W.

9 Input and Output

The input and output connections of the VMM are shown in Table 3. It describes the name of the signal and BGA ball address, the connection destination and direction, the electrical specification and a short description.

The single-ended signals are 1.2 V CMOS. The SLVS signals conform to the SLVS-400 JEDEC standard.

The *sett, setb* signals which, are used for the inter-chip communication of the neighbor logic, are custom bi-directional LVDS signals.

10 Detailed Functional Description and Specifications

As mentioned already, the VMM has four independent data paths and can operate in one of two modes, two-phase (analog) and continuous (digital). Configuration of the ASIC is yet another mode. In the following sections these modes and the relevant specifications will be described in detail.

10.1 Configuration Process

The ASIC can be put in configuration mode by having the *ena* signal low and the *cs* low. When in the configuration mode, the ASIC registers are accessible through the SPI clock *sck* and the data inputs *sdi*. The data transmitted are shifted at the falling edge of *sck* in groups of 96-bits and latched when the *cs* is high. The contents of the configuration register is available at the *sdo* output for daisy-chain configuration. For the NSW, up to 8 VMM devices will be mounted on a front end card and they will be individually configurable. In this mode there are common data input, data output, clock buses and individual chip select pins. For this reason if a VMM is not selected its configuration data output, *sdo*, is tri-stated. The timing diagram of the configuration of up to 8×VMMs is shown in Figure 9.

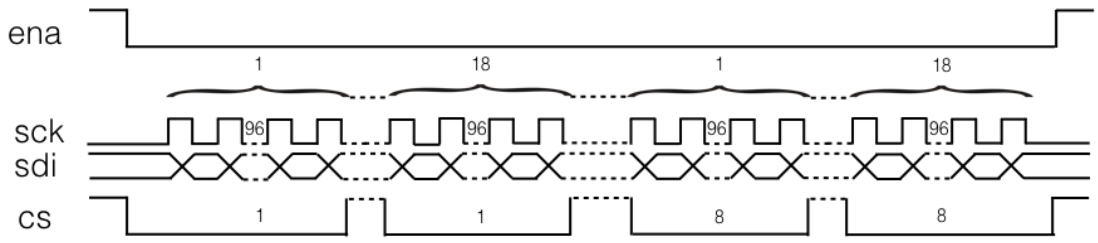

Figure 9: Configuration timing diagram of 8×VMMs.

The configuration is 18 × 96-bits of which 2 × 96-bits are the global registers and the rest are channel registers. Each of the 64 channels has a 24-bit configuration. The list of registers is shown in Tables 6,5. The sequence of registers to be written is global bank-1, channel registers, global bank-2. The first bit to write is the last bit of global bank-2 and the last bit to write is the global bank-1 first bit. The sequence is shown in Table 4.

Table 3: Input and Output Signals of the VMM3a.

Name, Position	**Connection**	**In, Out or I/O**	**Type of Signal or Max/Min**	**Description**
sett A19-20	VMM	I/O	Custom LVDS Bi-directional	Channel 0 force-neighbor signal
setb Y19-20	VMM	I/O	Custom LVDS Bi-directional	Channel 63 force-neighbor signal
ckbc (BCclk) C15-16	ROC	In	SLVS	Bunch crossing clock of 40 MHz / External trigger signal
cktp (Test Pulse) B15-16	ROC	In	SLVS	Test pulse clock
cktk (Level-0) D13-14	ROC	In	SLVS	Token clock / L0 (digital NSW mode)
ckdt (ROclk) E15-16	ROC	In	SLVS	Data clock
ckart (ARTclk) D19-20	ROC	In	SLVS	ART clock
sdi B17	SCA	In	CMOS	Configuration data input
sdo B18		Out	CMOS	Configuration data output (not used, HiZ state in NSW)
cs B19	SCA	In	CMOS	Chip Select, active low
sck B20	SCA	In	CMOS	Input SPI clock
t0-t63 E17-W20	TDS	Out	SLVS	Direct digital outputs
mo C9	SCA	Out	0-1 V	Analog output for calibration
tki (BCR/OCR) C13-14	ROC	In	SLVS	Token input (an. mode) / (BCR-OCR) / acceptance window in non-L0 cont. mode
tko B13-14		Out	SLVS	Token output (analog mode, not used in NSW)
ena (ENA/Soft Reset) C17-18	ROC	In	SLVS	Acquisition start/stop
ck6b C19-20	TDS	In	SLVS	6-bit ADC Clock
art E13-14	ART2GBT	Out	SLVS	Address in Real Time
data0 D15-16	ROC	Out	SLVS	data line
data1 D17-18	ROC	Out	SLVS	data line first bit, flag in cont.

Table 4: Sequence of Configuration Registers of the VMM3.

Register Type	**Sequence**
global registers - first bank	sp sdp sbmx sbft sbfp sbfm slg sm5:sm0 scmx sfa sfam st1:0 sfm sg2:0 sng stot sttt ssh stc1:0 sdt9:0 sdp9:0 sc010b:sc110b sc08b:sc18b sc06b:sc26b s8b s6b s10b sdcks sdcka sdck6b sdrv stpp res00 res0 res1 res2 res3 slvs s32 stcr ssart srec stlc sbip srat sfrst slvsbc slvstp slvstk slvsdt slvsart slvstki slvsena slvs6b sL0enaV slh slxh stgc nu nu nu nu nu reset reset
channel register (64×)	sc sl st sth sm smx sd0:sd4 sz010b:sz410b sz08b:sz38b sz06b:sz26b nu
global registers - second bank	nu0:30 nskipm_i sL0cktest sL0dckinv sL0ckinv sL0ena truncate_i0:5 nskip_i0:6 window_i0:2 rollover_i0:11 l0offset_i0:11 offset_i0:11 nu0:7

Table 5: Channel Configuration Registers of the VMM.

Channel bits (defaults are 0)	**Description**
sc [0 1]	large sensor capacitance mode ([0] <∼200 pF , [1] >∼200 pF)
sl [0 1]	leakage current disable [0=enabled]
st [0 1]	300 fF test capacitor [1=enabled]
sth [0 1]	multiplies test capacitor by 10
sm [0 1]	mask enable [1=enabled]
sd0-sd4 [0:0 through 1:1]	trim threshold DAC, 1 mV step ([0:0] trim 0 V , [1:1] trim -29 mV)
smx [0 1]	channel monitor mode ([0] analog output, [1] trimmed threshold))
sz010b, sz110b, sz210b, sz310b, sz410b	10-bit ADC offset subtraction
sz08b, sz18b, sz28b, sz38b	8-bit ADC offset subtraction
sz06b, sz16b, sz26b	6-bit ADC offset subtraction

Table 6: Global Configuration Registers of the VMM3.

Global bits (defaults are 0)	**Description**
sp	input charge polarity ([0] negative, [1] positive)
sdp	disable-at-peak
sbmx	routes analog monitor to PDO output
sbft [0 1], sbfp [0 1], sbfm [0 1]	analog output buffers, [1] enable (TDO, PDO, MO)
slg	leakage current disable ([0] enabled)
sm5-sm0, scmx	monitor multiplexing. • Common monitor: scmx, sm5-sm0 [0 000001 to 000100], pulser DAC (after pulser switch), threshold DAC, band-gap reference, temperature sensor) • channel monitor: scmx, sm5-sm0 [1 000000 to 111111], channels 0 to 63
sfa [0 1], sfam [0 1]	ART enable (sfa [1]) and mode (sfam [0] timing at threshold, [1] timing at peak)
st1,st0 [00 01 10 11]	peaktime (200, 100, 50, 25 ns)
sfm [0 1]	enables dynamic discharge for AC coupling ([1] enable)
sg2,sg1,sg0 [000:111]	gain (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC)
sng	neighbor (channel and chip) triggering enable
stot [0 1]	timing outputs control 1 (s6b must be disabled) • stpp,stot[00,01,10,11]: TtP,ToT,PtP,PtT • TtP: threshold-to-peak • ToT: time-over-threshold • PtP: pulse-at-peak (10ns) (not available with s10b) • PtT: peak-to-threshold (not available with s10b)
sttt [0 1]	enables direct-output logic (both timing and s6b)
ssh [0 1]	enables sub-hysteresis discrimination
stc1,stc0 [00 01 10 11]	TAC slope adjustment (60, 100, 350, 650 ns)
sdt9-sdt0 [0:0 through 1:1]	coarse threshold DAC
sdp9-sdp0 [0:0 through 1:1]	test pulse DAC
sc010b,sc110b	10-bit ADC conv. time (increase subtracts 60 ns)
sc08b,sc18b	8-bit ADC conv. time (increase subtracts 60 ns)
sc06b, sc16b, sc26b	6-bit ADC conversion time
s8b	8-bit ADC conversion mode
s6b	enables 6-bit ADC (requires sttt enabled)
s10b	enables high resolution ADCs (10/8-bit ADC enable)
sdcks	dual clock edge serialized data enable
sdcka	dual clock edge serialized ART enable
sdck6b	dual clock edge serialized 6-bit enable
sdrv	tristates analog outputs with token, used in analog mode
stpp [0 1]	timing outputs control 2
slvs	enables direct output IOs
stcr	enables auto-reset (at the end of the ramp, if no stop occurs)
ssart	enables ART flag synchronization (trail to next trail)

Table 6 (continued)

Global bits (defaults are 0)	Description
s32	skips channels 16-47 and makes 15 and 48 neighbors
stlc	enables mild tail cancellation (when enabled, overrides sbip)
srec	enables fast recovery from high charge
sbip	enables bipolar shape
srat	enables timing ramp at threshold
sfrst	enables fast reset at 6-b completion
slvsbc	enable slvs 100 Ω termination on ckbc
slvstp	enable slvs 100 Ω termination on cktp
slvstk	enable slvs 100 Ω termination on cktk
slvsdt	enable slvs 100 Ω termination on ckdt
slvsart	enable slvs 100 Ω termination on ckart
slvstki	enable slvs 100 Ω termination on cktki
slvsena	enable slvs 100 Ω termination on ckena
slvs6b	enable slvs 100 Ω termination on ck6b
sL0enaV	disable mixed signal functions when L0 enabled
reset reset	Hard reset when both high
sL0ena	enable L0 core / reset core & gate clk if 0
l0offset_i0:11	L0 BC offset
offset_i0:11	Channel tagging BC offset
rollover_i0:11	Channel tagging BC rollover
window_i0:2	Size of trigger window
truncate_i0:5	Max hits per L0
nskip_i0:6	Number of L0 triggers to skip on overflow
sL0cktest	enable clocks when L0 core disabled (test)
sL0ckinv	invert BCCLK
sL0dckinv	invert DCK
nskipm_i	magic number on BCID - 0xFE8
slh, slxh	configurable feedback currents (factor 10x, 100x respectively)
stgc	extreme charge handling compensation

10.2 Two-Phase Analog Mode

In two-phase (analog) mode (bit *s10* low), which is the mode originally implemented in the VMM1, the ASIC operates in two separate phases: acquisition with *ena* high and readout with *ena* low. During the acquisition phase the events are processed and stored in the analog memories of the peak and time detectors. As soon as a first event is processed, a flag is raised at the digital output *data0*. Once the acquisition is complete the ASIC can be switched to the readout phase and the readout proceeds injecting a token at the token input *tki*. The first set of amplitude and time voltages is made available at the analog outputs *pdo* and *tdo*. Analog buffers can be enabled using the bits *sbfp* and *sbft*. The address of the channel is serialized and made available at the output *data0* using six data clocks. The next channel is read out

by advancing the token with the token clock. The token is sparse, passed only among those channels with valid events. If, after the token clock occurs, the *data0* goes low, the readout is complete and the token is routed to the output *tko* for the readout of the next chip. This allows a daisy-chained readout with a single token input. Figure 10 shows the complete timing diagram of the analog mode operation.

This mode will not be used in the NSW, but is being left in subsequent versions as an option. It should be noted that the two trigger paths, the 64-channel parallel outputs as well as the ART stream are active in this mode as well. The flag of the ART can be used, for example, as a fast "OR" of all 64-channels whereas the prompt parallel outputs can be used to implement more sophisticated trigger algorithms. If not needed, the parallel SLVS outputs can be disabled with significant savings in power consumption and increased noise immunity from digital activity.

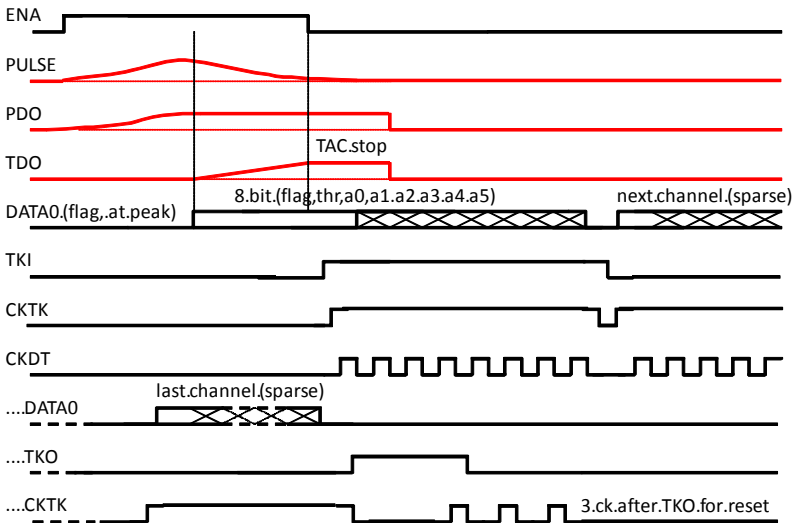

Figure 10: Data Readout with PDO,TDO and external ADC (2-phase mode)

10.3 Continuous (digital) Mode

In the continuous mode (bit *s10* high) the 64 channel digital outputs ttp0-ttp63 are activated when *sttt* is high and provide one of four different timing pulses: time-over-threshold (ToT), threshold-to-peak (TtP), peak-to-threshold (PtT), or a 10 ns pulse occurring at peak (PtP), and can be set using the global bits *stot* and *stpp*. The channel self resets at the end of the timing pulse, thus providing continuous and independent operation of all 64-channels. Alternatively, if the bit *s6b* is set high, the peak detector converts the voltage into a current that is routed to the 6-bit ADC. The 6-bit ADC provides a low-resolution A/D conversion of the peak amplitude in a conversion time of about 25 ns from the peak time. The conversion time and the baseline (zeroing) are adjustable using the global bit set *sc6b* (the conversion time is the number of data clocks set by the *sc6b* bits) and the channel bit set *sz6b* respectively. The serialized 6-bit data is made available at the channel output immediately after an event flag which occurs at the peak time. The flag is lowered at the next clock cycle of the data clock, and the 6-bit ADC data is shifted out after that, either at each clock cycle or at each clock edge of the data clock

depending on the global bit *sdck6b*. The channel reset occurs after the last bit has been shifted out.

In this mode the peak and time detectors convert the voltages into currents that are routed to the 10-bit ADC and 8-bit ADC respectively. The 10-bit ADC provides a high resolution A/D conversion of the peak amplitude in a conversion time of about 200 ns from the occurrence of the peak. The conversion time and baseline (zeroing) are adjustable using the global bit set *sc10b* (the conversion time is a 200 ns base plus a 60 ns increment for the MSB and LSB phases, set by the *sc10b* bits) and the channel bit set *sz10b* respectively. The 8-bit ADC provides the A/D conversion of the timing (measured using the TAC) from the time of the peak or the threshold to a stop signal. The TAC stop signal occurs at a next clock cycle of a shared 12-bit Gray-code counter which is incremented using the external clock signal BC. The counter value at the TAC stop time is latched into a local 12-bit memory, thus providing a total of 20-bit deep timestamp with a nanosecond resolution. The conversion time and baseline (zeroing) are adjustable using the global bit set *sc8b* (the conversion time is a 100 ns base plus a 60 ns increment for the MSB and LSB phases, set by the *sc8b* bits) and the channel bit set *sz8b* respectively. The channel is reset once both the 8-bit and 10-bit conversions are complete (or earlier if the *sfrst* is high) and the digital values are latched in digital memories. Thus, in continuous (digital) mode a total of 38-bits are generated for each event. The first bit is used as a readout flag, the second is the threshold crossing indicator (allows discrimination between above-threshold and neighbor events). Next is a 6-bits word for the channel address, followed by 10-bits associated with the peak amplitude, and 20-bits associated with the timing. The digital output bit assignment is summarized also on the table of Figure 1. At this point two modes should be distinguished. The non-ATLAS mode described in the following subsection. The ATLAS-specific readout and trigger modes to be used in NSW will be described in Section 11.

10.3.1 Non-ATLAS Continuous Mode

In this mode, the 38-bit word is stored in a 4-event deep derandomizing FIFO (there is one such FIFO per channel) and it is read out using a token-passing scheme where the token is passed first-come first-serve only among those FIFOs that contain valid events. The first token is internally generated as needed (*tki* becomes an acceptance window, if high at least for one *ckbc* then the event is processed otherwise discarded, *tko* IO is not used) and advanced with the token clock. The data in the FIFOs is thus sequentially multiplexed to the two digital outputs *data0* and *data1*. The second output *data1* is also used as a flag, indicating that events need to be read out from the chip. The external electronics releases a sync signal using the token clock as well (i.e. the token clock provides both advancement and data output synchronization), after which the 38-bit data is shifted out in parallel to the *data0* and *data1* outputs using either 19 clock cycles or 19 clock edges of the external data clock, depending on the global bit *sdcks*. The timing diagram relevant to this mode is shown in Figure 11

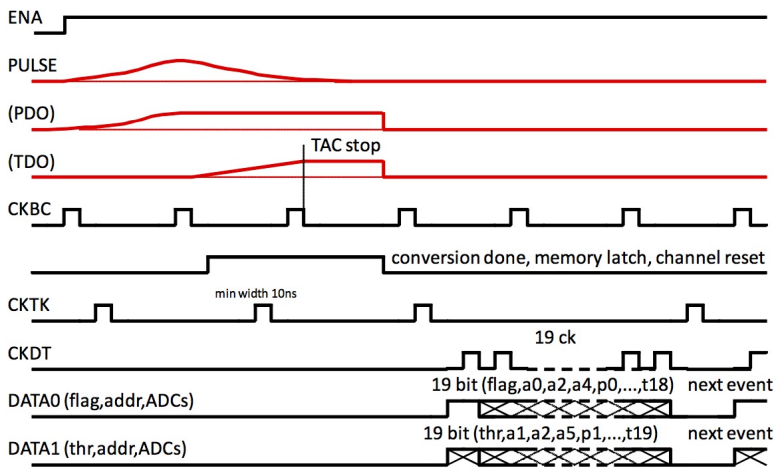

Figure 11: Data Readout with ADCs (continuous mode, 1 bit/ck).

11 NSW-specific Readout

For the NSW the readout requirements are significantly more complex requiring Level-0 in-VMM buffering (or the single-level now being considered by the ATLAS TDAQ group) since the VMM output bandwidth is not sufficient for the rates expected in some regions of the sTGC detectors. The requirements for such a readout have been established by the Readout Working group and are included in the "Requirements for the NSW VMM3 readout ASIC and the Readout Controler ASIC Design Review Report"
https://edms.cern.ch/file/1470540/1/NSW_VMM3_ROCReviewFeb2015_PDR_20150507.pdf
For completeness these specifications are reproduced here.

11.1 Summary of requirements and external constraints

General requirements

1. Level-0 rate: up to 1 MHz (Phase 2)
2. Level-0 latency: up to 10 µs fixed latency (Phase 2)
3. There is no simple dead time for Level-0; the complex dead time parameters are unknown.
4. Since several BCs may be read out per Level-0 trigger, a BC may belong to more than one trigger.
5. Level-1 rate: Phase 1: up to 100 kHz Phase 2: up to 400 kHz
6. Level-1 latency: Phase 1: 2.5 µs fixed latency Phase 2: up to 60 µs, variable latency
7. Configurable E-link speeds: 80, 160 or 320 Mb/s
8. Configuration registers and state machines must use TMR for SEU protection
9. The number of bunch crossings read out for a trigger must be configurable from 1 to 8.
10. A mechanism to completely identify the detector source of the data, independent of cable connections, must be provided.
11. The VMM and ROC will be configured via an SCA ASIC.
12. The ROC should generate test pulse trigger for the VMM in response to a TTC test pulse bit.

13. In response to the test pulse input, the VMM should generate the test pulse on the next BC clock.
14. Radiation tolerance. See: "New Small Wheel Radiation and Magnetic Field Environment" [5].
15. The VMM and ROC must provide an SEU flag or counter to be read, reset, by the SCA.
16. Resets: full reset (via pin and on power up); reset all but configuration registers.
17. The ITAR fuse from CERN must be placed in both the VMM and the ROC in order to be free of export restrictions.

VMM specific requirements

1. Max VMM output BW: 640 Mb/s (512 Mb/s, net with 8b/10b encoding)
2. The VMM configuration/monitor path must be operable independently of the acquisition state.
3. The VMM3 must provide a buffer overflow counter (per channel or per VMM?) to be read by the SCA.
4. Each VMM must have a dedicated (i.e. not shared) configuration connection to the SCA.
5. Each VMM must have a dedicated test pulse trigger pin and a test pulse enable configuration bit.
6. The hit output to the Read out Controller must be 8b/10b encoded. There must be at least one comma character sent between Level-0 events and they must be sent continuously when events are not sent.

Notes:

1. The VMM configuration/monitoring path, though independent of the acquisition path can not be operable while data taking. A configuration operation when VMM is sensitive (i.e. is acquiring data) would be extremely disruptive, and measurements would be certainly corrupted, with settling times typical of the stabilizers in the analog circuits. Considerable changes would be needed to attempt protection of the sensitive circuits and alleviate these effects.
2. The buffer overflow is handled by the digital interface (see section on exception messages).
3. The VMM3 does include a dedicated test pulse pin. It should be clarified that the test pulse should be aligned with the Bunch Crossing clock.

ROC specific requirements

1. TTC information is provided to the ROC via GBT from FELIX
2. The ROC must provide BCR and BC clock to other on-board ASICs, and, in addition, Level-0 Accept, ART clock (160 MHz), and RO (160 MHz) clock to each VMM.
3. The ROC will receive a 40 MHz BC clock, but needs a PLL to generate clocks for the 80, 160, 320 Mb/s E-links.
4. The data sent on the E-links must be 8b/10b encoded with Start-of-Packet and End-of-Packet symbols framing the data for one trigger.
5. Depending on a configuration bit, the ROC will send either the Level-0 Accept or the Level-1 Accept signal out as the "Level-0" signal.
6. The ROC E-links must adhere to SLVS or LVDS standards
7. When its buffers are nearing full, the ROC must be able to generate the BUSY-ON symbol in the Level-1 data flow to FELIX so that FELIX can generate RODBUSY to the Central Trigger. BUSY-OFF, with hysteresis, must be generated when the buffers return to a safe occupancy.

11.2 VMM

The overall block diagram for the part of the readout in the VMM is shown in Figure 12. It consists of FIFOs and logic blocks described below.

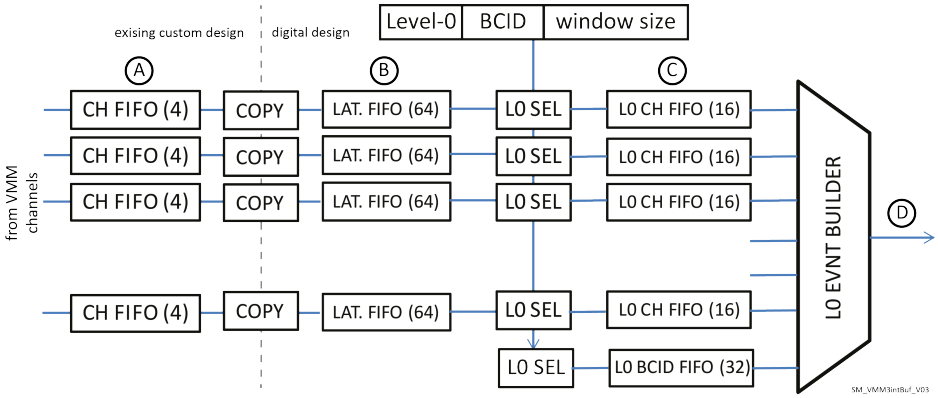

Figure 12: VMM3 internal buffers for Level-0 event output. The formats of the data at points A, B, C and D are shown in the figures following.

The existing VMM3 has a 4-deep FIFO per channel, implemented in custom layout. This will remain for non-ATLAS users wishing to operate in the continuous mode. The data (format shown in Figure 13) in these FIFOs is a sequence of hits that are transferred to a corresponding deep FIFO, implemented with the digital library, for the ATLAS-mode. Note that the 4-deep FIFO is filled asynchronously whenever the VMM peak detector finds a peak in its input signal. The channel has a minimum 200 ns dead time after a peak is found. Each channel will transfer between its FIFOs autonomously.

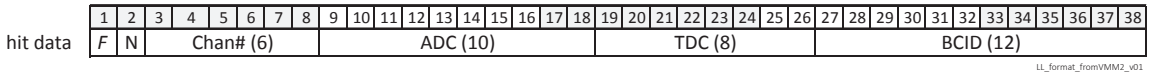

Figure 13: Data format from the VMM custom logic (Point A in Figure 12) "N" indicates that the hit is because the neighboring channel was above threshold. "F", flag, is always 1.

The maximum hit rate per channel is 4 MHz. With a 64-deep "latency" FIFO all hits for a period of 16.0 µs can be buffered, provided that the hits are read out at a rate of least 4 MHz. Since Level-0 Accepts can occur for consecutive bunch crossings, the read rate must be 40 MHz. Therefore overflow of the latency FIFOs cannot occur for Level-0 latencies smaller than 16 µs, unless the readout of the FIFOs stops (see below). The data format ("B") in the latency FIFO is shown in Figure 14. Since there is one FIFO for every channel, the channel number need not be stored.

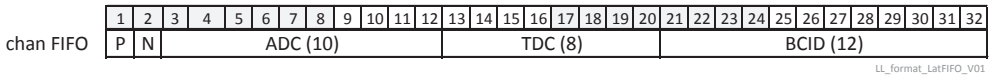

Figure 14: Format of the data in the Level-0 latency FIFO (Point B in Figure 12) "P" is a parity bit.

11.2.1 Level-0 data selector

Each channel has a Level-0 Selector circuit which is connected to the output of the channel's latency FIFO. The selector finds events within the BCID window (maximum size of 8 BCs) of a Level-0 Accept and copies them to the L0 Ch FIFO. The latency FIFO operates as a first-word-fall-through FIFO so that the FIFO output can be examined before it is discarded or copied. Since the maximum window size, 8 BCs, i.e. 200 ns, is less than the minimum dead time of a VMM channel, 200 ns, there can be at most one hit per channel in a trigger time window.

The selector compares the BCID field of the hit data in the FIFO (when the FIFO is not empty) with the content of a global BCID counter. This counter is offset by the Level-0 latency (less the number of BCs in the readout window before the triggering BCID) from the BCID counter used to tag hits when their peak is detected. In this way it indicates the BCID at the time of tagging, even though it is being examined after the Level-0 latency.

- On every BC clock, if the hit data becomes older than the Level-0 window, the data is flushed from the latency FIFO.
- If a Level-0 Accept is received for the given BCID and the BCID field of the hit data is inside the Level-0 window the hit data is copied to the following Level-0 FIFO.
- If a channel's L0 Sel circuit does not find a hit with a BCId falling within the window, a 'no data' item (first bit equal 0) is passed to the L0 Ch FIFO for that BCID.
- Therefore all L0 Ch FIFOs receive for each Level-0 Accept either a single 'hit data' or a 'no data' item and therefore all will simultaneously overflow when they are full (provided that the FIFOs are also read simultaneously). The L0 Ch FIFOs are effectively a single wide FIFO.
- Note that a hit may be copied more than once if more than one Level-0 Accept occurs within a BCID window.

The 24-bit item for a valid hit and for "no data" (format "C") is shown in Figure 15. For valid hit data the L0 Sel circuit also calculates a 3-bit relative BCId with respect to the BCId. The value of this relative BCId is 3 if the BCId in the data found in the latency FIFO and the BCId associated with the Level-0 Accept are equal. The parity bit is the parity bit read from the latency FIFO, checked and recalculated for Format "C". If the parity check failed, the recalculated parity bit is inverted to force detection of a parity error by the downstream logic. A parity error counter is also incremented.

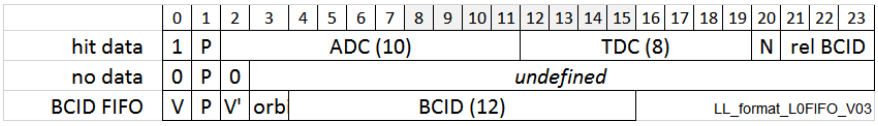

Figure 15: Format of the data in the Level-0 select output derandomizer FIFO (Point C in Figure 12)

For each Level-0 Accept, the BCID and a 2-bit orbit count associated with the Level-0 Accept are entered into a 16-bits wide FIFO, the L0 BCID FIFO (see Figure 12) together with a parity bit, P, and two overflow condition bits, V, V' (see Figure 15). If writing the items for the current Level-0 Accept caused the L0 Ch FIFOs to become full, the Overflow bit, V, in the BCID item is set and further writing to the L0 Ch FIFOs is suspended until their level falls

below a lower level. Note that the BCID FIFO is deeper than the L0 Ch FIFOs so writing to the BCID FIFO on every Level-0 Accept continues, but with the overflow bit set to indicate that there are no corresponding items in the L0 Ch FIFOs. If writing the BCID FIFO would cause an overflow, the second Overflow status bit (V') is set and subsequent writing to the BCID FIFO is suspended for the next 'Nskip' Level-0 Accepts. This is at least 'Nskip' µs and allows time for several events to be transferred out of the BCID and L0 Chan FIFOs.

11.2.2 Level-0 event building

For each Level-0 Accept, the outputs of the BCId FIFO and of the L0 Ch FIFOs are read in round-robin manner, starting with the BCId FIFO. Only valid data is forwarded to the event builder stage. To achieve synchronous overflow of all L0 Ch FIFOs the data of these FIFOs is transferred synchronously into registers which are then read in sequence by the Event Builder.

The format of the Level-0 Event Builder output, the data sent to the Read out Controller, is shown in Figure 16. The header is always sent, even when there are no following hits. The truncation bit, "T", indicates that the number of hits exceeded the (configurable) maximum for a VMM and that further hits for this Level-0 trigger have been discarded. It is set in the last hit that is transferred.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
header	V	P	orb		BCID (12)												1st word after comma															
hit data	1	P	*R*	T	Chan# (6)						ADC (10)										TDC (8)								N	rel BCID		

LL_format_VMM3out_V04

Figure 16: Format of the data sent to the ROC ASIC (Point D in Figure 12) Zero or more hits may follow the header.

Once the overflow bit, "V", in the BCID word is active, only the header is output; the BCId read from the BCId FIFO is the first BCId for which the overflow occurred. To make this possible the depth of the BCId FIFO has to be at least one word larger than that of the L0 Ch FIFOs. For outputting 64 32-bit words output via a link with an effective bandwidth of 512 Mb/s, 4 µs is needed, i.e. 160 bunch crossings. In this time, for Phase 2, on average four Level-0 Accepts would occur, but in theory up to 160 could occur. Complex dead time would reduce this, but the complex dead time parameters for Phase 2 are not known. However, since the complex dead time parameters are not known, possible BCID FIFO overflows must be handled. If a BCID word written into the FIFO would cause the BCID FIFO to be full, it is written with the overflow bit, V', set (Figure 15). The Level-0 Event Builder sends a message word indicating this overflow. The ROC then knows not to expect data from this VMM for the next 'Nskip' Level-0 Accepts.

Event building in one stage at an average Level-0 Accept rate of 1 MHz requires that a complete round-robin cycle on average should be completed in 1 µs, i.e. in 15 ns per step. Event building in two stages would allow reducing this to 30 ns, i.e. a 40 MHz clock can be used.

The depths of the L0 and BCID FIFOs were determined for a worst case occupancy corresponding to the highest η region of the Micromegas detectors. Figure 17 shows the channel occupancy per VMM per L0 accept resulting from a detailed simulation which assumes a hit rate of 15 kHz/cm^2 and that the single plane hits are the result of track segments (producing higher number of hits than single photon hits). Then a detailed model of the FIFOs was gen-

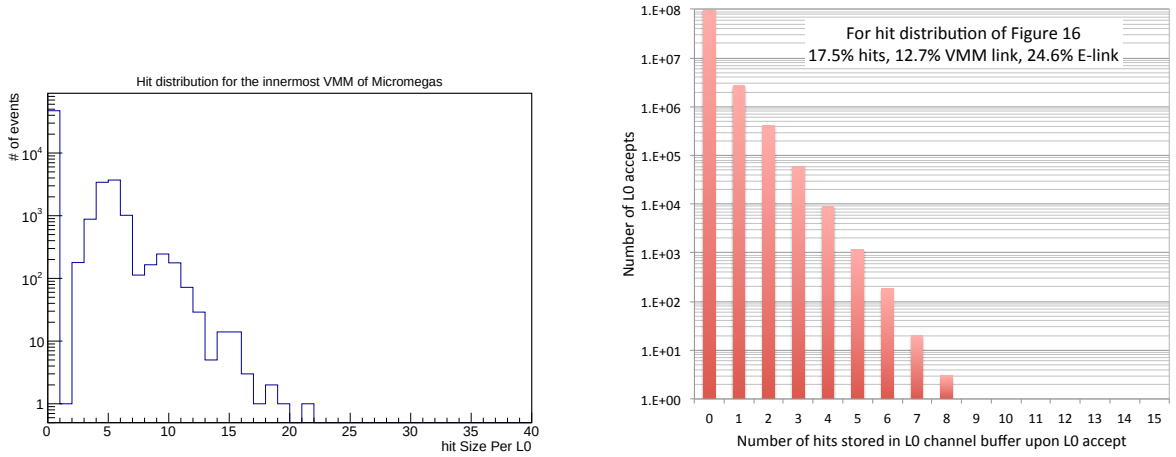

Figure 17: Left:Simulated distribution of the number of channels per VMM hit per L0 accept. Right: Simulated L0 FIFO occupancy for the hit simulated hit distribution for the distribution on the left.

erated using an 1 MHz L0 trigger rate, a typical LHC bunch fill, and the VMM bandwidth. It has been assumed that together with each event fragment two comma characters are output, indicating the start and the end of the fragment. The model generated 10^8 L0 triggers Poisson distributed in steps of the BC clock period. The resulting L0 FIFO occupancy for the simulated hit distribution is shown in Figure 17. In Figure 18, the L0 FIFO occupancy corresponding to an extreme case is shown. The fraction of L0 accepts with hits is about 3 times higher than the simulated fraction (50% instead of 17.5%) and has a hit distribution generated by assuming a hit probability per channel such that the average number of hits is 12.0, more than twice the average of the simulated distribution (4.9). In this case the model determines for each L0 accept for each channel whether there is a hit on the basis of the hit probability per channel. It has been verified that this procedure for an average number of hits of 4.9, for 17.5% of the L0 accepts having hits, results in almost the same L0 FIFO occupancy as shown in Figure 17. The VMM3 L0 FIFO is therefore 16-deep whereas the BCID FIFO, which needs to be deeper as explained above, is 32-deep.

11.2.3 Transfer from VMM to Readout Controller

The data transfer from VMM to Readout Controller is via two serial lines (even bits on one, odd bits on the other) running at 160 MHz with Double Data Rate (DDR) giving a total bandwidth of 640 Mb/s. Two lines are used to reduce the clock rate. Figure 19 shows the data as clocked out from the VMM data lines.

The Readout Controller supplies the clock for this transfer. 8b/10b encoding is used with one or more comma characters transmitted continuously between Level-0 events. The 8b/10b encoding reduces the effective bandwidth to 512 Mb/s. The 512 Mb/s VMM output capacity is clearly sufficient. (The readout clock input of the VMM can be up to 200 MHz, but this would require modifying the CERN ePLL to produce 200 MHz output.)

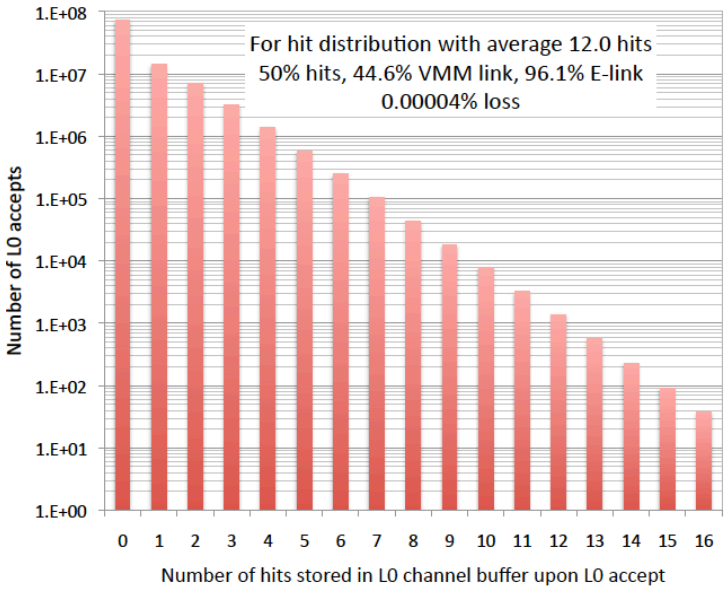

Figure 18: Simulated L0 channel FIFO occupancy for 50% (instead of 17.5%) of the L0 accepts giving rise to hits, the number of hits is on average 12 (instead of 4.9), the procedure used for picking the number of hits per L0 accept is described in the text.

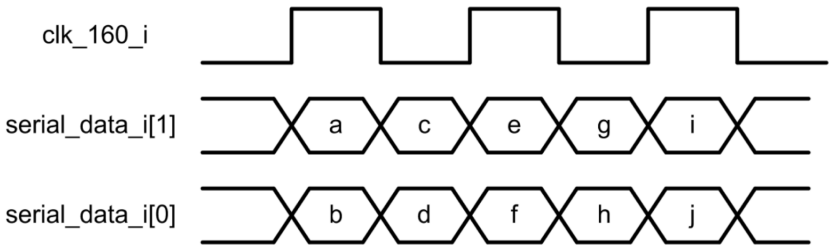

Figure 19: Data as clocked out from the VMM.

11.2.4 VMM clock domains

40 MHz (BC clock): Front-end, Latency FIFOs, Level-0 Selection, Level-0 FIFOs (in port)
160 MHz (VMM Readout clock): Level-0 FIFOs (out port), Event Builder

11.3 Trigger Paths

The VMM, in addition to the information recorded at Level-1 (or Level-0), provides trigger primitives for both Micromegas and sTGC detectors. In each case an independent trigger data path provides information to the trigger processor at the bunch crossing frequency. In the next two subsections a short description, the requirements, and implementation of the two data paths will be discussed.

11.3.1 Micromegas Trigger Primitive

The Micromegas Detector in the NSW has a total of ~ 2 million channels that would make it impossible to have a trigger system using information from these channels in parallel and in real time. The Micromegas trigger concept takes advantage of the fine pitch ($\approx 0.5\,\text{mm}$) of the detectors in the following way. Each VMM provides, at a single dedicated digital output, art, the address of the first on-chip above-threshold event, called address in real time (ART). The system, thus, is equivalent to a trigger system with segmentation of $3.2\,\text{cm}$ ($64 \times 0.5\,\text{mm}$) with spatial resolution of the order of $300\,\mu\text{m}$ sufficient for the angular resolution required in order to reject candidates that are not consistent with those originating at the interaction point. This way the trigger channel count is reduced to $\sim 32,000$ channels.

The ART mode is enabled with the bit *sfa*. Either at the pulse threshold crossing (bit *sfam* low) or at the pulse peak (bit *sfam* high) a flag is released at the art output. The flag is followed by the serialized address of the event. Also in this case the address is released either at each clock cycle or at each clock edge of the external ART clock, depending on the global bit *sdcka*.

ART Requirements/Properties

- Arbitration logic blocks subsequent to the first hit those occurring 2 or more ns later.
- The ART stream clock frequency is $160\,\text{MHz}$ and is provided in each VMM of a front end board by a dedicated SLVS line from the ROC serving the front end board.
- It can be optionally clocked at both edges of the clock for an effective rate of $320\,\text{MHz}$.
- The ART must be aligned to the ART clock.
- It can optionally be provided at threshold crossing or at peak found. In the NSW implementation we choose the former. It reduces the latency by about the peaking time and at the same time allows the use of longer integration time which results in lower electronic noise and higher charge collection. Furthermore, for the trigger path, amplitude slue is not an issue.
- While the direct outputs are active simultaneously with all modes of operation they are not needed in Micromegas. It must be possible to turn off the SLVS drivers in order to reduce power consumption and the possibility of digital interference with the front end operation.

The ART latency is the sum of several delays

1. Time from instantaneous charge event to 1% of the peak is $\sim 10\,\text{ns}$
2. Time from pulse peak to peak found $\sim 5\,\text{ns}$
3. Digital latency from comparator firing to leading edge of ART is $\sim 5\,\text{ns}$
4. Digital latency from peak found to leading edge of ART is $\sim 5\,\text{ns}$

Or $\sim 15\,\text{ns}$ for the threshold crossing option or $\sim 20\,\text{ns}$ + peaking time if the peak detect is chosen. The above assumes a typical case of input capacitance of $200\,\text{pF}$ and a load of $20\,\text{pF}$ at the digital output.

11.3.2 sTGC Trigger Primitives

The sTGC detector trigger concept uses projective, overlapping cathode pads to define a candidate track segment by a 3 out of four coincidence in both quadruplets in a sector. The projective tower defines then bands of strips to be read out and sent to the sTGC trigger logic. The pad signals operate in the direct-output mode in which the 64 channel digital outputs ttp are activated and provide one of four different timing pulses:

- Time-over-threshold (ToT)
- Threshold-to-peak (TtP)
- Peak-to-threshold (PtT)
- A 10ns pulse occurring at peak (PtP)

The mode can be set using the global bits *stot* and *stpp*. The channel self resets at the end of the timing pulse, thus providing continuous and independent operation of all 64 channels. Alternatively, if the bits *spdc* and *s6b* are both set high, the peak detector converts the voltage into a current that is routed to the 6-bit ADC. The 6-bit ADC provides a low-resolution A/D conversion of the peak amplitude in a conversion time of about 25 ns from the peak time. The conversion time and the baseline (zeroing) are adjustable using the global bit set *sc6b* (the conversion time is the number of data clocks set by the *sc6b* bits) and the channel bit set *sz6b* respectively. The serialized 6-bit data is made available at the channel output immediately after an event flag which occurs at the peak time. The flag is lowered at the next clock cycle of the data clock, and the 6-bit ADC data is shifted out after that, either at each clock cycle or at each clock edge of the data clock depending on the global bit *sdck6b*. The channel reset occurs after the last bit has been shifted out.

Because of the large area of some pads and the high rate, dead time per channel with an effect in efficiency is of concern for the sTGC trigger system and therefore choice of the direct output format is important. We summarize here the requirements of the digital part (see section 4 for the analog requirements):

sTGC digital trigger requirements/properties

- While the direct outputs are active simultaneously with all modes of operation they are not needed in readout of the sTGC strips and wires. It must be possible to turn off the SLVS drivers in order to reduce power consumption and the possibility of digital interference with the front end operation.
- The 6-bit stream clock frequency is 160 MHz and is provided in each VMM of a front end board by a dedicated SLVS line from the TDS serving the front end board.
- It can be optionally clocked at both edges of the clock for an effective rate of 320 MHz .

The direct mode latency can be calculated from the following:

1. Time from instantaneous charge event to 1% of the peak is ~ 10 ns
2. Time from pulse peak to peak found ~ 5 ns

3. Digital latency from comparator–threshold to the leading edge of ToT is ~ 4 ns
4. Digital latency from peak found to leading edge of 6-bit ADC is ~ 4 ns

Therefore the total latency is 14 ns for ToT or 18 ns +peaking time for the 6-bit ADC option. The dead time because of the 10-bit ADC latency is ~ 200 ns after the peak. However it is possible to interrupt the 10-bit ADC conversion when the signal drops below threshold (the earliest the channel can be reset) thus providing a lower resolution peak value with the minimum dead time by enabling the bit *sfrst*.

12 VMM3 testing

There are many tests performed until now on the VMM3 ASIC. Most of them are reported on the progress report and intermediate reviews shown in subsection 2.2. Moreover the following tests were performed:

- L0 - The readout was tested on the so called L0 mode and was found to be working correctly at the nominal 160 MHz clock. The data lines though found to be swapped and are corrected on VMM3a. https://indico.cern.ch/event/631131/contributions/2561766/attachments/1450723/2237564/2017_3_27_VMM_L0_Iakovidis.pdf
- Report on the ADC accumulation, locking situation, early measurements with micromegas, noise measurements, functionality tests and features: https://indico.cern.ch/event/626471/contributions/2533318/attachments/1435432/2207051/2017_03_28_MMWeekly_VMM3_Update_Iakovidis.pdf
- Yield issues with massive chip testing: https://indico.cern.ch/event/657773/contributions/2681319/attachments/1504147/2343627/2017_8_04_VMM_ADCYield.pdf
- ESD protection studies: https://indico.cern.ch/event/657773/contributions/2681018/attachments/1503925/2343346/2017_8_04_ESD.pdf (update will be given during the review).
- Performance with the sTGC and Micromegas detectors will be shown during the review.

12.1 Integration with the NSW Electronics

The NSW electronics are integrated in the Vertical Slice lab at B188. There are integration week hold every 3-4 months on which all the system is put together and tested. The VMM3 was integrated and tested with all the following interfaces/ASICs:

- ADDCv2. The VMM3 was found compatible and fully functional with the ARTv2 ASIC.
- The VMM3 was found fully compatible with the TDSv2 ASIC on the sTGC frontend boards.
- The VMM3 was found compatible with the SPI programming through the SCA ASIC.

- The readout of the VMM was tested and found fully functional with the FPGA-ROC algorithm, readout by L1DDC and FELIX. The test of ROC interface is pending to date due to low availability of ROC ASICs. It is intended to be tested by the Michigan group which develops a board hosting a VMM3, a ROC, TDS and one SCA. Results maybe available during the review.

The full report of the last integration week: https://indico.cern.ch/event/655015/contributions/2667675/attachments/1496964/2329595/2017_07_21_NSW_ELX_VS.pdf

12.2 VMM3 calibration

The VMM3 was calibrated for the following:

- DAC pulser and threshold to mV by the xADC on the FPGA
- Gain calibration by varying the input charge (internal capacitor) and measuring the PDO.
- TAC gain, time-walk and time-resolution measurements
- Pedestal and noise measurement

Details of these calibration procedures will be given during the review.

13 Radiation Tolerance and SEU

The VMM ASIC is expected to be exposed to a total ionization dose of 100 krad according to the simulations done [6]. Deep sub-micron technologies are known to be immune to much higher TID doses because of increasingly thinner oxide layers which can trap smaller amounts of charge. Of course design techniques are also applied to mitigate issues. Although not expected to be a problem, the VMM3 will be tested for TID tolerance in the ^{60}Co source irradiation facility at BNL. However single event upsets (SEU) become increasingly more serious as the technology feature size decreases because of the smaller capacitance in the storage elements that need smaller energy depositions in order to flip their state. In the VMM there are two types of storage elements that require SEU protection, the configuration register, and the state machine control logic. In the data domain perhaps the 12-bit BCID register (under discussion) whereas the FIFOs need not be protected as an occasional data corruption is not an issue. To mitigate the SEU effects in the VMM storage elements two different techniques are used:

1. Dual Interlocked Cells (DICE) for the protection of the configuration register, and
2. The more common Triple Modular Redundancy (TMR) for the state machines and possibly the BCID register

The DICE uses redundancy to significantly reduce susceptibility to an upset. D flip flops based on the dual interlocked cell latches have redundant storage nodes and restore the cell's original state when an SEU error is introduced in a single node [7]. The scheme fails if multiple nodes are upset but this is far less likely, especially at the rather modest neutron levels of $\sim 10^{12}\, n/\mathrm{cm}^2$/year at luminosity $7 \times 10^{34}\,\mathrm{s}^{-1}\mathrm{cm}^{-2}$ The TMR technique is used to protect the small number (less than 20) storage elements of the state machines. At the measured upset cross sections of order $10^{-14}\mathrm{cm}^2$/bit the upset probability is of order one tenth of an upset per VMM per year.

13.1 VMM1 SEU testing

The first version of the VMM was tested in the NSCR Demokritos Tandem accelerator. The VMM1 was irradiated in the area of the configuration registers for ∼44 h n of energy range ∼18-22 MeV achieving an integrated n flux of $3.1 \times 10^{11}\, n\text{cm}^{-2}$. The measured cross-section found to be $(4.1 \pm 0.7) \times 10^{-14}\,\text{cm}^2$/bit. This shows a probability of ∼ 60 SEU/y/VMM for the NSW expected n flux.

13.2 VMM3 SEU testing

The VMM3 was irradiated at NSCR Demokritos Tandem accelerator as VMM1. It was irradiated in the area of the configuration registers, the state machine and the L0 registers. For the non-L0 registers and non-L0 state machine the on chip location is well defined. For L0 an automated place& route was used and the registers may be scattered all over the L0 area.
Neutron energy was well defined at 20.1 MeV (Figure 20 left) through the nuclear reaction ^{3}H(d,n)^{4}He (according to NeusDesc). Few parasitic (compared to the main flux). The Tritium target of $5 \times 5\text{mm}^2$ was used providing enough to uniformly in the needed regions of VMM with $\sim 4\pi$ coverage. VMM3 accumulated a dose of $2.28 \times 10^{11}\, n\text{cm}^{-2}$ in 34.7 h total in which an automated firmware was writing and reading the SPI every 12 sec comparing the readout bits to the one that were written before. No bit-flips observed meaning that the redundancy scheme was able to correct for it. Also the chip was readout for several periods (cannot readout while writing the SPI) and no running glitches were observed in the readout (both continuous and L0 readout modes).

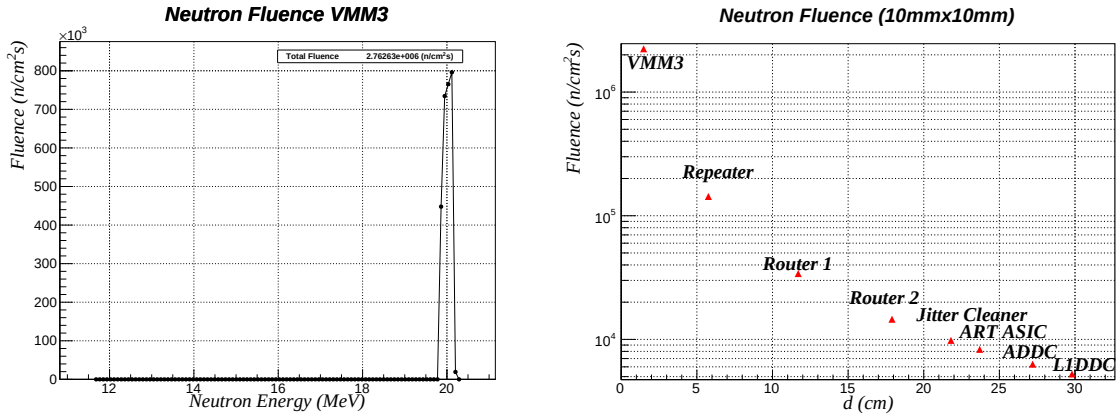

Figure 20: Left: Energy spectrum of the irradiated neutrons, Right: The flux of the neutrons versus the position of the NSW components placed under the irradiation.

14 Testing, Validation and Commissioning

The production testing of the VMM will be done along with the functional testing of the ASIC. The testing will be based in the noise, alive channels and functionality that will be defined as crucial for the ASIC validation before mounted to the boards. An automated test pattern

generator can be used to test the packaged chips on the bench-top with a dedicated test PCB. The chips will be categorized based on the criteria to “Good”, “Good as Spare” and “Rejected”.

15 Reliability Matters

15.1 Consequences of Failures

The consequences of VMM failures are easily deduced from the system architecture and overall NSW design. In increasing severity they are:

- Occasional inoperative individual channels due to a variety of reasons have little impact on the quality of data. An isolated channel will result in reduced (local) spatial resolution in both the Micromegas and sTGC detectors, while two or more adjacent channel failures will have a (local) effect in efficiency as well
- Failure of a VMM will result in the loss of information from all 64 channels. In the case of the Micromegas detectors this would result in a dead segment 3.5 cm in radius of a single plane of a given sector. In the case of sTGC, because of the larger pitch, it would result in a significantly larger loss depending on the type of readout affected (strips, pads, wires, as well as the location in a sector).

15.2 Prior Knowledge of Expected Reliability

No such knowledge exists at this point.

15.3 Measures Proposed to Insure Reliability of Component and/or System

The assembled front end cards will undergo burn-in following guidelines described in the IBM 8RF Design Manual, with perhaps modifications to be determined.

15.4 Quality Control to Validate Reliability Specifications during Production

The production devices will be tested in an automated station to be designed and fabricated by the Tomsk group in collaboration with BNL. The goal will be to identify fully operational units, failed ones to be discarded and functional ones with issues that might be useable if necessary. The exact test protocol and parameters that will determine usability will be determined as we gain more experience with the VMM2 and VMM3 prototypes.

Appendices

A Deadtime in Several modes of operation

A.1 sTGC modes of operation

For the different detector elements of sTGC detectors the modes of operation along with the configuration registers are shown in Table 7.

Table 7: Modes of Operation and its configuration registers for sTGC detectors.

	Trigger Path	**Data Path**	**Detector Element**	**Configuration Registers**
1	ToT	10-bit	Pads	*sttt=1, stot=1, s10b=1, stpp=0, s6b=0, sfrst=0*
2	ToT	1-bit	Pads	*sttt=1, stot=1, s10b=1, stpp=0, s6b=0, sfrst=1*
3	6-bit	10-bit	Strips, Wires	*sttt=1, stot=N/A, s10b=1, stpp=N/A, s6b=1, sfrst=0*

The dead time of **Mode 1** (Figure 21) of the above table is explained as follow: The trigger output is high between the rising edge and the falling edge (as long as the signal is above threshold). The readout output is the 10-bit ADC. The effective dead time starts at the rising edge and ends 220 ns (the digitization time) + 30 ns (the reset time) after the peaking. If the ToT is longer than the digitization time the last occurring reset (ToT or ADC) will dominate.

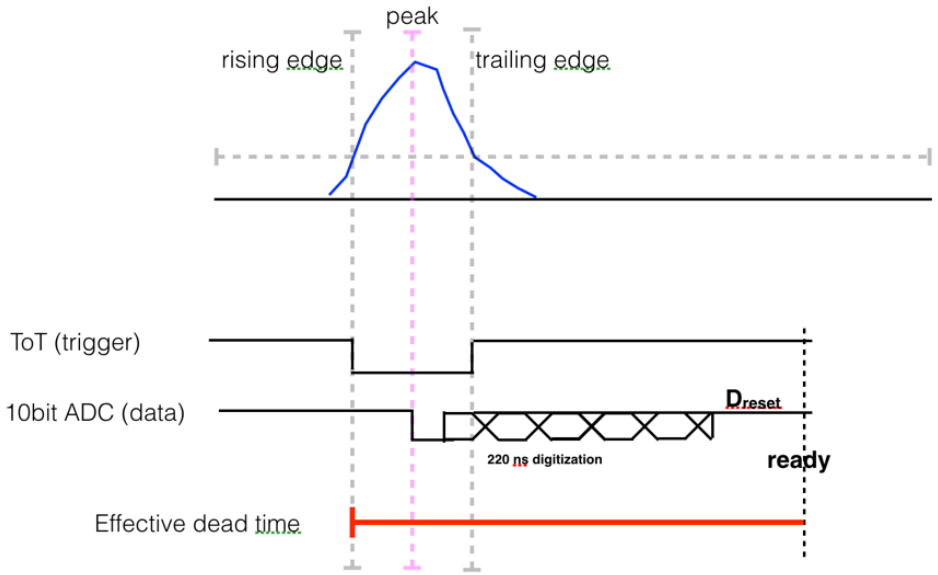

Figure 21: ToT (trigger) + 10-bit ADC (data) output signals.

The dead time of **Mode 2** (Figure 22) of the above table is explained as follow: The trigger output is high between the rising edge and the falling edge (as long as the signal is above threshold). The readout output is the 1-bit ADC, with value 1 signifying above threshold. The effective dead time starts at the rising edge and ends 60 ns (the reset time) after the trailing edge. As long as the total charge is bellow 6 pC the reset time is 60 ns . If the ToT is longer than the digitization time the last occurring reset (ToT or ADC) will dominate.

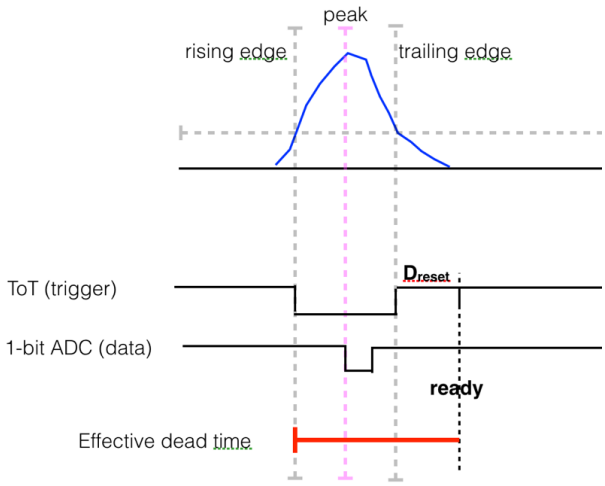

Figure 22: ToT (trigger) + 1-bit ADC (fast reset) (data) output signals.

The dead time of **Mode 3** (Figure 23) of the above table is explained as follow: The trigger output is the 6-bit ADC. The readout output is the 10-bit ADC. The effective dead time starts at the rising edge and ends 220 ns (the digitization time) + 30 ns (the reset time) after the peak.

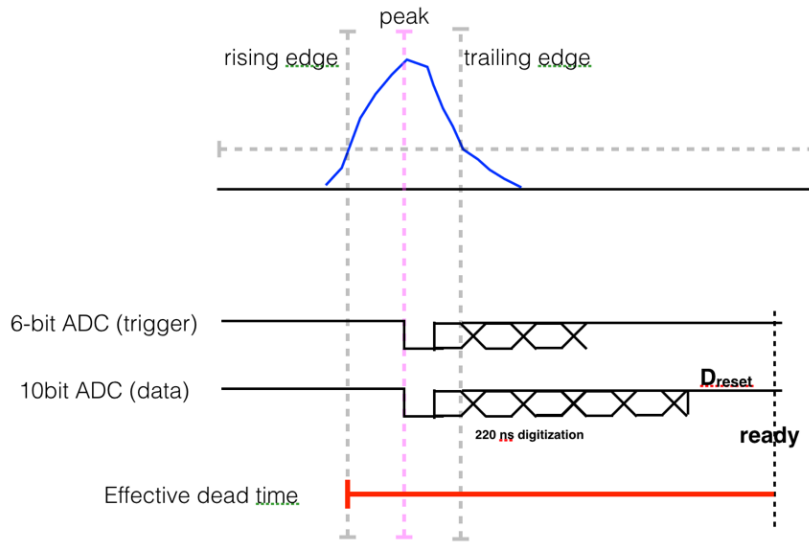

Figure 23: 6-bit ADC (trigger) + 10-bit ADC (data) output signals.

The modes are summarized in Table 8.

Table 8: Modes of Operation and its configuration registers for sTGC detectors.

	Trigger Path	**Data Path**	**Dead time start**	**Duration**	**BC**
1	ToT	10-bit	Rising edge	Peaking time + 220 ns digitization time + 30 ns reset time	Peak
2	ToT	1-bit	Rising edge	ToT + 60 ns fast reset	Peak
3	6-bit	10-bit	Rising edge	Peaking time + 220 ns digitization time + 30 ns reset time	Peak

Notes of clarification

Figure 23 shows the output in the ToT (trigger) + 1-bit ADC (readout) (Mode 2):

- The trailing edge of the first signal and the rising edge of the second signal are separated by more than D_{TOT}. In this case both signals are detected.
- The trailing edge of the first signal and the rising edge of the second signal are separated by less than D_{TOT}, but the signals do not overlap. In this case the second signal is lost.
- The same as above but with a third signal following the second one with its rising edge before the falling edge of the second one. In this case only the first signal is detected.
- The two signals overlap (their pileup is not shown in the figure). In this case, the output signal is active from the rising edge of the first signal until the trailing edge of the second signal.

A.2 Micromegas trigger dead time

The micromegas trigger system has only one detector element and this is the strips. The schema is much simpler using the ART address. It takes 2 CKART clock cycles (13 ns at 160 MHz) to reset the ART circuit after the release of the last ART bit. The ART can occur at threshold or the peak depending on the configuration of registers *sfa=1, sfam=0* for timing at threshold and *sfa=1, sfam=1* for timing at peak. The *ssart* register enables the ART flag synchronization.

References

[1] G. De Geronimo and S. Li. "Shaper Design in CMOS for High Dynamic Range". *Nuclear Science, IEEE Transactions on* **58** (Oct. 2011), p. 2382. DOI: 10.1109/TNS.2011.2162963.

[2] G. De Geronimo *et al.* "VMM1 - An ASIC for Micropattern Detectors". *Nuclear Science, IEEE Transactions on* **60** (June 2013), p. 2314. DOI: 10.1109/TNS.2013.2258683.

[3] G. De Geronimo *et al.* "ASIC for Small Angle Neutron Scattering Experiments at the SNS". *Nuclear Science, IEEE Transactions on* **54** (June 2007), p. 541. DOI: 10.1109/TNS.2007.893718.

[4] G. Iakovidis. "Research and Development in Micromegas Detector for the ATLAS Upgrade". CERN-THESIS-2014-148. PhD thesis. Natl. Tech. U., Athens, Oct. 2014.

[5] R. Edgar *et al. New Small Wheel Radiation and Magnetic Field Environment.* Jan. 2015.

[6] ATLAS Collaboration. *New Small Wheel Technical Design Report.* CERN-LHCC-2013-006. ATLAS-TDR-020. Geneva, June 2013.

[7] F. Faccio *et al.* "Total dose and single event effects (SEE) in a 0.25 µm CMOS technology". *Electronics for LHC experiments. Proceedings, 4th Workshop, Rome, Italy, September 21-25, 1998.* 1998.