2   Data Format – L0 Trigger Mode

All data words are 32 bits. Some words are identified by a 4-bit type field (bits 31-28). Hit data words have a 32-bit payload with no type field. The number of hit data words are specified in a typed word that proceeds them.

Each trigger produces an Event Header followed by a pair of Trigger Time words. For each VMM chip there is a chip header word followed by a variable number (0-64) of hit data words. The chip header word contains the number of hit data words that follow it. A chip trailer word signals the end of data from the VMM chip.

Data from the second VMM chip in the same format immediately follows.

2.1   Data Type List

0 – Event Header
1 – Trigger Time 1
2 – Trigger Time 2
3 – VMM 1 Chip Header
4 – VMM 1 Chip Trailer
5 – VMM 2 Chip Header
6 – VMM 2 Chip Trailer

2.2   Data Types

Event Header (0) – marks beginning of event.

(31 – 28) = 0 (Type)
(27 – 0) = trigger number

Trigger Time (1, 2) – time of trigger occurrence relative to the most recent global reset. Time is measured by a 48-bit counter that is clocked by the 160 MHz clock. The six bytes of the trigger time are reported in two words:

$$\text{Time} = T_A\ T_B\ T_C\ T_D\ T_E\ T_F$$

Word 1:
(31 – 28) = 1 (Type)
(27 – 26) = phase count (40 MHz clock offset in 160 MHz periods)
(25 – 24) = T_C bits 1-0 (duplicated in Word 2)
(23 – 16) = T_D
(15 – 8)   = T_E
(7 – 0)   = T_F

<u>Word 2</u>:

 (31 – 28) = 2 (Type)
 (27 – 24) = reserved (read as 0)
 (23 – 16) = T_A
 (15 – 8) = T_B
 (7 – 0) = T_C

VMM 1 Chip Header (3) – marks beginning of data from VMM 1.

 (31 – 28) = 3 (Type)
 (27 – 24) = reserved (read as 0)
 (23 – 16) = number of 32-bit hit data words to follow (0-64)
 (15 – 0) = chip trigger header

VMM 1 Chip Trailer (4) – marks end of data from VMM 1.

 (31 – 28) = 4 (Type)
 (27 – 0) = chip trigger number (from count of chip data groups)

VMM 2 Chip Header (5) – marks beginning of data from VMM 2.

 (31 – 28) = 5 (Type)
 (27 – 24) = reserved (read as 0)
 (23 – 16) = number of 32-bit hit data words to follow (0-64)
 (15 – 0) = chip trigger header

VMM 2 Chip Trailer (6) – marks end of data from VMM 2.

 (31 – 28) = 6 (Type)
 (27 – 0) = chip trigger number (from count of chip data groups)

32-bit hit data words format (added by Sergey):

 (31-29) relBCID
 (28) N
 (27-20) TDC
 (19-10) ADC
 (9-4) channel number
 (3) T
 (2) R
 (1) P
 (0) = 1

Data stream

Event Header (trigger 1)
Trigger Time 1
Trigger Time 2
VMM 1 Chip Header
      Hit 1
      Hit 2
      ------   (n = 0-64)
      Hit n
VMM 1 Chip Trailer
VMM 2 Chip Header
      Hit 1
      Hit 2
      ------   (m = 0-64)
      Hit m
VMM 2 Chip Trailer

Event Header (trigger 2)
Trigger Time 1
Trigger Time 2
VMM 1 Chip Header
      Hit 1
      Hit 2
      ------   (n = 0-64)
      Hit n
VMM 1 Chip Trailer
VMM 2 Chip Header
      Hit 1
      Hit 2
      ------   (m = 0-64)
      Hit m
VMM 2 Chip Trailer

. . . .
. . . .
. . . .

1   FPGA Prototype Registers

1. <u>BOARD ID</u> [addr = 0]

    (31) – (0) ID (R) – "xxxxxxxx"

2. <u>CONTROL</u>   [addr = 4]

    (0) GO (R/W) – '1' = go acquisition, '0' = stop acquisition

    (1) RESET MAIN CLOCK GENERATOR (R/W) – '1' = hold reset, '0' = enable
        locking to input clock

    (2) – (26) – not used

    (25) CLEAR LATCHED BITS (W) – '1' = assert pulse

    (26) SYNC_RESET PULSE (W) – '1' = assert pulse

    (27) START TEST PULSER (W) – '1' = assert (only if CONTROL 2 (7) = '0')

    (28) LATCH STATUS PULSE (W) – '1' = assert pulse

    (29) TRIGGER DELAY LOAD PULSE (W) – '1' = assert pulse

    (30) BUS SOFT RESET PULSE (W) – '1' = assert pulse

    (31) RESET PULSE (W) – '1' = assert pulse

3. <u>CONTROL 2</u> [addr = 8]

    (1) – (0) TRIGGER SELECT (R/W) – '0' = external, '1' = external delayed,
            '2' = internal pulser (delayed)

    (2) – SYNC_RESET SELECT (R/W) – '0' = external, '1' = internal

    (3) – not used

    (5) – (4) TEST PULSE SELECT (R/W) – '0' = none, '1' = external trigger,
            '2' = internal pulser

    (6) – VMM SELECT (R/W) – '0' = VMM #1, '1' = VMM #2

    (7) START TEST PULSER on SYNC_RESET (R/W) – '0' = no, '1' = yes

(10) – (8) – BCR mode – 0 = BCR only, 1 = OCR only, 2 = OCR2 only,
3 = BCR + OCR, 4 = BCR + OCR2
5 = OCR4 only, 7 = NONE (done only)

(11) – (31) – unused

4. DOUBLE PULSE INTERNAL TRIGGER [addr = C]

(15) – (0) – DELAY between trigger pulse pair (R/W) – (1 count = 25 ns)
(DELAY should be > Internal TRIGGER WIDTH – see DELAY register)

(16) – DOUBLE PULSE ENABLE (R/W) – '0' = disable, '1' = enable

(17) – (31) – unused

5. <u>RESERVED 2</u> [addr = 10]

6. <u>RESERVED 3</u> [addr = 14]

7. <u>DELAY</u> [addr = 18]

(11) – (0) – TRIGGER DELAY (R/W) – (1 count = 25 ns) (max = 102.4 us)

(12) – (15) – unused

(23) – (16) – Internal TRIGGER WIDTH (R/W) – (1 count = 25 ns)

(24) – (31) – unused

8. <u>BUSY</u> [addr = 1C]

(15) – (0) – TRIGGER BUSY PERIOD (R/W) – (1 count = 6.25 ns)

(16) – USE TRIGGER BUSY (R/W) – '0' = no, '1' = yes

(17) – (31) – unused

9. <u>STATUS 0</u> [addr = 20]

(11) – (0) – READ ADDRESS FOR TRIGGER DELAY MEMORY (R)

(23) – (12) – WRITE ADDRESS FOR TRIGGER DELAY MEMORY (R)

```
--------------------------------------------------------------------------------
        when  WRITE ADDRESS  >  READ ADDRESS
               DELAY = WRITE ADDRESS – READ ADDRESS

        when  READ ADDRESS  >  WRITE ADDRESS
               DELAY = 4096 – READ ADDRESS – WRITE ADDRESS
--------------------------------------------------------------------------------
```

(24) – (26) – unused

(27) – REF CLOCK GENERATOR LOCKED (R) – (250, 100, 62.5, 12.5 MHz)

(28) – MAIN CLOCK GENERATOR LOCKED (R) – (320, 160, 40 MHz)

(29) – DIRECT DATA CLOCK GENERATOR LOCKED (R) – (160 MHz)

(30) – LOSS OF DIRECT LOCK OCCURRED (R) – since last reset of latched bits

(31) – LOSS OF MAIN LOCK OCCURRED (R) – since last reset of latched bits

NOTE: Recovery from loss of lock for MAIN or DIRECT clocks requires reset of main clock generator, clearing of latched data bits, and phase adjustment of both main and direct clocks.

10. RESERVED [addr = 24]

11. PHASE ADJUST - MAIN DATA [addr = 28]

     (11) – (0) – NUMBER OF PHASE ADJUSTMENT STEPS (R/W) – (1 step = 18.6ps)

     (12) – (30) – unused

     (31) – PULSE START OF PHASE ADJUSTMENT (W) – '1' = assert

12. PHASE STATUS - MAIN DATA [addr = 2C]

     (0) – PHASE ADJUSTMENT STATUS (R) – '0' = active, '1' = not active (done)

     (1) – PHASE SHIFT STATUS (R) – '1' = phase shift requested and intact, '0' = any previous phase shift request is not valid and must be done again. This bit is reset when PLL enters the locked state. A loss and subsequent regain of lock will reset this bit. Also check the PLL locked status. If this bit was previously set and the PLL is no longer locked this bit will remain '1' until re-lock is achieved.

     (2) – (3) – unused

     (15) – (4) – NUMBER OF PHASE SHIFT STEPS ACKNOWLEDGED (R)

(16) – (31) – unused

13. <u>PHASE ADJUST - DIRECT DATA</u> [addr = 30]

    (11) – (0) – NUMBER OF PHASE ADJUSTMENT STEPS (R/W) – (1 step = 18.6ps)

    (12) – (30) – unused

    (31) – PULSE START OF PHASE ADJUSTMENT (W) – '1' = assert

14. <u>PHASE STATUS - DIRECT DATA</u> [addr = 34]

    (0) – PHASE ADJUSTMENT STATUS (R) – '0' = active, '1' = not active (done)

    (2) – PHASE SHIFT STATUS (R) – '1' = phase shift requested and intact, '0' = any previous phase shift request is not valid and must be done again. This bit is reset when PLL enters the locked state. A loss and subsequent regain of lock will reset this bit. Also check the PLL locked status. If this bit was previously set and the PLL is no longer locked this bit will remain '1' until re-lock is achieved.

    (2) – (3) – unused

    (15) – (4) – NUMBER OF PHASE SHIFT STEPS ACKNOWLEDGED (R)

    (16) – (31) – unused

15. <u>SPARE 1</u> [addr = 38]

    (31) – (0) – unused

16. <u>SPARE 2</u> [addr = 3C]

    (31) – (0) – unused

17. <u>CONFIG MEMORY</u> <u>CONTROL</u> [addr = 40]

    (2) – (0) – MODE :   0 = write memory,
                               1 = read memory,
                               2 = configure VMM 1,
                               3 = configure VMM 2,
                               4 = hard reset VMM 1
                               5 = hard reset VMM 2

    (3) – unused

(4) – Data select for input shift register (0 = VMM 1, 1 = VMM 2)
 (See CONFIG TEST registers)

(5) – (6) – unused

(7) INITIALIZE MODE (R/W) – '1' = to initialize selected MODE
 (will reset mode memory address to 0)

(8) – (31) – unused

18. <u>CONFIG MEMORY READ</u> [addr = 44]

 (31) – (0) – DATA from configuration memory (R) - latched when bit 1 of CONFIG
 MEMORY CONTROL REGISTER is asserted

19. <u>CONFIG MEMORY WRITE</u> [addr = 48]

 (31) – (0) – DATA to configuration memory (W) - written when bit 0 of CONFIG
 MEMORY CONTROL REGISTER is asserted

20. <u>CONFIG MEMORY STATUS</u> [addr = 4C]

 (5) – (0) – Current address of configuration memory (R)

 (6) – (7) – unused (read as zeros)

 (10) – (8) – Current mode of access (R) – 0 = write, 1 = read, 2 = configure VMM #1,
 3 = configure VMM #2, 4 = hard reset VMM #1, 5 = hard reset VMM #2

 (11) – (31) – unused (read as zeros)

21. <u>CONFIG TEST 1</u> [addr = 50]

 (31) – (0) – DATA bits (95-64) shifted out of selected VMM during configuration (R).

22. <u>CONFIG TEST 2</u> [addr = 54]

 (31) – (0) – DATA bits (63-32) shifted out of selected VMM during configuration (R).

23. <u>CONFIG TEST 3</u> [addr = 58]

 (31) – (0) – DATA bits (31-0) shifted out of selected VMM during configuration (R).

24. <u>TEST PULSE CONTROL 1</u> [addr = 5C]

(31) – (0) – HIGH portion of pulser period (R/W) – 25 ns per count

25. <u>TEST PULSE CONTROL 2</u> [addr = 60]

    (31) – (0) – LOW portion of pulser period (R/W) – 25 ns per count

26. <u>TEST PULSE CONTROL 3</u> [addr = 64]

    (31) – (0) –NUMBER of pulses to generate (R/W)

27. <u>TEST PULSE DELAY</u> [addr = 68] **???????????**

    (31) – (4) – unused

    (3) – (0) – delay added to CKTP – 12.5 ns per count

28. <u>TEST PULSE SCALER</u> [addr = 6C]

    (31) – (0) – count of pulses generated (R)

29. <u>ENABLE</u> [addr = 70]

    (0) – ENABLE VMM #1 (R/W) – '1' = enable

    (1) – ENABLE VMM #2 (R/W) – '1' = enable

    (2) – (6) – unused

    (7) – CKTP source – '0' = internal pulser, '1' = external trigger   **XX**

    (8) – ENABLE CKTP to VMMs (R/W) – '1' = enable **XX**

    (9) – ENABLE CKBC to VMMs (R/W) – '1' = enable

    (10) – ENABLE CKDT to VMMs (R/W) – '1' = enable

    (11) – (15) – unused

    (16) – ENABLE TRIGGERS (R/W) – '1' = enable

    (17) – ENABLE QUERRY (CKTK) for data in continuous mode (R/W) – '1' = enable **X**

    (18) – TOKEN (TKI) for data in continuous mode (R/W) – '1' = enable **??**

9

(18) – unused

(20) – ENABLE Clock for VMM Direct outputs (R/W) – '1' = enable

(21) – (31) – unused

30. <u>TIMING ERROR CONTROL</u> [addr = 74]

(0) – Capture time error data (W) – '1' = generate pulse

(1) – (30) – unused

(31) – Clear time error data (W) – '1' = generate pulse

31. <u>TIMING ERROR 1</u> [addr = 78]

(31) – (0) – falling edge time error data (R) – channels 31 – 0

32. <u>TIMING ERROR 2</u> [addr = 7C]

(31) – (0) – falling edge time error data (R) – channels 63 – 32

33. <u>TIMING ERROR 3</u> [addr = 80]

(31) – (0) – falling edge time error data (R) – channels 95 – 64

34. <u>TIMING ERROR 4</u> [addr = 84]

(31) – (0) – falling edge time error data (R) – channels 127 – 96

35. <u>TIMING ERROR 5</u> [addr = 88]

(31) – (12) – unused – read as zero
(11) – (8) – falling edge time error data (R) – (D1_1, D0_1), (D1_2, D0_2)
(7) – (4) – unused – read as zero
(3) – (0) – rising edge time error data (R) – (D1_1, D0_1), (D1_2, D0_2)

36. <u>SPARE 4</u> [addr = 8C]

(31) – (0) – unused

37. <u>SPARE 5</u> [addr = 90]

(31) – (0) – unused

38. <u>SPARE 6</u> [addr = 94]

    (31) – (0) – unused

39. <u>SCALER CONTROL 1</u> [addr = 98]

    (6) – (0) – Channel select (0 - 127) for read (R/W)

    (14) – (7) – unused

    (15) – Direct output mode used for scalers (0 = 6 bit ADC, 1 = time pulse)

    (16) – Enable (R/W) – '1' = enable counting in all scalers

    (17) – (31) – unused

40. <u>SCALER CONTROL 2</u> [addr = 9C]

    (0) – Count reset (W) – '1' = reset count in all scalers

    (1) – Latch count for all channels (W) – '1' = latch

    (2) – (31) – unused

41. <u>SCALER DATA</u> [addr = A0]

    (31) – (0) – Scaler count for selected channel (R)

42. <u>SCALER TIME</u> [addr = A4]

    (31) – (0) – Count of clock periods from enable to latch of scalers (R) – 1 count = 3.2us

43. <u>SCALER TRIGGER</u> [addr = A8]

    (31) – (0) – Count of triggers while enabled for acquisition (G0 = '1') (R)

44. <u>SCALER TRAILER 1</u> [addr = AC]

    (31) – (0) – Count of VMM #1 trailers (R)

45. <u>SCALER TRAILER 2</u> [addr = B0]

        (31) – (0) – Count of VMM #2 trailers (R)