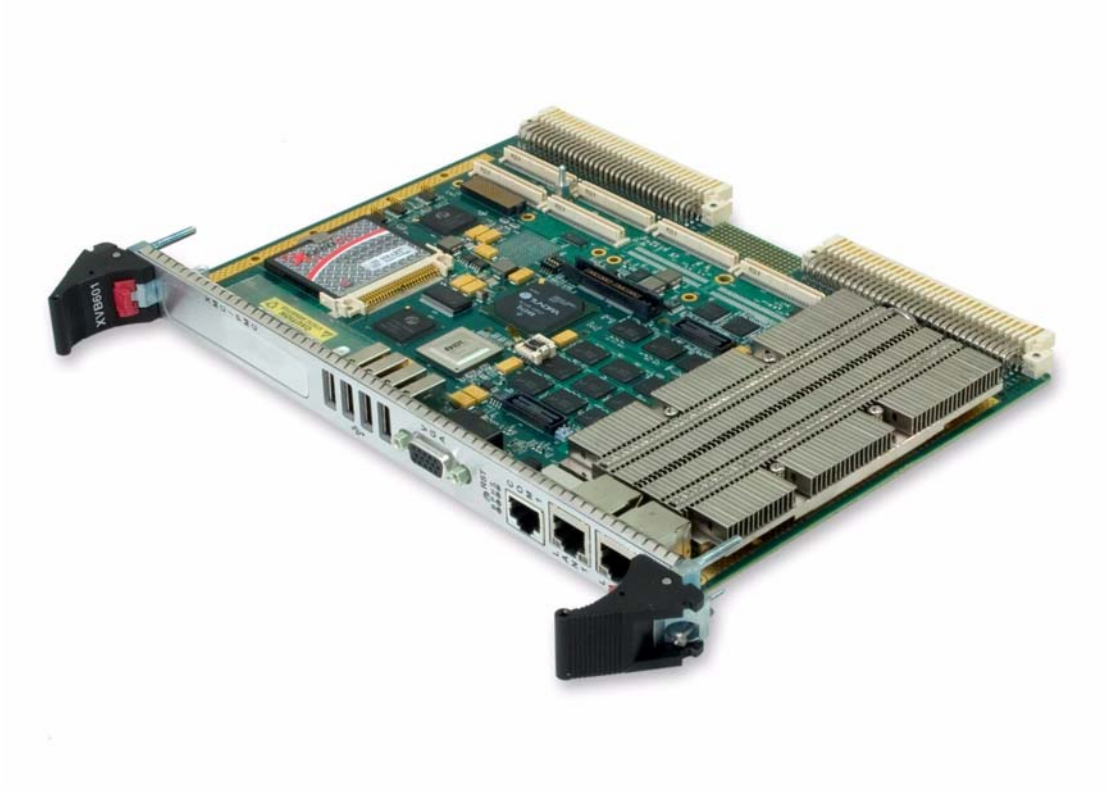
GE
Intelligent Platforms

Hardware Reference

XVB601*

Single Slot VME Single Board Computer

THE XVB601 IS DESIGNED TO MEET THE EUROPEAN UNION (EU) RESTRICTIONS OF HAZARDOUS SUBSTANCE (ROHS) DIRECTIVE (2002/95/EC) CURRENT REVISION.



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Waste Electrical and Electronic Equipment (WEEE) Returns

GE is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

GE will evaluate requests to take back products purchased by our customers before August 13, 2005 on a case by case basis. A WEEE management fee may apply.

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Overview

Introduction

GE Intelligent Platforms' XVB601* is a VMEbus single board computer (SBC) in a single-slot, convection cooled, 6U VME form factor. The XVB601 uses the next generation Intel® Core™ i7 Processor and Mobile Intel QM57 Express Chipset. The XVB601 board, with i7 processor, operates at speeds of 2.53 GHz and 1.06 GHz, supporting up to 8 GBytes of memory. It features dual onboard expansion slots with provision for one PCI-X PMC/x4 PCI Express XMC Card and one PCI-X PMC board. Connectivity includes two front GbE ports, VGA, eight USB ports, DVI and three COM ports.

XVB601 Board Form Factor and Packaging

The XVB601 board assembly is designed to withstand benign environment shock and random vibration, and is offered as a standard temperature product.

The XVB601 board is a single-slot board assembly (233.35mm H x 160mm D x 20.48mm W) meeting the mechanical and electrical requirements defined in the ANSI/VITA 1-1994, ANSI/VITA 1.1-1997, ANSI/VITA-1.5-2003, IEEE STD 1101.2-1992 and ANSI/VITA 20-2001, VITA 30 specifications. Both front panel and rear I/O external interfaces are supported.

- The assembly includes mechanical support and an internal connector to support an add-on PMC carrier board (EXP237*) that creates a two-slot assembly.
- The XVB601 convection option is defined for standard commercial temperature operation in an air cooled chassis.

I/O Options

The XVB601 rear I/O, through P2, is compatible with GE's V7865*, V7768*, and V7875* through the ACC-0603* or ACC-0627* rear transition modules. The ACC-0627 is a new rear transition module that allows access through the rear I/O of the XVB601, including the P0 I/O. The XVB601 also takes advantage of the EXP237 Expansion Carrier Board for additional PMC I/O capability. See **Section 1.8 XVB601 Rear I/O Support** on page 41 for more information on Rear I/O Transition Modules compatible with the XVB601.

XVB601 Features

The XVB601 provides the following core hardware and firmware resources:

- Up to 8 GByte Soldered Memory with ECC
- Dual Gigabit Ethernet via front panel
- Single PMC site option - with USB/VGA
  - One PMC site
  - VGA connector access
  - Four USB ports
- Dual PMC site option - without USB/VGA
- One Front Panel Push button Reset Switch
- DVI via P2, compatible with ACC-0603 or ACC-0627 (rear I/O)
- SATA x2 via P2 compatible with ACC-0603 or ACC-0627
- COM1 via front panel
- COM2 via P2 compatible with ACC-0603 or ACC-0627
- One Front Panel RJ45 connector for COM1 RS232/RS422 from FPGA
- Four general purpose LEDs via front panel
- USB x4 via P2 compatible with ACC-0603 or ACC-0627
- x8 PCIe board to board connector (Mictor) supports EXP237
- One XMC site option available on Front Panel
- Onboard removable battery
- Tsi148 VME Interface
- VMEbus Interface to P1 and P2 per VITA 1-1994,VITA 1.1-1997 and 2eSST per VITA 1.5-2003
- VMEbus P0 connector per ANSI/VITA 1.1-1997 (Optional)
- Core i7 XDP port routed to an American Arium compatible emulator connector
- QM57 Express Chipset XDP port routed to an American Arium compatible emulator connector

Embedded Features

- Remote Boot Agent for all Ethernet ports
- Up to 16 GBytes optional CompactFlash (via PCH SATA channel and SATA to IDE bridge)
- Watchdog, Timers, 128 KByte NVRAM and UART via FPGA
- PMC1 I/O via P0 - 46 pins
- PMC2 I/O via P2 - 46 pins, per VITA 35, compatible with ACC-0603 or ACC-0627
- Dual SATA via P0, compatible with ACC-0627
- GPIO via P0 (FPGA)

The embedded features of the XVB601 are described in **Chapter 3: Embedded PC/ RTOS Features**.

Intel Core i7 Processor and Mobile Intel QM57 Express Chipset

The XVB601 incorporates the latest Intel chipset technology. The IA processor core chipset is built around a Core i7 Dual Core processor with integrated memory controller hub, + the QM57 Express Chipset. Core i7 is the next generation of 64-bit, multi-core mobile processors built on 32-nanometer process technology. The major feature of the Core i7-ECC is the DDR3 memory and graphics controller integration with the Westmere (32nm Nehalem) Dual Core CPU.

Software Support

The XVB601 provides two Core i7 processor cores with a shared memory and I/O resource pool. Customer system applications call for software platforms that support Symmetric Multiprocessing (SMP) operation as well as near real time support of independent application threads.

Generally, these different software needs require the support of multiple operating systems, and also require software driver and Board Support Packages (BSP) to support the low level hardware functions.

Device Driver Strategy

Standard device drivers for the silicon resources are used where possible. The XVB601 software re-uses existing device drivers for features that are common to previous single board computers.

BIOS firmware, Infrastructure Support

The XVB601 includes dual BIOS firmware and OS compatible UART support via FPGA on the LPC bus. The BIOS firmware, provided with the XVB601 includes all functions required by the processor core and chipset. This package also includes the onboard hardware initialization code that is executed following release from reset. The BIOS code is supported via flash devices on the PCH SPI bus.

The BIOS also supports expansion ROM code that supports remote booting from either of the dual Ethernet ports.

Target Operating Systems

The following OS configurations are supported on the XVB601 hardware and software platform:

- Windows XP SP3

NOTE

There is a known issue with certain brands and models of USB CDROM drives where the USB CDROM path is lost during WindowsXP Install to CompactFlash.
Solution:
-Use SATA CD/DVDROM drive.
-Unplug USB mouse and keyboard after first phase of XP install complete and message stating "windows will restart in 15 seconds".
-Plug USB mouse and keyboard into USB port connected to (first/second) USB controller, and the USB CDROM into USB port connected to (second/first) USB controller.
-Paste the drive letter path into the dialog box when XP install states "The file "asms/.../..' on Windows XP Professional Service Pack 3 CD-ROM is needed".

- Linux Fedora 11

NOTE

To get the I^2C and temperature drivers to work under Fedora 11, you need to make a change to /boot/grub/menu.lst, first by adding 'acpi_enforce_resources=no' kernel option. This fixes an ACPI and I^2C conflict and allows the I^2C and temperature probe drivers to work.

- VxWorks 6.6

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January 2010

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Intel® 82574 GbE Controller Family Datasheet
Intel Document Number 317694
October 2009

ACC-0603RC Product Specification
Doc. No. 800-9300800603-000
GE
12090 South Memorial Parkway
Huntsville, AL 35803-3308
(800) 322-3616
www.ge-ip.com

ACC-0603RC VME Rear Transition Module Installation Guide
Doc. No. 522-9300800603-000
GE
12090 South Memorial Parkway
Huntsville, AL 35803-3308
(800) 322-3616
www.ge-ip.com

ACC-0627 VME Rear Transition Module for the XVB601 Installation Guide
Publication No. 522-9300800627-000
GE
12090 South Memorial Parkway
Huntsville, AL 35803-3308
(800) 322-3616
www.ge-ip.com

EXP237 XMC/PMC Carrier Board Hardware Reference Manual
Doc. No. 500-9300000715-000
GE
12090 South Memorial Parkway
Huntsville, AL 35803-3308
(800) 322-3616
www.ge-ip.com

The following documents are continuously updated and are available at http://www.intel.com/products/processor/manuals/

Intel® 64 and IA-32 Architectures Software Developer's Manual Volume 1: Basic Architecture

Intel® 64 and IA-32 Architectures Software Developer's Manual Volume 2A: Instruction Set Reference, A-M

Intel® 64 and IA-32 Architectures Software Developer's Manual Volume 2B: Instruction Set Reference, N-Z

Intel® 64 and IA-32 Architectures Software Developer's Manual Volume 3A: System Programming Guide Part 1

Intel® 64 and IA-32 Architectures Software Developer's Manual Volume 3B: System Programming Guide Part 2

Intel® 64 Architecture x2APIC Specification

Intel® 64 and IA-32 Architectures Application Note TLBs, Paging-Structure Caches, and Their Invalidation

Intel® 64 and IA-32 Architectures Optimization Reference Manual

Organization

This manual is composed of the following chapters and appendices:

Overview provides a general description of the XVB601, References, general Safety Summary and symbols.

Chapter 1 Installation and Setup describes unpacking, handling and installing the hardware, as well as describing external interfaces.

Chapter 2 Standard Features describes the product's standard features and functionality.

Chapter 3 Embedded PC/RTOS Features describes capabilities beyond typical desktop computer systems.

Maintenance provides GE's contact information relative to the care and maintenance of the unit.

Compliance provides information regarding regulatory compliance.

Appendix A: Connectors and Pinouts illustrates and defines the connectors included in the unit's I/O ports.

Appendix B:* BIOS *Setup Utility describes the setup options in the system BIOS firmware.

Appendix C: Specifications and Physical Description lists the hardware specifications for the XVB601.

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

GE assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to GE for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this system.
Use extreme caution when handling, testing and adjusting.

Warnings, Cautions and Notes

WARNING

WARNING denotes a hazard. It calls attention to a procedure, practice, or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

CAUTION denotes a hazard. It calls attention to an operating procedure, practice, or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE

NOTE denotes important information. It calls attention to a procedure, practice, or condition which is essential to highlight.

TIP

Tip denotes a bit of expert information.

LINK

This is link text.

1 • Installation and Setup

This chapter describes the unpacking, handling, installation and front panel of the XVB601.

1.1 Unpacking Procedures

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to GE Customer Care.

1.2 Handling Precautions

CAUTION

Some of the components assembled on GE's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

1.3 Hardware Setup

The XVB601 is factory populated with user-specified options as part of the XVB601 ordering information. Contact Sales for ordering information at 1-800-322-3616. For option upgrades or for any type of repairs, contact customer care to receive a Return Material Authorization (RMA).

GE Customer Care is available at: 1-800-433-2682, 1-780-401-7700.

Or, visit our website at:

www.ge-ip.com

The XVB601 is tested for system operation and shipped with factory-installed header jumpers and switches. The physical locations of the headers and connectors for the SBC with the PMC option are illustrated in **Figure 1-2** ***Top Assembly Switch, Header, Connector Locations*** on page 24. The definitions of the connectors, headers and switches are included in the Table Connectors, Headers and Switches in this Chapter.

All jumpers and switches marked *User Configured* in the following tables may be changed or modified by the user. All jumpers and switches marked *Factory Configured* should not be modified by the user.

Care must be taken when making jumper and switch modifications to ensure against improper settings or connections. Improper settings may result in damage to the unit.

Modifying any jumper and switch not marked *User Configured* will void the Warranty and may damage the unit.

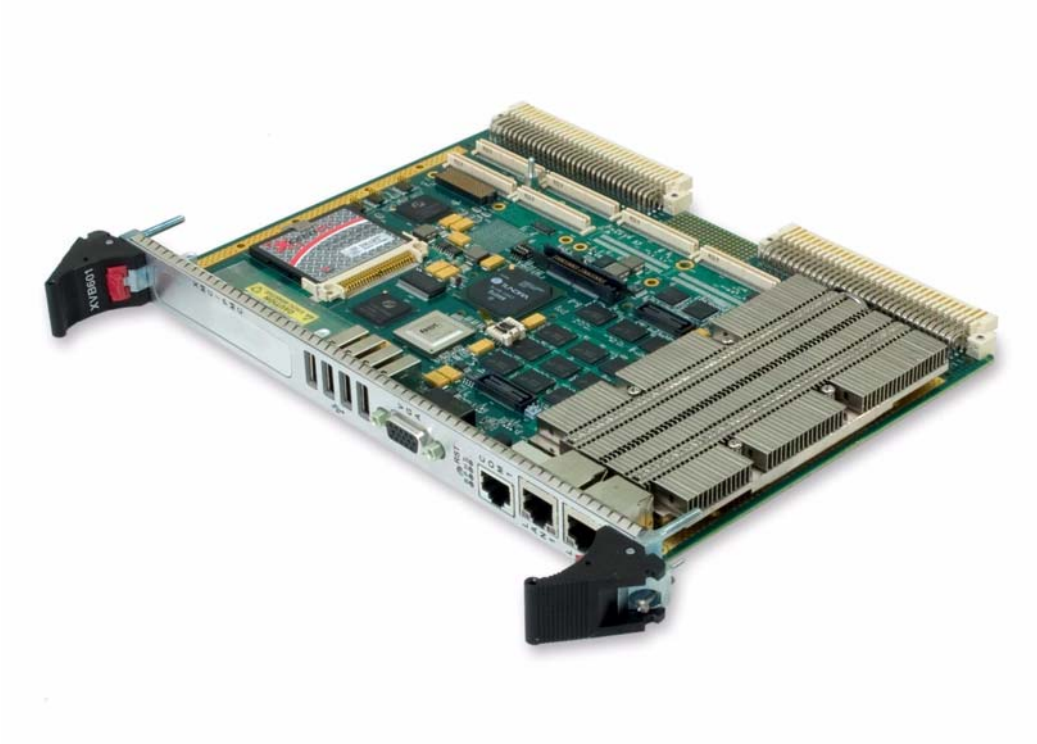
1.4 Mechanical Layout

The XVB601 is constructed as a single 6U VME board with multiple optional modules or mezzanines that meets the mechanical and electrical requirements defined in the VITA 1-1994 specification.

The assembly includes mechanical support and an internal connector to support an add-on PMC carrier board (EXP237) to create a two-slot assembly.

The main board is shown below:

Figure 1-1 XVB601 Main Board 1 PMC Slot



For installation instructions, see Section **1.5** ***Installation of XVB601 into Chassis*** on page 32 and Section **1.6** ***Installing or Removing a PMC Card*** on page 33.

The XVB601 Top and Bottom Assembly are illustrated in the following figures:

Figure 1-2 Top Assembly Switch, Header, Connector Locations

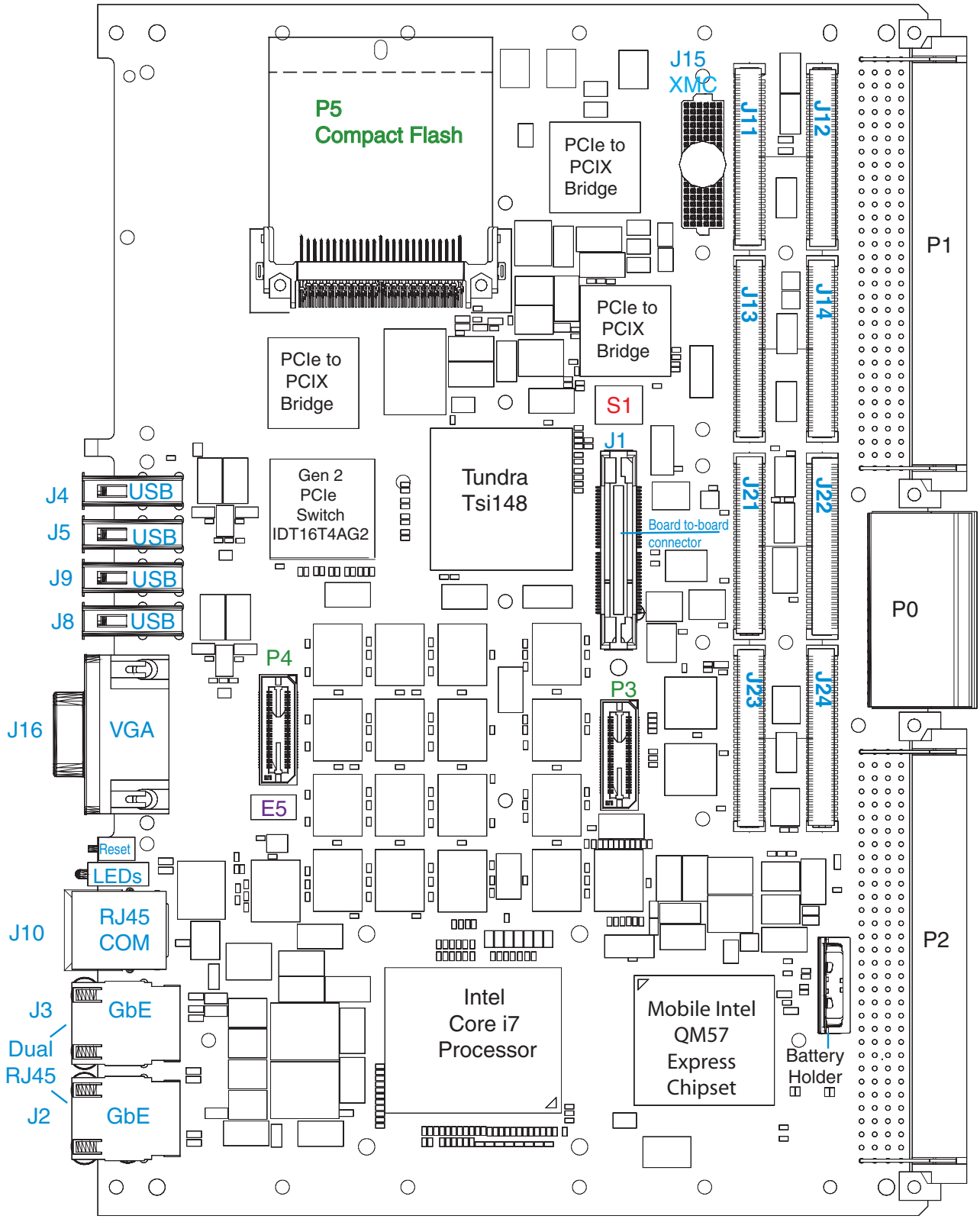


Figure 1-3 Bottom Assembly Switch Locations

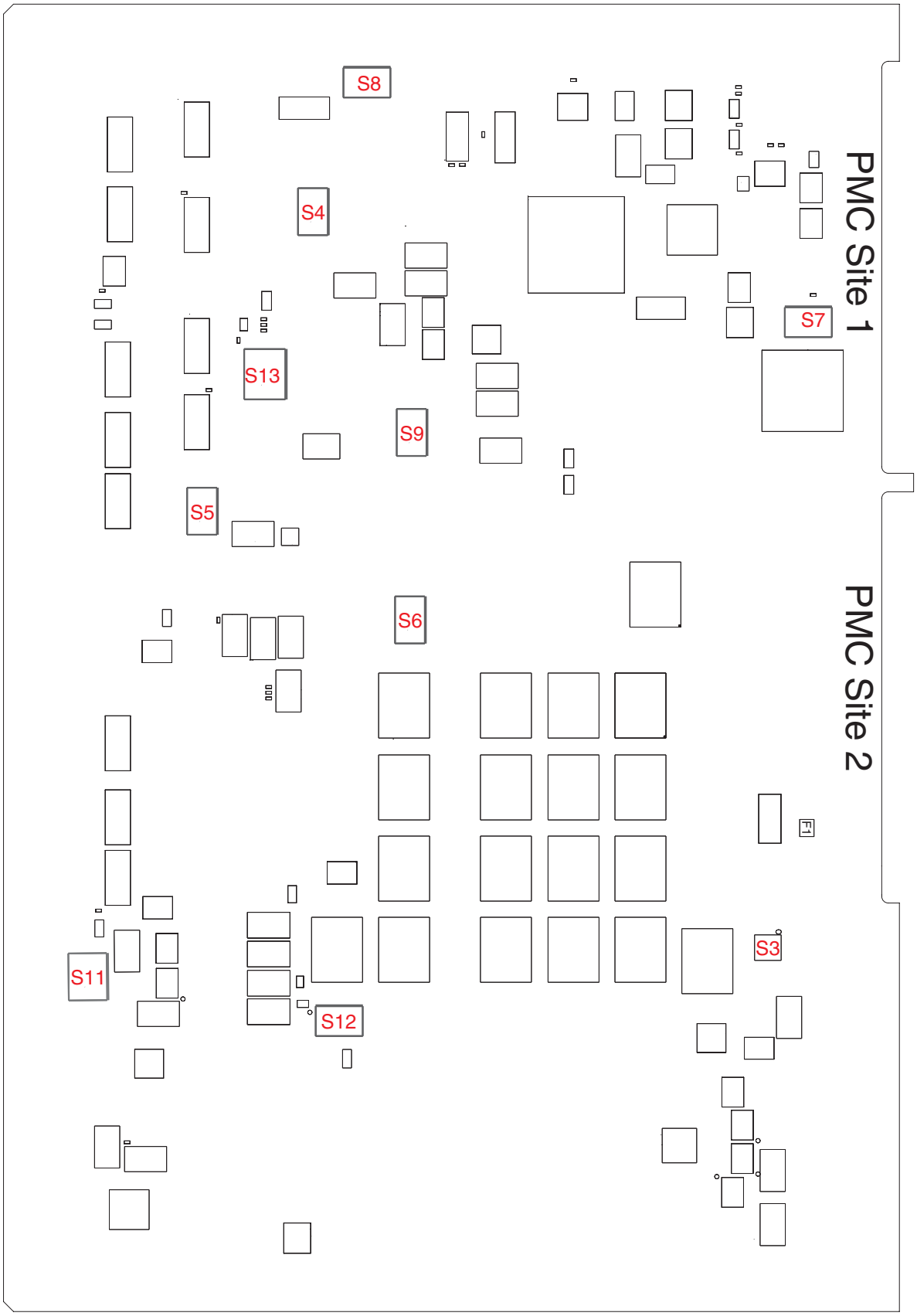


Table 1-1 Connectors, Header, Switches

Connector	Function
P0	Interface Connector (optional)
P1	VME Interface Connector
P2	USB 2.0, Serial ATA, COM2
P3	XDP Port
P4	XDP Port
P5	CompactFlash Socket
J1	Board to Board Connector for EXP237
J2, J3	LAN1 and LAN2 Gigabit Ethernet Connector (Dual RJ45)
J4, J5, J8, J9	USB Ports
J10	Serial Port Connector (COM1)
J11, J12, J13 and J14	PMC Site 1 Connectors
J15	XMC Site Connector
J16	VGA
J21, J22, J23, J24	PMC Site 2 Connectors
Header	**Function**
E5	Front Panel COMPort Signal Configuration
Switches	**Function**
S1	XMC SMBus ID/SMBus to XMC Enable/Disable
S3	COM1 (RS422 Ohm Termination)
S4	VME SYSRST In/Out Enable/Disable
S5	Tsi148 VMEbus SFAILEN Control and Status
S6	Tsi148 VMEbus Auto/Geographic Enable
S7	JTAG Enable/Disable
S8	Front Panel COM Port 232/422 Driver Configuration
S9	SYSCON Control
S11	Flash Desc. Override/Battery Enable
S12	RTC Reset
S13	XMC Write Prohibit (MVMRO)

NOTE

Default settings for switches are displayed in bold in the tables that follow.

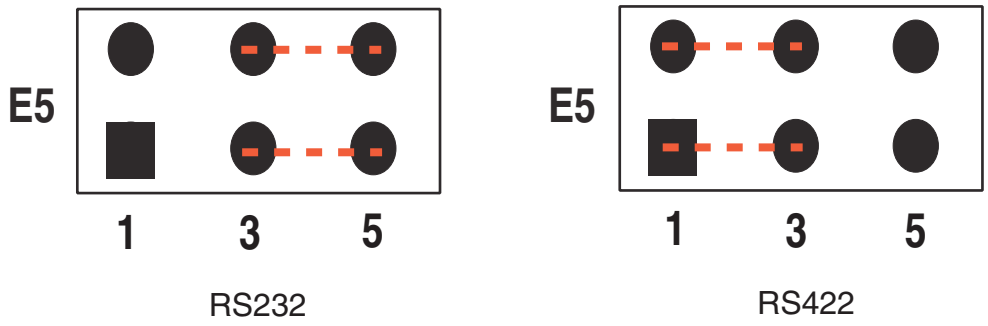
1.4.1 Top Assembly Switch and Header Locations

Switch 1 and Header E5 are located on the top assembly of the XVB601 board. **Table 1-2** describes the positions and state of Switch 1. Header E5 is displayed in **Figure 1-4** ***Header E5 Front Panel COM Port 232/422 Signal Configuration*** on page 27. **Table 1-3** describes the positions of the COM1 Configuration, Header E5.

Table 1-2 Switch 1 (S1) XMC SMB ID/SMB to XMC Enable/Disable

Position	State
1 Off	**XMC SMBus ID 0 (Default)**
1 On	XMC SMBus ID 0
2 Off	**XMC SMBus ID 1 (Default)**
2 On	XMC SMBus ID 1
3 Off	**XMC SMBus ID 2 (Default)**
3 On	XMC SMBus ID 2
4 Off	Enable SMBus to XMC
4 On	**Disable SMBus to XMC (Default)**

Figure 1-4 Header E5 Front Panel COM Port 232/422 Signal Configuration



NOTE

232 Default

Table 1-3 COM1 Configuration (RS232/RS422 Select) - Header (E5) User Configurable

Select	S8 State	E5 Position	S3 State
RS232	**1-4 ON and 2-3 ON**	**3-5, 4-6**	**1-4 and 2-3 both OFF**
RS422 w/Termination	1-4 and 2-3 both OFF	1-3, 2-4	1-4 and 2-3 both ON
RS422 w/o Termination	1-4 and 2-3 both OFF	1-3, 2-4	1-4 and 2-3 both OFF

1.4.2 Bottom Assembly Switch Locations

The following Tables describe the positions and states of switches located on the bottom assembly of the XVB601 board. See **Figure 1-3** ***Bottom Assembly Switch Locations*** on page 25.

Table 1-4 Switch S3 RS422; 120 Ohm Termination Configuration (User Configurable)

Position	State	Function
1	**Off**	**Disable Rx Termination (Default)**
1	On	Enable Rx Termination
2	**Off**	**Disable CTS Termination (Default)**
2	On	Enable CTS Termination

Table 1-5 Switch S4 VME SYSRST In/Out Enable/Disable (User Configurable)

Position	State	Function
1	Off	Disable VME SYSRST Driver
1	**On**	**Enable VME SYSRST Driver (Default)**
2	Off	Disable VME SYSRST Receiver
2	**On**	**Enable VME SYSRST Receiver (Default)**

Table 1-6 Switches S5 and S6 Tsi148 Powerup Options (User Configurable)

Select	Switch S5		Switch S6	
1 = VD[0]	**On (Default)**			
2 = VD[1]	**On (Default)**			
1 = VD[2]			**On (Default)**	
2 = VD[3]			**On (Default)**	
Description	Power-up Option	VMEbus Data Signal	Control Register	Detailed Information
SFAILEN Control Bit Reset Value	SFAILEN_RV	VD[0]	Control and Status Register • SFAILEN bit	System Fail Enable (SFAILEN) Configuration
SFAILAI Control Bit Auto Clear	SFAILAI_AC	VD[1]	VMEbus Control Register • SFAILAI bit	Auto Slot ID Operation
Auto Slot ID Enable	ASIDEN	VD[2]	None - power-up option only	Auto Slot ID Operation
Geographic Slot ID Enable	GSIDEN	VD[3]	None - power-up option only	Geographic Slot ID Enable

Table 1-7 Switches S5 and S6 CR/CSR Base Address Configuration (User Configurable)

Select	Switch 5	Switch 6
1 = VD[0]	**On (Default)**	
2 = VD[1]	**On (Default)**	
1 = VD[2]		**On (Default)**
2 = VD[3]		**On (Default)**
VD [3:0]	GA (All High)	Description
00X0	X	CR/CSR disabled CRAT register, EN cleared by S reset VCTRL register, SFAILAI cleared by S reset GCTRL register, SFAILEN cleared by S reset
00X1	X	CR/CSR disabled CRAT.EN cleared by S reset VCTRL.SFAILAI cleared by S reset GCTRL register, SFAILEN set by S reset
0100	X	Auto Slot ID CRAT register, EN cleared by S reset VCTRL register, SFAILAI set by S reset GCTRL register, SFAILEN cleared by S reset
01X1	X	Illegal Configuration
0110	X	Auto Slot ID CRAT register, EN cleared by S reset VCTRL register, SFAILAI set by S reset, cleared 1ms after S reset GCTRL register, SFAILEN cleared by S reset
VD [3:0]	GA (All High)	Description
10X0	X	Geographical Addressing CRAT register, EN set by S reset VCTRL register, SFAILAI cleared by S reset GCTRL register, SFAILEN cleared by S reset
10X1	X	Geographical Addressing CRAT register, EN set by S reset VCTRL register, SFAILAI cleared by S reset GCTRL register, SFAILEN set by S reset
11X0	0	Geographical Addressing CRAT register, EN set by S reset VCTRL register, SFAILAI cleared by S reset GCTRL register, SFAILEN set by S reset
11X1	X	Illegal Configuration
1100	1	Default to Auto Slot ID CRAT register, EN cleared by S reset VCTRL register, SFAILAI set by S reset, cleared 1 ms after S reset GCTRL register, SFAILEN cleared by S reset
1110	1	Default to Auto Slot ID CRAT register, EN cleared by S reset VCTRL register, SFAILAI set by S reset, cleared 1 ms after S reset GCTRL register, SFAILEN cleared by S reset

Table 1-8 Switch S7 JTAG Enable/Disable (User Configurable)

Position	State	Function
1	**Off**	**Disable JTAG (Default)**
1	On	Enable JTAG
2	**Off**	**Factory Use Only (Default)**
2	On	Factory Use Only

Table 1-9 Switch S8 Front Panel COM Port 232/422 Driver

Position	State	Function
1	Off	422/485 Mode
1	**On**	**232 Mode (Default)**
2	**Off**	**Factory Use Only (Default)**
2	On	Factory Use Only

Table 1-10 Switch S9 System Controller (User Configurable)

Position	State	Position	State	Function
1	Off	2	On	Force Syscon Disable
1	On	2	Off	Force Syscon Enable
1	**Off**	**2**	**Off**	**AutoSyscon (Default)**
1	On	2	On	Force Syscon Disable

Table 1-11 Switch S11 Flash Descriptor Override/Battery Enable (User Configurable)

Position	State	Function
1	**Off**	**Disable Flash Descriptor Override (Default)**
1	On	Enable Flash Descriptor Override
2	Off	Disconnect Battery
2	**On**	**Connect Battery (Default)**

Table 1-12 Switch S13 XMC Write Prohibit (MVMRO) (**Not** User Configurable)

Position	State	Function
1	**Off**	**Disable Writes to XMC NV Memory (Default)**
1	On	Enables Writes to XMC NV Memory
2	**Off**	**Factory Use Only (Default)**
2	On	Factory Use Only

1.4.3 Clear CMOS/RTC/Password

NOTE

The BIOS has the capability of password protecting casual access to the unit's CMOS setup screens. The CMOS Clear switch allows the user to clear the password in the case of a forgotten password. This will also clear all CMOS settings and restore factory defaults.

To clear the CMOS password:

1. Turn off power to the unit.
2. Move switch S12 position 1 to On.
3. Wait approximately five seconds.
4. Move switch S12 position 1 to Off.
5. Power up the unit.

When power is reapplied to the unit, the CMOS password will be cleared, and the CMOS will be set to its defaults.

1.5 Installation of XVB601 into Chassis

The XVB601 conforms to the VME physical specification for a 6U board. The XVB601 can be used as the system controller or as a peripheral board. It can be plugged directly into any standard chassis accepting either type of board.

CAUTION

Do not install or remove the board while power is applied.

The following steps describe the GE recommended method for installation and powerup of the XVB601:

1. Make sure power to the equipment is off.
2. Connect a PMC or an XMC module to the XVB601 (if it is to be used) prior to board installation. See **1.6 *Installing or Removing a PMC Card*** on page 33. Refer to the Product Manual for the XMC/PMC module for configuration and setup.

NOTE

Air flow as measured at the output side of the heatsink is to be greater than 450 LFM.

3. Choose chassis slot. The XVB601 must be attached to a P1/P2 VME backplane. In some cases, an XVB601 with a P0 connector installed will not plug into a standard VME backplane.
   a. If the XVB601 is to be the VME system controller, choose the first VME slot.
   b. If a different board is the VME system controller, choose any slot ***except*** Slot One.

      The XVB601 does not require jumpers for enabling/disabling the system controller function.

      See S9 switch settings to force system controller settings
4. Insert the XVB601 into a VME chassis system controller or peripheral slot.
   a. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector.
   b. Use the ejector handles to firmly seat the board.
5. Access all needed peripherals from the front panel or the rear I/O. Each connector is clearly labeled. Detailed pinouts are in ***Appendix A: Connectors and Pinouts***.
6. Connect a keyboard and mouse if the system has not been previously configured.
7. Refer to Section **3.4 *CompactFlash,*** page 85 for setup details, if applicable. The XVB601 features an optional CompactFlash Disk resident on the board.
8. If an external drive module is installed, the BIOS Boot Setup Menu or F7 first boot key may be used to select booting from the drive. If applicable, see Appendix B.
9. Install the operating system according to the manufacturer's instructions, if a drive module is present.

1.5.1 BIOS Setup

The XVB601 has an onboard BIOS Setup program that controls many configuration options. These options are saved in a special non-volatile, battery-backed memory chip and are collectively referred to as the board's CMOS Configuration. The CMOS configuration controls many details concerning the behavior of the hardware from the moment power is applied. The CMOS clear switch clears BIOS settings to factory defaults.

Details of the XVB601 BIOS setup program are included in ***Appendix B: BIOS Setup Utility***.

NOTE
The BIOS referred to in this Manual is an EFI BIOS.

1.6 Installing or Removing a PMC Card

The XVB601 incorporates PMC expansion sites that support the PCI-X bus. The PMC sites are on a private PCI-X bus segment allowing for maximum data transfer rates of 1064 MByte/s between the processors and the PMC device. The PMC sites are capable of up to 133 MHz operation and support 3.3 V (and 5 V) signaling (or VIO). They are compatible with the earlier PCI interface versions (33/66 MHz, 32/64-bit).

NOTE
For best performance, PMC card drivers should use DMA.

The following procedure is applicable for both removal and installation of PMC modules and fully populated PMC cards. See **Figure 1-5** ***PMC Installed onto XVB601 1-PMC Site Model*** on page 34 and **Figure 1-6** ***PMC Installed onto XVB601 2-PMC Site Model*** on page 34.

1. Remove the mezzanine screws.
2. Separate the mezzanine connector while lifting and rotating the mezzanine board. Pull away from the front panel.
3. Remove the PMC modules by removing two mounting screws per module. This step will be necessary when initially installing a PMC card into a XVB601.

Follow the reverse sequence to install a PMC card or a PMC module.

1.6.1 Installing 3.3 V or 5.0 V VIO Keypin

The XVB601 supports both 3.3 V and 5.0 V VIO via the placement of the PMC keypin.

Figure 1-5 PMC Installed onto XVB601 1-PMC Site Model

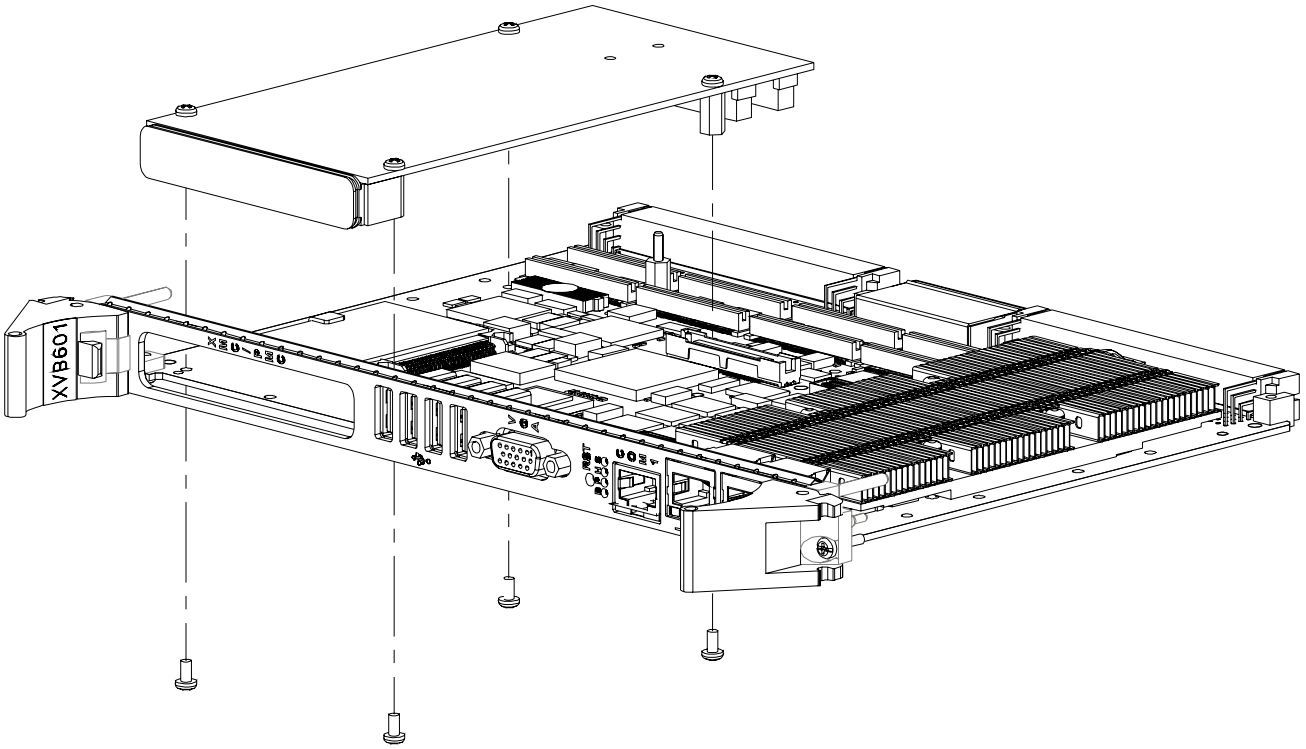
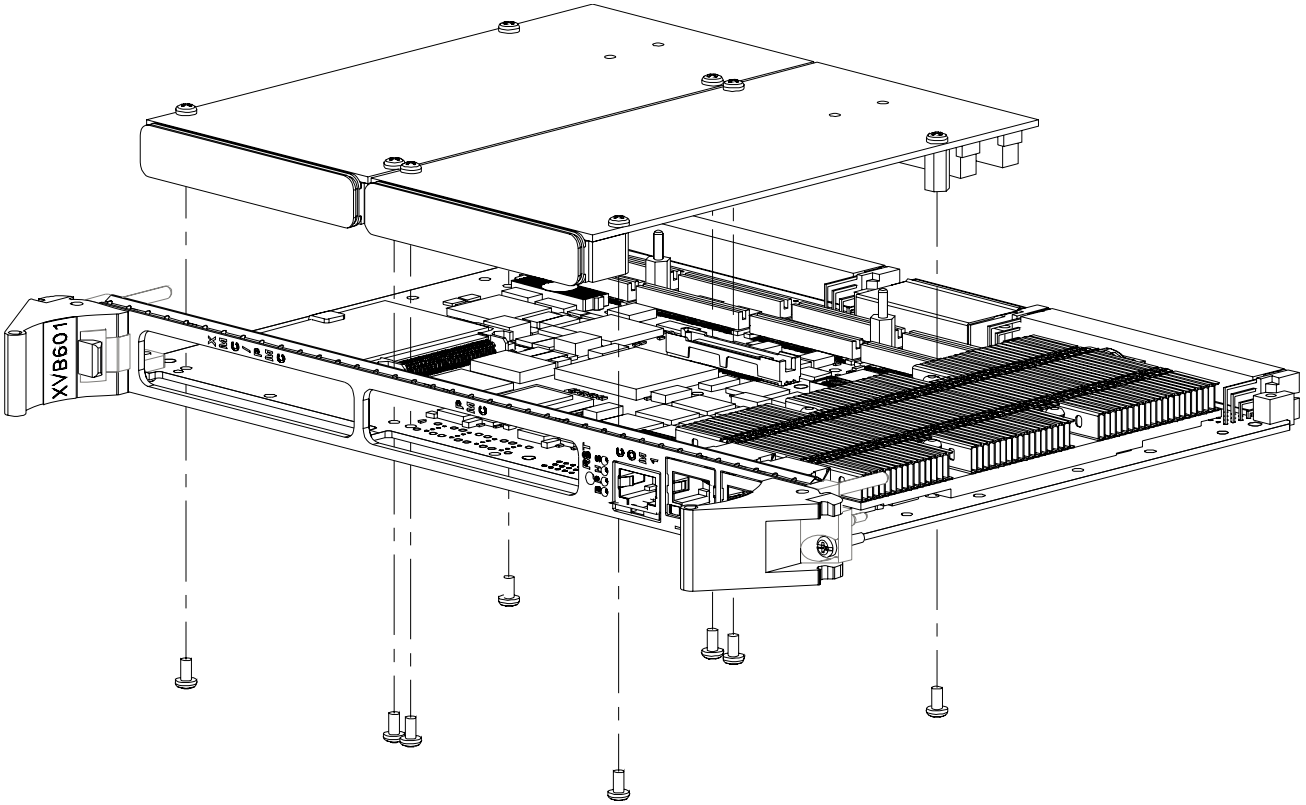


Figure 1-6 PMC Installed onto XVB601 2-PMC Site Model



1.7 Front Panel of XVB601

1.7.1 Connectors

On the 1-PMC Front Panel site option, the XVB601 provides front panel access to the XMC/PMC expansion site, four USB Serial Ports, the VGA Video connector, the manual reset switch, four status LEDs, COM1 port, two GbE connectors. A drawing of the XVB601 front panel is shown in **Figure 1-7** ***Front Panel Layout/ LED Status (1 PMC Site) XVB601*** on page 36.

The front panel connectors and indicators are labeled as follows:

- XMC/PMC XMC/PMC slot
- Ψ USB Connectors
- VGA VGA connector
- RST Manual reset switch
- BPHS Status LEDs
- COM1 COM port
- LAN1 GbE Connector, Front
- LAN2 GbE Connector, Front

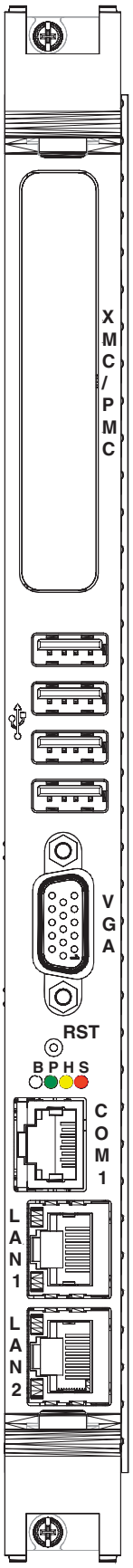
On the 2-PMC Front Panel site option, the XVB601 provides front panel access to:

- XMC/PMC XMC/PMC slot
- PMC Second PMC slot
- RST Manual reset switch
- BPHS Status LEDs
- COM1 COM port
- LAN1 GbE Connector, Front
- LAN2 GbE Connector, Front

NOTE

If a board reset is required via the manual reset switch, ensure that the switch is not repeatedly pressed during the power up/reset cycle.

Figure 1-7 Front Panel Layout/LED Status (1 PMC Site) XVB601



XMC-PMC Site

Ψ – Quad USB Serial Ports

VGA - Video Graphics Array Connector access

RST - Reset allows the system to be reset from the front panel

BPHS Status LEDs

All four front panel LEDs illuminate when the Processor/ICH are in the S5 Power Management state.

B Boot Done - Indicates BIOS powerup self test (POST) is in progress, LED is lit (Red LED). Once POST completes, LED turns off.

P Power Good - Indicates when all onboard power is within tolerance (Green LED).

H Drive Activity - Indicates hard drive activity on either one of the SATA or CompactFlash drives (Yellow LED).

S VME SYSFAIL* Indicates when the VME SYSFAIL* signal is asserted (Red LED).

COM1 -Communications port (RS232 or RS422 serial link interface)

LAN1 - 10/100/1000 Mbit Ethernet Connector

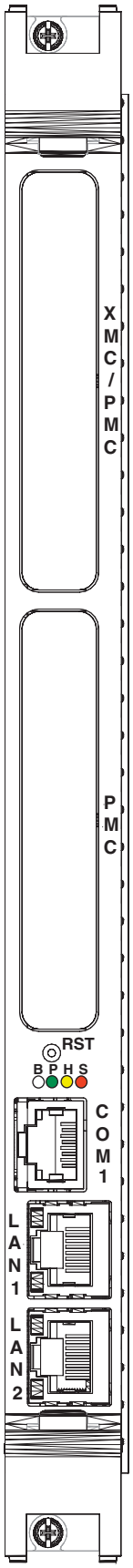
LAN2 - 10/100/1000 Mbit Ethernet Connector

Ethernet Activity: L - Blinks green when the Ethernet is linked and active. It remains steady if the Ethernet is linked, with no activity.

Ethernet Speed: S - Indicates at which speed the Ethernet is running:

10Base-T: LED is off
100Base-TX: Yellow LED
1000Base-T: Green LED

Figure 1-8 Front Panel Layout/LED Status (2 PMC Sites) XVB601



XMC/PMC Site

PMC Site

RST - Reset allows the system to be reset from the front panel

BPHS Status LEDs

All four front panel LEDs illuminate when the Processor/ICH are in the S5 Power Management state.

B Boot Done - Indicates BIOS powerup self test (POST) is in progress, LED is lit (Red LED). Once POST completes, LED turns off.

P Power Good - Indicates when all onboard power is within tolerance (Green LED).

H Drive Activity - Indicates hard drive activity on either one of the SATA or CompactFlash drives (Yellow LED).

S VME SYSFAIL* Indicates when the VME SYSFAIL* signal is asserted (Red LED).

COM1 -Communications port (RS232 or RS422 serial link interface)

LAN1 - 10/100/1000 Mbit Ethernet Connector

LAN2 - 10/100/1000 Mbit Ethernet Connector

Ethernet Activity: L - Blinks green when the Ethernet is linked and active. It remains steady if the Ethernet is linked, with no activity.

Ethernet Speed: S - Indicates at which speed the Ethernet is running:

10Base-T: LED is off
100Base-TX: Yellow LED
1000Base-T: Green LED

1.7.2 LEDs

Front Panel Indicators

The XVB601 front panel provides the following indicators:

The four general status LEDs provide status information as follows (left to right on the panel):

- Boot status (RED): illuminates during BIOS boot and power-on self test operation only
- Power (GREEN): illuminates when all internal rail voltages are within operating tolerances
- Drive Activity (YELLOW): illuminates while S-ATA drive accesses are in progress
- VME SYSFAIL (RED): illuminates when SYSFAIL is asserted on the backplane bus

When the Processor/PCH are in the S5 Power Management state, all four front panel LEDs illuminate.

The two LEDs integrated in the RJ45 receptacle for GbE ports provide link activity and link speed status information for the Ethernet ports on XVB601 as follows (left to right on the panel):

- Link Activity [GREEN]: illuminates during link, flashing during active data transfers on the port
- Link Speed [YELLOW/GREEN]: link speed is 1 Gb/s when Green, 100 Mb/s when yellow, 10 Mb/s when extinguished

The Reset switch is a standard push-button. When activated, this switch forces a hardware reset to the XVB601 assembly.

Signal assignments for the front panel connectors are provided in ***Appendix A: Connectors and Pinouts***.

Figure 1-9 Front Panel XVB601 Isometric View (1 PMC Slot)

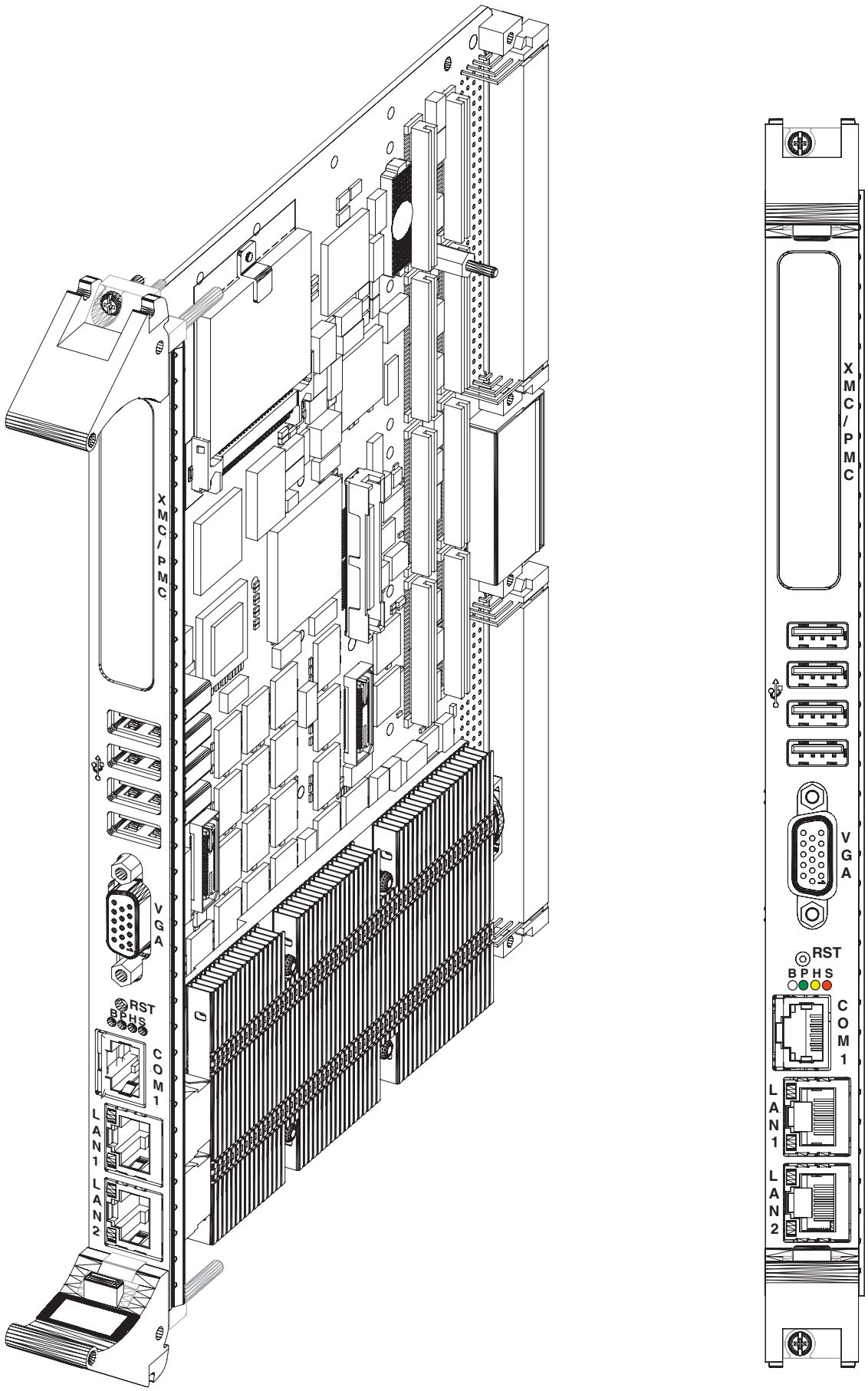
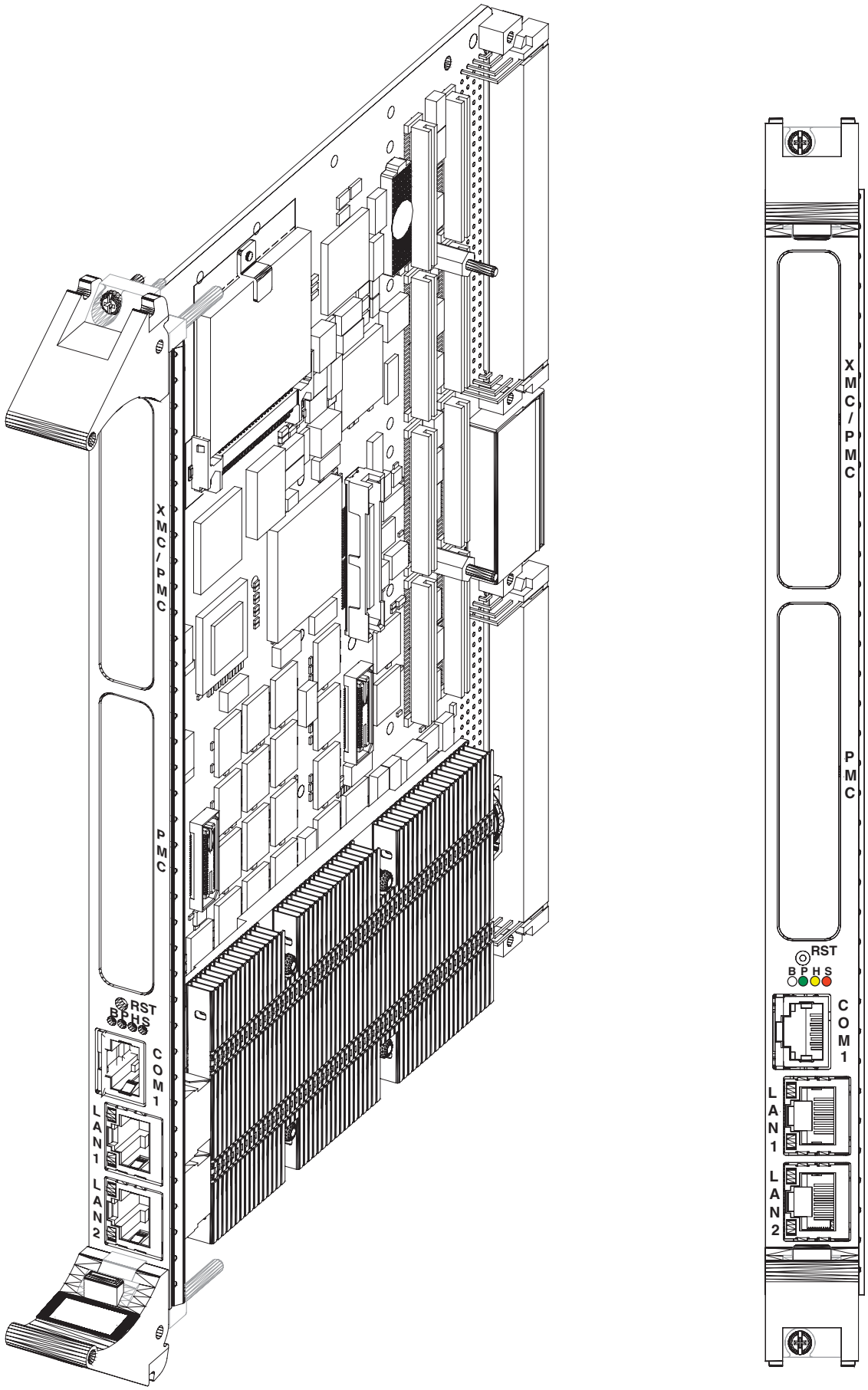


Figure 1-10 Front Panel XVB601 (2 PMC Slot) Isometric View



1.8 XVB601 Rear I/O Support

The XVB601 provides rear I/O support for VME with 2eSST 320MB/s, DVI via P2, four USB ports, COM2 (RS232/RS422), and up to four SATA drives and eight GPIOs.

These signals are accessed by the use of a rear transition module (RTM), such as the ACC-0627 or ACC-0603RC, which terminates the signals into industry standard connectors. Connector pinouts and orientation for the XVB601, are defined in ***Appendix A: Connectors and Pinouts***.

RTMs may not support all available XVB601 rear I/O mentioned above. RTM connections are defined in the appropriate RTM Installation Guides that are described in the following section.

1.8.1 Rear Transition Modules Compatible with XVB601

The XVB601 processor board is designed to support the following existing products:

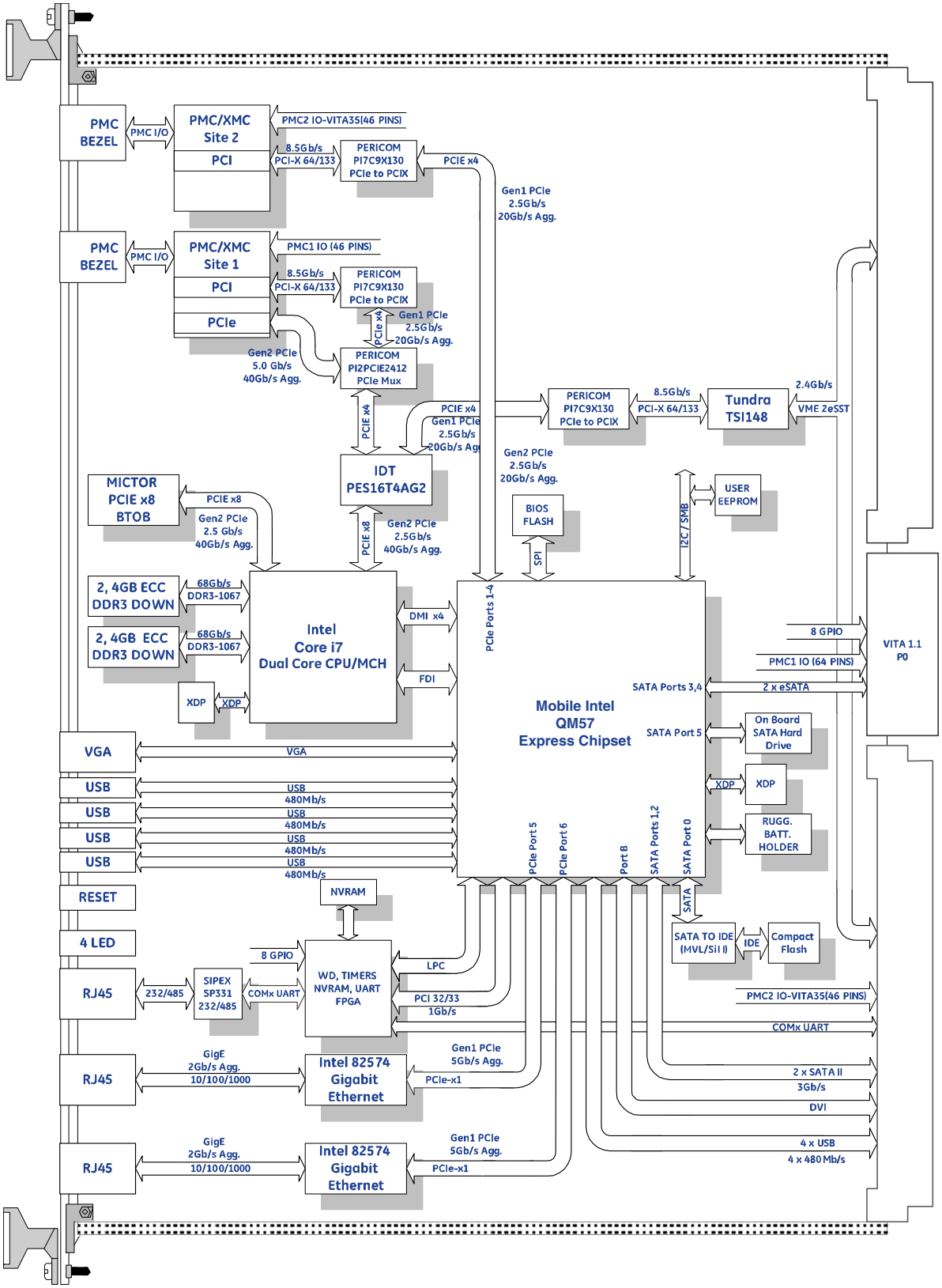
- ACC-0603 rear transition module
- ACC-0627 rear transition module (with P0 connector). The ACC-0627 RTM is functionally very close to the ACC-0603. Major differences are the option loading of the PIM connectors, inclusion of optional P0 connector and SATA re-drivers, and adding two more USB connectors to the front panel.

1.9 BIOS Setup

The XVB601 has an onboard BIOS Setup program that controls many configuration options. These options are saved in non-volatile, battery-backed memory and are collectively referred to as the board's "CMOS Configuration." The CMOS configuration controls many details concerning the behavior of the hardware from the moment power is applied. The CMOS clear switch, S12, clears BIOS settings to factory defaults.

If applicable: See ***Appendix B: BIOS Setup Utility*** setup details.

Figure 2-1 Functional Block Diagram XVB601



2.1 Functional Definitions

2.1.1 IA Processor Core Chipset

The IA processor core chipset is built around the Core i7 Dual Core processor with integrated memory controller hub, + the QM57 Express Chipset. The Core i7 integrated processor functions are as follows:

- Two SKUs (2.53 GHz 37W and 1.0 GHz 17W)
- Four MBytes of L2 cache in addition to L1 instruction and data caches.
- Integrated two channel DDR3-1067 memory controller supports optional error correction code (ECC) check word generation or checking
- 2D display operations on video data as well as 3D display operations, and includes FDI output interface to the QM57 Chipset that supports DVI, and VGA displays
- PCI Express (PCIe) Graphics port for onboard PCIe devices as well as PCIe expansion.
- BGA package

2.1.2 QM57 Express Chipset

The QM57 Express Chipset contains a DMI serial link interface to the Core i7 processors plus internal logic to control data transfers between the Core i7 memory controller and the various I/O and local peripheral resources.

External serial link and parallel bus functions of the QM57 Chipset include:

- Generation 1 x1 or X4 PCIe serial links, running at 2.5 Gb/s
- Generation 2 PCIe running at 2.5 Gb/s
- USB 2.0 serial links
- Generation 2 SATA serial links running at 3.0 Gb/s
- LPC bus
- SPI bus
- SMBus
- PCI 32 bit 33 MHz bus
- SVGA and DVI video ports
- Flexible Display Interface (FDI)
- PECI Interface
- Requires External Battery support or VME +5 V Standby power circuit support for RTC/CMOS

The QM57 Express Chipset also includes a number of local processor peripheral resources, including general purpose timers, an interrupt controller, a Real-Time Clock (RTC) circuit, and a GPIO port controller. See the Section *Software Support* on page 13.

2.1.3 Main Memory Array

The main memory array on XVB601 is as follows:

- Two channels of DDR3-1067 SDRAM components on a 72-bit data bus with ECC support (Total of 8 GBytes max).
- Bank 0 is a 4 GByte maximum array on Channel 0 with components soldered to the main XVB601 PCB. Bank 1 is a 4 GByte maximum array on Channel 1 with components soldered to the main XVB601 PCB.
- Memory Options at 4 GByte and 8 GByte (Symmetric)

CAUTION

Caution must be used when sharing memory between the local processor and the VME to prevent a VME deadlock and to prevent a VME master from overwriting the local processor's operating system.

CAUTION

The XVB601 includes 128 KByte of non-volatile SRAM which can be accessed by the CPU at any time, and is used to store system data that must not be lost during power-off conditions.

2.1.4 LPC Bus Resources

The LPC bus on XVB601 supports the following resources:

- FPGA with two Standard UARTs that terminate at the front panel (COM1) and rear access (COM2) for use with RS232/422 COM ports

2.1.5 PCI-Express Serial Link Resources

The PCI-Express root controller on the QM57 Chipset hosts the following:

- Two Gigabit Ethernet MAC / PHY devices each on a x1 PCH PCI-Express serial link (supports remote boot)
- PMC Site #2, via a x4 PCH PCI Express link

The PCI-Express root controller on the Core i7 hosts the following:

- x8 Gen 2 Core i7 PCI-Express serial link to a Mictor expansion connector for supporting the EXP237 expansion card
- x8 Gen 2 Core i7 PCI-Express serial link divided by a PCI-E switch into two x4 PCI-E links. One x4 link supports PMC/XMC site #1. The second x4 link supports the Tsi148 VME interface using a PCI-E to PCI-X bridge.

2.1.6 PCI Local Bus Resources

The PCI local bus segment on the XVB601 is a 32-bit/33 MHz bus, with VIO defined to be 3.3 V. The QM57 Chipset PCI bus interface serves as the root controller / master of this segment, which contains target devices, as follows:

- One FPGA (PCI Target only) including 128 KByte (minimum) NVRAM, HW registers, two 16-bit and two 32-bit general purpose (GP) timers, and a Watchdog Timer

2.1.7 CompactFlash Module Site

The XVB601 assembly includes one Type 1 CompactFlash module site supporting up to 16 GByte.

- The SATA to IDE bridge is used to convert the QM57 Chipset SATA port to an EIDE CompactFlash bus interface.
- The CompactFlash site is capable of hosting CompactFlash memory modules with bus interfaces ranging up to UDMA-100.

2.1.8 Onboard Hard Disk Drive

The XVB601 assembly includes support for a future onboard SATA hard disk drive.

- The QM57 Chipset SATA channel is routed to the I/O connector of PMC site 1. This allows a low cost SATA Hard drive module to mount onto the PMC site that supports an onboard disk drive.

2.1.9 SPI bus resources

The XVB601 supports BIOS firmware, code using the QM57 Chipset SPI bus channel.

- The BIOS firmware is contained in one 4 MByte size SPI bus Flash part. The SPI flash parts can be in-circuit programmed with updates after initial programming of the SPI bus parts occurs off of the unit.

2.1.10 I^2C/SMBus resources

The XVB601 assembly includes support for I^2C/SMBus devices

- Two Serial EEPROMs, one each supporting the two DDR3 memory channels
- One Serial EEPROM for user data

2.2 External Interfaces

As noted in the Overview, the XVB601 board layout supports convection cooled mechanicals that supports both front panel and rear I/O external interfaces. This section provides an overview of the functionality associated at each port, while detailed signal assignments on the backplane connectors are provided in ***Appendix A: Connectors and Pinouts***.

The front panel also includes six status LEDs. The functional definition for each LED is provided in section ***1.7.2 LEDs,*** page 38.

2.2.1 Front Panel USB Ports

- Four USB ports on the front panel are a Type A (host) interface, capable of supporting USB 1.0, 1.1, and 2.0 targets. These ports terminate at the QM57 Chipset peripheral controller in the core chipset.
- Front Panel USB Ports are capable of supporting 1.5A power.

2.2.2 Front Panel GbE Ports

- Two 10/100/1000Base-T Ethernet Ports. Each of these ports terminate at an Ethernet MAC / PHY device (Intel 82574 or equivalent).
- The RJ45 receptacles used at these ports include two status LEDs, which provide link status and activity indications as defined in **section *1.7.2 LEDs,*** page 38**.**
- Both GbE ports support remote boot from either the Front or Rear configuration.

2.2.3 Front Panel Serial Port

- RJ45 connector for the COM1 serial port from the onboard FPGA. The port supports RS232/422 signaling as set by onboard switches or jumpers.

2.2.4 Front Panel Video Port

- Standard DB15 connector interface for the (S)VGA output of the PCH. The port includes an I^2C serial link with the color and sync signals.

2.2.5 Rear Access SATA Ports

- Two 3.0 Gb/s Gen 2 SATA ports at the backplane P2 connector. Pinouts of these ports match those of the ACC-0603 or ACC-0627 rear transition cards. These ports terminate at the QM57 Express Chipset.
- Two additional 3.0 Gb/s Gen 2 SATA ports at the backplane P0 connector. These ports target eSATA connectors on a new rear transition module.

2.2.6 Rear Access USB Ports

- Four USB ports are routed to the VME P2 connector to match the pinout of the ACC-0603 or ACC-0627 rear transition modules. These ports terminate at the QM57 Express Chipset.

2.2.7 Rear Access COM2 Ports

- The COM2 port (TTL signaling only) is provided at the backplane P2 connector, and is routed to match the ACC-0603 or ACC-0627 rear transition modules. The COM2 port terminates at a UART in the XVB601 FPGA.

2.2.8 VMEbus Backplane Interface

The VMEbus backplane controller is the Tundra Tsi148. This PCI-X to VME bridge provides a VMEbus interface, supporting bus transfer operations defined in the VITA 1-1994 and VITA 1.1-1997 and 2eSST bus cycles per VITA 1.5-2003.

2.2.9 PMC Site Front and Rear Ports

The XVB601 supports the options of either single or dual PMC sites. Front and rear port functions are defined by the mezzanine module provisioned in this site.

- On PMC site 1, sixty-four of the sixty-four mezzanine module rear I/O signals are connected to the XVB601 circuit board through the Pn4 connector at the PMC site and routed to the optional backplane P0 connector.
- On PMC site 2, forty-six of the sixty-four mezzanine module rear I/O signals are connected to the XVB601 circuit board through the Pn4 connector at the PMC site and routed to the backplane P2 connector on row d and z pins as defined in Section 2.4 of the VITA 35-2003 specification. The remaining eighteen rear I/O signal contacts on the Pn4 connector at the PMC site are not utilized on the XVB601 board.
- Front panel I/O PMC modules

2.2.10 Rear Access DVI Port

The QM57 Chipset DVI interface is routed to the VME P2 connector to be compatible with the ACC-0603 or ACC-0627 RTMs.

2.2.11 XDP Connectors

The XVB601 board supports XDP debug connectors as follows:

- XDP port connected to Core i7 Processor, compatible with American Arium emulator
- XDP port connected to QM57 Express Chipset, compatible with American Arium emulator

2.2.12 JTAG Connector

A JTAG boundary scan chain is provided on the XVB601 board, starting and ending at an internal connector defined by manufacturing and test engineering. This boundary scan chain connects to all devices with a compliant IEEE 1149.1-1990 Test Access Port, and includes the PMC site in the scan chain.

2.2.13 Power Entry and Distribution Definitions

The VMEbus backplane 5 V and +/-12 V power rails are accessed by the XVB601 following the functional requirements for VMEbus boards in VITA 1-1994. This circuit also controls the Power LED on the front panel of the assembly **(See Section 1.7.2 *LEDs* on page 38).** Live insertion as defined in VITA 1.4 is not supported on the XVB601.

- The 5 V rails are used for the XVB601 circuits and at the PMC site. The +12 V and -12 V rails are only used at the PMC site.
- VMEbus +5 V Standby power may be used as the input to a power circuit for Standby power generation instead of an onboard battery in extended or required applications.

Aggregate current load is expected to be 60 W maximum for the main XVB601 board, plus a maximum of 7.5 W for each of the PMC sites. Additional current loading may be supported at the PMC site, to the limit of the backplane and PMC site connector capacities.

2.3 PCI Device/Vendor IDs and Bus Number

The following table details the PCI Vendor/Device IDs as well as the bus number of the device without any PMC cards installed.

Table 2-1 PCI Device/Vendor IDs and Bus Number

Device	Component	Device ID	Vendor ID	BUS
DRAM Controller	Intel Core i7 CPU	0044	8086	00
Controller x8 PCI Express Root Port	Intel Core i7 CPU	0045	8086	00
Controller Graphics	Intel Core i7 CPU	0046	8086	00
Controller x8 PCI Express Root Port	Intel Core i7 CPU	0047	8086	00
USB EHCI Controller	Intel QM57 PCH	3B3C	8086	00
PCH x4 PCI Express Root Port	Intel QM57 PCH	3B42	8086	00
PCH x1 PCI Express Root Port	Intel QM57 PCH	3B4A	8086	00
PCH x1 PCI Express Root Port	Intel QM57 PCH	3B4C	8086	00
USB EHCI Controller	Intel QM57 PCH	3B34	8086	00
DMI to PCI Bridge	Intel QM57 PCH	2448	8086	00
PCI to LPC Bridge	Intel QM57 PCH	3B07	8086	00
SATA Controller	Intel QM57 PCH	3B2E	8086	00
SMBus Controller	Intel QM57 PCH	3B30	8086	00
SATA Controller	Intel QM57 PCH	3B2D	8086	00
PCI Express Switch	IDT PES16T4AG2	806C	111D	01
PCI Express to PCIX Bridge (PMC1)	Pericom PI7C9XC130	E130	12D8	03
PCI Express to PCIX Bridge (VME)	Pericom PI7C9XC130	E130	12D8	05
PCI-X to VME Bridge	IDT TSI148-133	0148	10E3	06
*PCI Express to PCIX Bridge (PMC2)	Pericom PI7C9XC130	E130	12D8	08
Ethernet Controller	Intel 82574	10D3	8086	0A
Ethernet Controller	Intel 82574	10D3	8086	0B
Watchdog, Timers, NVRAM FPGA	Altera EP3C	0008	114A	0C

*Bridge only present with 2 PMC board option.

2.4 SATA Ports

The SATA interface is provided by the Intel I/O Controller Hub (QM57 Express) chip. The SATA interface supports up to four channels. One SATA channel is routed to the optional CompactFlash socket. Two SATA channels are routed out the VME backplane and can be accessed using an ACC-0627, or ACC-0602RC/ ACC-0603RC RTM which terminate into standard SATA connectors.

2.5 Dual 10/100/1000 Ethernet via the Front Panel

The XVB601 supports Ethernet LANs with two Intel Ethernet controllers (a controller built into the QM57 Chipset and an 82574 controller). 10Base-T, 100Base-TX and GbE options are supported via two front panel RJ45 connectors.

10Base-T A network based on the 10Base-T standard uses unshielded twisted-pair cables, providing an economical solution to networking by allowing the use of existing telephone wiring and connectors. The RJ45 connector is used with the 10Base-T standard. 10Base-T has a maximum length of 100 meters.

100Base-TX The XVB601 also supports the 100Base-TX Ethernet. A network based on a 100Base-TX standard uses unshielded twisted-pair cables and an RJ45 connector. 100Base-TX has a maximum length of 100 meters.

1000Base-T The XVB601 supports GbE offering speeds of 1000Mb/s. It is fully compatible with existing Ethernets, since it uses the same CSMA/CD and MAC protocols. 1000Base-T has a maximum length of 3000 meters using Single-mode Fiber-Optic cables.

2.5.1 Boot ROM BIOS firmware

The XVB601 supports booting on the front panel GbE ports using a ROM Ethernet BIOS firmware. Refer to Section **3.5** ***Remote Ethernet Booting*** on page 85.

2.6 Video Graphics Adaptor

The XVB601 supports high-resolution graphics and multimedia-quality video using the Intel HD graphics controller. Screen resolutions up to 1,600 x 1,200 colors (single view mode) are supported by the graphics adapter.

NOTE

Under simultaneous heavy processor and graphics activity with the 1.07 GHz processor option, video quality may degrade slightly.

2.6.1 VGA Interface

The VGA interface can be accessed using an included adapter to adapt from the DVI-D front panel connector to a HD15 VGA connector. Supported display modes for VGA include:

Table 2-2 Partial List of Display Modes Supported for Analog

	Bits Per Pixel (Frequency) in Hz	
Resolution	16-bit	32-bit
640 x 480*		
800 x 600	60, 72, 75, 85, 100, 120	60, 72, 75, 85, 100, 120
1,024 x 768	60, 70, 75, 85, 100, 120	60, 70, 75, 85, 100, 120
1,152 x 864	60, 75, 85, 100	60, 75, 85, 100
1,280 x 600	60	60
1,280 x 720	60, 75, 85, 100	60, 75, 85, 100
1,280 x 768	60, 75, 85,	60, 75, 85
1,280 x 960	60, 75, 85	60, 75, 85
1,280 x 1,024	60, 75, 85, 100, 120	60, 75, 85, 100, 120
1,280 x 1,050	60, 75, 85	60, 75, 85
1,600 x 900	60, 75, 85, 100, 120	60, 75, 85, 100, 120
1,600 x 1,200	60, 75, 85, 100	60, 75, 85, 100

*The Intel Extreme Graphics driver 14.36.3.4990 does not load at 640x480 resolution as set by BIOS. Default color depth = 4 with no frequency options.

2.6.2 Digital Visual Interface (DVI-D)

The XVB601 supports a Digital Visual Interface that provides a high-speed digital connection for visual data types that are display technology independent. DVI-D is a display interface developed in response to the proliferation of digital flat-panel displays.

Table 2-3 Partial List of Display Modes Supported for Digital

	Bits Per Pixel (Frequency) in Hz	
Resolution	16-bit	32-bit
640 x 480*		
800 x 600	60	60
1024 x 768	60	60
1600 x 1200	60, 75, 85, 100	60, 75, 85, 100

*The Intel Extreme Graphics driver 14.36.3.4990 does not load at 640x480 resolution as set by BIOS. Default color depth = 4 with no frequency options.

NOTE

Under simultaneous heavy processor and graphics activity with the 1.07 GHz processor option, video quality may degrade slightly.

2.7 Universal Serial Bus

The XVB601 provides four Universal Serial Bus (USB) connections on the front panel and four USB interface ports out the VME P2 connector. The onboard USB controller supports the standard USB interface Rev. 2.0.

3 • Embedded PC/RTOS Features

GE's XVB601 features additional capabilities beyond those of a typical desktop computer system. The units provide four software-controlled, general-purpose timers along with a programmable Watchdog Timer for synchronizing and controlling multiple events in embedded applications. The XVB601 provides a bootable CompactFlash Disk system and 128 KByte of non-volatile RAM. Also, the XVB601 supports an embedded intelligent VME bridge to allow compatibility with the most demanding VME applications. These features make the unit ideal for embedded applications, particularly where standard hard drives and floppy disk drives cannot be used.

3.1 VME Bridge

In addition to its PC/AT functions, the XVB601 has the following VME features:

The VMEbus backplane controller is the Tundra Tsi148. This PCI-X to VME bridge provides a VMEbus interface, supporting bus transfer operations defined in the VITA 1-1994 and VITA 1.1-1997 and 2eSST bus cycles per VITA 1.5-2003. The Tundra Tsi148 allows VME to run at a bandwidth of up to 320 MByte/s (UM34) along the full length of a 21-slot backplane. This increases the performance in the following ways:

- 2eSST VME transfers
- 8x faster than the 40 MByte/s transfer rate of VME64
- 3x faster than a multi-domain, 64-bit/66 MHz CompactPCI bus
- Broadcast Mode support for sending data to multiple cards at one time

Other standard features include:

- Legacy protocol support
- User-configured interrupter
- User-configured interrupt handler
- Full VME system controller functionality
- Two programmable DMA controllers
- System Controller auto detection

The XVB601 VME interface is based on the high performance PCI-X-to-VME interface from the Tundra Tsi148. Providing a 64-bit bus width capable of operating at 100 MHz, the Tundra Tsi148 uses PCI-X version 2.0 mode 1. Tsi148 is fully compliant with both 2eSST and VME64 Extension standards (UMp30).

The functions and the programming of the Tsi148-based VME interface are addressed in detail in the *Tsi User Manual*.

3.1.1 PCI-X To VME Bridge (Tsi148) Software Guidelines

Programmers writing code or using GE computer Board Support Packages (BSPs) for the Tsi148 Bridge as used on the XVB601 single board computer, must be aware of requirements of the Tsi148-based PCI-X to VME architecture.

The XVB601 PCI-X to VME Interface uses the Tundra Tsi148 2eSST Bridge. This architecture interfaces the VME to the onboard SBC PCI-X bus. In doing so, the user must be aware of the following guidelines as related to Software programming of the Tsi148:

Shared XVB601 Memory: Any XVB601 DRAM memory made available to another VME master through the Tsi148 is subject to deadlock that may cause a VMEbus error unless specific precautions are taken. If onboard DRAM memory is slaved to the VME, and a program on the XVB601 with slaved memory attempts to write (from the processor) to the VME through the Tsi148, then the user must first request ownership of the VME through the Device Wants Bus (DWB) Bit in the Tsi148, and be granted the VME, prior to doing writes to the Tsi148.

NOTE

Please see the Tsi148 Manual and Errata regarding the requirements to use the DWB bit of the Tsi148.

The user may also implement other methods of gaining ownership of the VME, such as Tsi148 semaphores. But, regardless of the method used, when using shared memory, the user must gain exclusive VME ownership prior to generating asynchronous VME writes.

Extremely Long VME Slave Response Time: VME slave devices (or VME BERR conditions) that have a DTACK (or BERR) response time of greater than 16µ can cause Bridge Ordering rule issues with intermixed reads and writes through the Tsi148. If the SBC user wishes to do an extended number (larger than the depth of the Tsi148 write post buffer) of consecutive writes from the processor to the VME through the Tsi148, and those writes can be intermixed with reads from another task, then the user must verify that all slaves within the system have DTACK response time of less than 16µ, and that the VME BERR timer of the system is set to 16µ max. Also, it is suggested that prior to doing any large VME transfer, the users should first request ownership of the VME through the DWB Bit in the Tsi148, and be granted the VME, prior to doing writes to the Tsi148.

NOTE

Please see the Tsi148 Manual and Errata regarding the requirements to use the DWB bit of the Tsi148.

The user may also implement other methods of gaining ownership of the VME, such as Tsi148 semaphores. But, regardless of the method used, when generating an extended number of consecutive processor to VME writes (larger than the depth of the Tsi148 write post buffer), the user must gain exclusive VME ownership prior to generating these asynchronous VME writes.

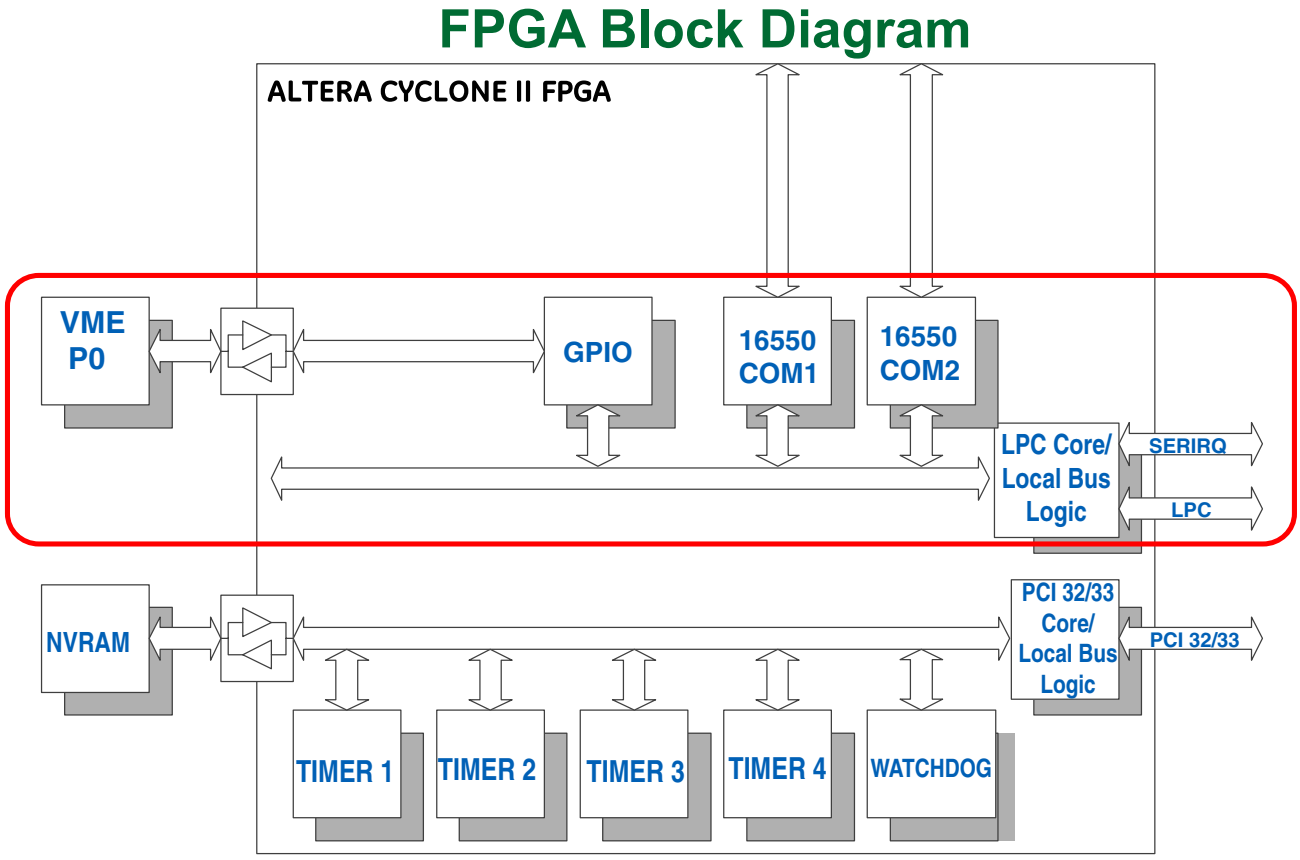
NOTE

Failure to implement the procedures outlined above may cause some system implementations to lockup or generate unwanted VME errors.

3.2 Embedded LPC Functions

The XVB601 FPGA provides a general purpose I/O port as well as two 16550 compatible UARTs via the LPC bus. The block diagram for the FPGA is shown in the figure below with the COM and GPIO functions circled in red.

Figure 3-1 FPGA Block Diagram: LPC Functions



3.2.1 FPGA LPC Access Port and General Configuration Registers

The FPGA contains three logical functions; the two UARTs and the 8-bit GPIO port. These functions are configured through a bank of registers that are indirectly accessed through a pair of I/O ports to set up the I/O address, interrupt line, and operating parameters. Each function has its own set of run-time registers that are accessed directly using I/O read and write cycles.

Configuration Access Port

Access to the configuration register file is indirect via a pair of I/O ports, the index port and the data port.

Table 3-1 Configuration Access Port

I/O Address	Name	Description
0x002E	Index	Configuration register index pointer.
0x002F	Data	Configuration data access.

After reset, all the configuration registers are locked and cannot be accessed. Configuration register access is enabled by writing an unlock code, 0x78, to the Index port address. Subsequently, configuration register access can be disabled again by writing a lock code, 0x87, to the Index port address. The lock and unlock codes do not match any internal index addresses.

Index Port

The Configuration Index register is an 8-bit read/write register used as a pointer into the configuration register file. It contains the index of the configuration register that is accessed through the data port.

Table 3-2 Configuration Index Register (I/O Address 0x002E)

Bit	Name	Access	Default	Description
7:0	INDEX	R/W	0x00	Pointer to configuration register index.

Data Port

The Configuration Data register is an 8-bit virtual register used for the data path to the configuration register pointed to by the Index register. Writes or reads to/from the Data port access the actual configuration register.

Table 3-3 Configuration Data Register (I/O Address 0x002F)

Bit	Name	Access	Default	Description
7:0	DATA	R/W	-	Data to/from indexed configuration register.

General Configuration Registers

Configuration register access uses a banked logical device method to facilitate standard plug-and-play software. Each functional block is assigned a separate logical device number. For the index range 0x00-0x2F, data port accesses map into the general device configuration registers. One of these registers is the logical device number register. For the index range 0x30-0xFF, data port accesses map into the configuration registers of the logical device pointed to by the logical device number register.

Table 3-4 General Configuration Registers

Index	Name	Description
0x07	Logical Device Number	Selects the current logical device.
0x20	Device ID	Identity number of the chip.
0x21	Version	Firmware version (major release) number.
0x22	Revision	Firmware revision (minor release) number.
0x23	-	Reserved.

Logical Device Number

This register selects the current logical device.

Table 3-5 Logical Device Number Register (Index 0x07)

Bit	Name	Access	Default	Description
7:0	LDN	R/W	0x00	Logical device number 0x04: UART 1 0x05: UART 2 0x07: GPIO Port

Device ID

The Device ID register provides a means to identify the chip to software.

Table 3-6 Device ID Register (Index 0x20)

Bit	Name	Access	Default	Description
7:0	ID	R	0x35	Device identification number.

Version

The Version register provides the major load number of the FPGA firmware.

Table 3-7 Firmware Version Register (Index 0x21)

Bit	Name	Access	Default	Description
7:0	VER	R	-	Firmware version (major release) number.

Revision

The Revision register provides the minor load number of the FPGA firmware.

Table 3-8 Firmware Revision Register (Index 0x22)

Bit	Name	Access	Default	Description
7:0	REV	R	-	Firmware revision (minor release) number.

3.2.2 GPIO Port

The GPIO_Port provides the basic functionality to access and control a set of general-purpose I/O pins. These functions include the following.

- Individually configurable I/O options. The configuration registers may be external to or integrated within the GPIO_Port module, based on a strapping option.
  - Direction - input or output.
  - Polarity - non-inverted or inverted.
  - Output type - totem-pole or open-drain.
  - Input interrupt type - level or edge.
  - Debounce - direct input or 15ms debounce filtered.
- GPIO line status. The input line, following the input polarity and debounce logic, is always readable whether the GPIO pin is configured as an input or an output.
- GPIO line drive. In totem-pole output mode the line can be actively driven both high and low. In open-drain mode it can be driven low or tri-stated, and an external pull-up resistor is required. The output state can be controlled directly via an output data register, or manipulated through set and clear registers. Data is inverted or not depending on the state of the polarity configuration register.
- Interrupt generation. Two separate interrupt outputs, intended for masked and non-masked applications, are provided. Each interrupt has its own set of local status and mask registers. The polarity of the interrupt mask may be set high or low based on a module strapping option. For non-NMI applications the corresponding logic and registers may be optimized out based on another module strapping option.

General-Purpose I/O

The XVB601 provides eight programmable general-purpose I/O (GPIO) pins on the backplane P0 connector. Each GPIO pin is highly flexible and can be independently configured as an input or output, non-inverting or inverting, totem-pole or open-drain driver, level or edge sensitive, and with or without debounce filtering. The eight GPIO port bits are assigned a common interrupt request line, and each individual GPIO pin can be configured to assert the assigned group IRQ or a non-maskable interrupt (NMI), or have interrupt generation disabled (masked).

Table 3-9 GPIO DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Notes
Input HIGH voltage	V_{IH}	2.0		+3.3 V	V	
Input LOW voltage	V_{IL}	-0.5		0.8	V	
Output HIGH voltage	V_{OH}	2.4			V	I_{OUT} = -8mA
Output LOW voltage	V_{OL}			0.4	V	I_{OUT} = 8mA

GPIO Register Descriptions

There are two sets of GPIO registers. One set is the configuration registers and the other set is the run-time registers.

NOTE

All GPIO registers are scaled to the port size of the module. The register descriptions below show all the bits for the 8-bit module. For the 8-bit module, bits [15:8] are not implemented.

NOTE

Register offsets are dependent on the width of the module and how the external address is connected. In the 8-bit module, addr[2:0] are used to decode the register offsets. The address offsets shown below are based on the actual address bits that are decoded within the module.

GPIO Configuration Registers

GPIO configuration registers are shown below. The address indicates the offset from the associated base address of the mode configuration register "0xF0". These registers are only present within the module when the local_cfg input is set to 1.

Table 3-10 GPIO Configuration Registers

Index	Name	Description
0x30	Control	Logical device activation control.
0x60	GPIO Base (High)	GPIO registers base I/O address (upper 8 bits).
0x61	GPIO Base (Low)	GPIO registers base I/O address (lower 8 bits).
0x70	GPIO IRQ	GPIO interrupt request assignment.
0xF0	GPIO Direction	GPIO input/output direction.
0xF1	GPIO Polarity	GPIO input/output polarity.
0xF2	GPIO Output Type	GPIO totem-pole/open-drain output type.
0xF3	GPIO Input Type	GPIO level/edge input type.
0xF5	GPIO Debounce	GPIO input debounce enable.

GPIO Control

The GPIO Control register allows the logical device to be activated or deactivated.

Table 3-11 GPIO Control Register (LDN 0x07, Index 0x30)

Bit	Name	Access	Default	Description
7:1	-	R	0b0000000	Reserved.
0	ACTIVATE	R/W	0	Logical device activation. 0: Disabled. 1: Enabled.

GPIO Base Address

The GPIO Base Address register sets the I/O base addresses for the GPIO registers. The base address must be aligned on an 8-byte boundary.

Table 3-12 GPIO Base Address Register (LDN 0x07, Index 0x60-0x61)

Bit	Name	Access	Default	Description
15:3	ADDR[15:3]	R/W	0x0000	Base address bits 15:3.
2:0	-	R	0b000	Reserved.

GPIO IRQ

The GPIO IRQ register sets the interrupt request line used by the GPIO port.

Table 3-13 GPIO IRQ Register (LDN 0x07, Index 0x70)

Bit	Name	Access	Default	Description
7:4	-	R	0b0000	Reserved.
3:0	IRQ	R/W	0b0000	Interrupt request line assignment. 0b0000: None. 0b0001: IRQ1. 0b0010: IRQ2. 0b0011: IRQ3. 0b0100: IRQ4. 0b0101: IRQ5. 0b0110: IRQ6. 0b0111: IRQ7. 0b1000: IRQ8. 0b1001: IRQ9. 0b1010: IRQ10. 0b1011: IRQ11. 0b1100: IRQ12. 0b1101: IRQ13. 0b1110: IRQ14. 0b1111: IRQ15.

GPIO Direction

The GPIO Direction register sets the individual direction for each bit of the GPIO port. Each bit can be independently configured as an input or an output.

Table 3-14 GPIO Direction Register (LDN 0x07, Index 0xF0)

Bit	Name	Access	Default	Description
7	DIR7	R/W	0	Bit 7 I/O direction. 0: Input. 1: Output.
6	DIR6	R/W	0	Bit 6 I/O direction.
5	DIR5	R/W	0	Bit 5 I/O direction.
4	DIR4	R/W	0	Bit 4 I/O direction.
3	DIR3	R/W	0	Bit 3 I/O direction.
2	DIR2	R/W	0	Bit 2 I/O direction.
1	DIR1	R/W	0	Bit 1 I/O direction.
0	DIR0	R/W	0	Bit 0 I/O direction.

GPIO Polarity

The GPIO Polarity register sets the individual polarity for each bit of the GPIO port. Each bit can be independently configured as non-inverting or inverting.

Table 3-15 GPIO Polarity Register (LDN 0x07, Index 0xF1)

Bit	Name	Access	Default	Description
7	POL7	R/W	0	Bit 7 polarity. 0: Noninverted. 1: Inverted.
6	POL6	R/W	0	Bit 6 polarity.
5	POL5	R/W	0	Bit 5 polarity.
4	POL4	R/W	0	Bit 4 polarity.
3	POL3	R/W	0	Bit 3 polarity.
2	POL2	R/W	0	Bit 2 polarity.
1	POL1	R/W	0	Bit 1 polarity.
0	POL0	R/W	0	Bit 0 polarity.

GPIO Output Type

The GPIO Output Type register sets the individual output driver type for each bit of the GPIO port. Each bit may be independently configured as totem-pole or open-drain.

Table 3-16 GPIO Output Type Register (LDN 0x07, Index 0xF2)

Bit	Name	Access	Default	Description
7	OTYPE7	R/W	0	Bit 7 output driver type. 0: Totem pole. 1: Open drain.
6	OTYPE6	R/W	0	Bit 6 output driver type.
5	OTYPE5	R/W	0	Bit 5 output driver type.
4	OTYPE4	R/W	0	Bit 4 output driver type.
3	OTYPE3	R/W	0	Bit 3 output driver type.
2	OTYPE2	R/W	0	Bit 2 output driver type.
1	OTYPE1	R/W	0	Bit 1 output driver type.
0	OTYPE0	R/W	0	Bit 0 output driver type.

GPIO Input Type

The GPIO Input Type register sets the individual input trigger type for each bit of the GPIO ports. Each bit may be independently configured as level or edge sensitive.

Table 3-17 GPIO Input Type Register (LDN 0x07, Index 0xF3)

Bit	Name	Access	Default	Description
7	ITYPE7	R/W	0	Bit 7 input trigger type. 0: Level. 1: Edge.
6	ITYPE6	R/W	0	Bit 6 input trigger type.
5	ITYPE5	R/W	0	Bit 5 input trigger type.
4	ITYPE4	R/W	0	Bit 4 input trigger type.
3	ITYPE3	R/W	0	Bit 3 input trigger type.
2	ITYPE2	R/W	0	Bit 2 input trigger type.
1	ITYPE1	R/W	0	Bit 1 input trigger type.
0	ITYPE0	R/W	0	Bit 0 input trigger type.

GPIO Debounce

The GPIO Input Debounce register sets the input debounce filter for each bit of the GPIO port. Each bit may be independently configured to bypass or enable a 16-msec digital filter.

Table 3-18 GPIO Debounce Register (LDN 0x07, Index 0xF5)

Bit	Name	Access	Default	Description
7	DBNC7	R/W	0	Bit 7 input debounce filter. 0: None. 1: Enabled - 16msec.
6	DBNC6	R/W	0	Bit 6 input debounce filter.
5	DBNC5	R/W	0	Bit 5 input debounce filter.
4	DBNC4	R/W	0	Bit 4 input debounce filter.
3	DBNC3	R/W	0	Bit 3 input debounce filter.
2	DBNC2	R/W	0	Bit 2 input debounce filter.
1	DBNC1	R/W	0	Bit 1 input debounce filter.
0	DBNC0	R/W	0	Bit 0 input debounce filter

GPIO Run-Time Registers

GPIO run-time registers are listed below. The address indicates the offset from the port base addresses programmed in the configuration registers.

Table 3-19 GPIO Run-Time Registers

Offset	Name	Description
0x0	Input Data	Input port data.
0x1	I/O Data	Input/output port data.
0x2	IRQ Event Status	Interrupt request event status.
0x3	Interrupt Enable	Input event interrupt enable.
0x4	NMI Event Status	Non-maskable interrupt event status.
0x5	NMI Enable	Input event non-maskable interrupt enable.
0x6	Clear Data	Output data bit clear.
0x7	Set Data	Output data bit set.

Input Data

The GPIO Input Data register shows the state, after any applicable logic inversion and/or debounce filtering, for each bit of the GPIO port.

Table 3-20 GPIO Input Data Register (Offset 0x0)

Bit	Name	Access	Default	Description
7	D7	R	-	Bit 7 input data.
6	D6	R	-	Bit 6 input data.
5	D5	R	-	Bit 5 input data.
4	D4	R	-	Bit 4 input data.
3	D3	R	-	Bit 3 input data.
2	D2	R	-	Bit 2 input data.
1	D1	R	-	Bit 1 input data.
0	D0	R	-	Bit 0 input data.

I/O Data

The GPIO I/O Data register provides the means to set the state for each output bit of the GPIO port. Reads from this register are aliased to the Input Data register and therefore show the state of the external port and not the data written to the internal register.

Table 3-21 GPIO Input/Output Data Register (Offset 0x1)

Bit	Name	Access	Default	Description
7	D7	R/W	-	Bit 7 input/output data.
6	D6	R/W	-	Bit 6 input/output data.
5	D5	R/W	-	Bit 5 input/output data.
4	D4	R/W	-	Bit 4 input/output data.
3	D3	R/W	-	Bit 3 input/output data.
2	D2	R/W	-	Bit 2 input/output data.
1	D1	R/W	-	Bit 1 input/output data.
0	D0	R/W	-	Bit 0 input/output data.

IRQ Event

The GPIO IRQ Event register shows the status of interrupt request events for each input bit of the GPIO port. An event is considered to be the asserted state for level-sensitive inputs, and an inactive-to-active transition for the edge-triggered inputs, based on the associated polarity bit setting. Interrupt events are captured in this register whether or not they are masked from generating external interrupts. Edge-triggered events are cleared by writing ones to the corresponding register bit positions. Level sensitive events must be cleared at the source.

Table 3-22 GPIO IRQ Event Register (Offset 0x2)

Bit	Name	Access	Default	Description
7	ISTAT7	R/C	0	Bit 7 IRQ event status.
6	ISTAT6	R/C	0	Bit 6 IRQ event status.
5	ISTAT5	R/C	0	Bit 5 IRQ event status.
4	ISTAT4	R/C	0	Bit 4 IRQ event status.
3	ISTAT3	R/C	0	Bit 3 IRQ event status.
2	ISTAT2	R/C	0	Bit 2 IRQ event status.
1	ISTAT1	R/C	0	Bit 1 IRQ event status.
0	ISTAT0	R/C	0	Bit 0 IRQ event status.

GPIO Interrupt Enable

The GPIO Interrupt Enable register provides the means to enable or mask interrupt events for each input bit of the GPIO port.

Table 3-23 GPIO IRQ Enable Register (Offset 0x3)

Bit	Name	Access	Default	Description
7	IEN7	R/W	0	Bit 7 interrupt enable. 0: Interrupt masked. 1: Interrupt enabled.
6	IEN6	R/W	0	Bit 6 interrupt enable.
5	IEN5	R/W	0	Bit 5 interrupt enable.
4	IEN4	R/W	0	Bit 4 interrupt enable.
3	IEN3	R/W	0	Bit 3 interrupt enable.
2	IEN2	R/W	0	Bit 2 interrupt enable.
1	IEN1	R/W	0	Bit 1 interrupt enable.
0	IEN0	R/W	0	Bit 0 interrupt enable.

NMI Event

The GPIO NMI Event register shows the status of non-maskable interrupt events for each input bit of the GPIO port. An event is considered to be the asserted state for level-sensitive inputs, and an inactive-to-active transition for the edge-triggered inputs, based on the associated polarity bit setting. Interrupt events are captured in this register whether or not they are masked from generating external interrupts. Edge-triggered events are cleared by writing ones to the corresponding register bit positions. Level sensitive events must be cleared at the source.

Table 3-24 GPIO NMI Event Register (Offset 0x4)

Bit	Name	Access	Default	Description
7	NSTAT7	R/C	0	Bit 7 NMI event status.
6	NSTAT6	R/C	0	Bit 6 NMI event status.
5	NSTAT5	R/C	0	Bit 5 NMI event status.
4	NSTAT4	R/C	0	Bit 4 NMI event status.
3	NSTAT3	R/C	0	Bit 3 NMI event status.
2	NSTAT2	R/C	0	Bit 2 NMI event status.
1	NSTAT1	R/C	0	Bit 1 NMI event status.
0	NSTAT0	R/C	0	Bit 0 NMI event status.

NMI Enable

The GPIO NMI Enable register provides the means to enable or mask interrupt events for each input bit of the GPIO port.

Table 3-25 GPIO NMI Enable Register (Offset 0x5)

Bit	Name	Access	Default	Description
7	NEN7	R/W	0	Bit 7 interrupt enable. 0: Interrupt masked. 1: Interrupt enabled.
6	NEN6	R/W	0	Bit 6 interrupt enable.
5	NEN5	R/W	0	Bit 5 interrupt enable.
4	NEN4	R/W	0	Bit 4 interrupt enable.
3	NEN3	R/W	0	Bit 3 interrupt enable.
2	NEN2	R/W	0	Bit 2 interrupt enable.
1	NEN1	R/W	0	Bit 1 interrupt enable.
0	NEN0	R/W	0	Bit 0 interrupt enable.

Clear Data

The GPIO Clear Data register is a virtual register that provides the means to clear individual output bits without impacting the state of the remaining output bits.

Table 3-26 GPIO Clear Data Register (Offset 0x6)

Bit	Name	Access	Default	Description
7	CLR7	W	0	Bit 7 clear data. 0: No effect. 1: Output data bit is cleared to 0.
6	CLR6	W	0	Bit 6 clear data.
5	CLR5	W	0	Bit 5 clear data.
4	CLR4	W	0	Bit 4 clear data.
3	CLR3	W	0	Bit 3 clear data.
2	CLR2	W	0	Bit 2 clear data.
1	CLR1	W	0	Bit 1 clear data.
0	CLR0	W	0	Bit 0 clear data.

Set Data

The GPIO Set Data register is a virtual register that provides the means to set individual output bits without impacting the state of the remaining output bits.

Table 3-27 GPIO Set Data Register (Offset 0x7)

Bit	Name	Access	Default	Description
7	SET7	W	0	Bit 7 set data. 0: No effect. 1: Output data bit is set to 1.
6	SET6	W	0	Bit 6 set data.
5	SET5	W	0	Bit 5 set data.
4	SET4	W	0	Bit 4 set data.
3	SET3	W	0	Bit 3 set data.
2	SET2	W	0	Bit 2 set data.
1	SET1	W	0	Bit 1 set data.
0	SET0	W	0	Bit 0 set data.

3.2.3 UART Ports

The XVB601 FPGA provides a pair of 16550 compatible UARTs on the LPC bus at logical device numbers 0x04 and 0x05 similar to a standard Super I/O. There are two sets of registers for each UART. One set is the configuration registers and the other set is the run-time registers. The register layout is the same for both UARTs.

UART Port Configuration Registers

Table 3-28 UART Port Configuration Registers

Index	Name	Description
0x30	Control	Logical device activation control.
0x60	UART Base (High)	UART registers base I/O address (upper 8 bits).
0x61	UART Base (Low)	UART registers base I/O address (lower 8 bits).
0x70	UART IRQ	UART interrupt request assignment.
0x74	UART DMA Channel 0	UART DMA channel select 0.
0x75	UART DMA Channel 1	UART DMA channel select 1.
0xF0	UART Mode 0	UART extended mode settings.
0xF1	UART Mode 1	Additional UART extended mode settings.

UART Control

The UART Control register allows the logical device to be activated or deactivated.

Table 3-29 UART Control Register (LDN 0x02, Index 0x30)

Bit	Name	Access	Default	Description
7:1	-	R	0b0000000	Reserved.
0	ACTIVATE	R/W	0	Logical device activation 0: Disabled 1: Enabled.

UART Base Address

The UART Base Address register sets the I/O base address for the UART registers. The base address must be aligned on an 8-byte boundary and lie within the range 0x0100-0x03F8.

Table 3-30 UART Base Address Register (LDN 0x02, Index 0x60-0x61)

Bit	Name	Access	Default	Description
15:10	-	R	0b000000	Reserved.
9:3	ADDR[9:3]	R/W	0b0000000	Base address bits 9:3.
2:0	-	R	0b000	Reserved.

UART IRQ

The UART IRQ register sets the interrupt request line used by the UART port.

Table 3-31 UART IRQ Register (LDN 0x02, Index 0x70)

Bit	Name	Access	Default	Description
7:4	-	R	0b0000	Reserved.
3:0	IRQ	R/W	0b0000	Interrupt request line assignment 0b0000: None 0b0001: IRQ1 0b0010: IRQ2 0b0011: IRQ3 0b0100: IRQ4 0b0101: IRQ5 0b0110: IRQ6 0b0111: IRQ7 0b1000: IRQ8 0b1001: IRQ9 0b1010: IRQ10 0b1011: IRQ11 0b1100: IRQ12 0b1101: IRQ13 0b1110: IRQ14 0b1111: IRQ15

UART DMA Channels

Two DMA channels can be provisioned for the UART port. Channel 0 is used for transmit operations (DMA reads from memory to the transmit FIFO), and channel 1 is used for receive operations (DMA writes from the receive FIFO to memory). The UART supports 8-bit DMA transfers only, therefore only DMA channels 0-3 are valid. A value of 4-7 indicates that no DMA channel is active.

Table 3-32 UART DMA Channel Select Register (LDN 0x02, Index 0x74/0x75)

Bit	Name	Access	Default	Description
7:3	-	R	0b00000	Reserved
2:0	CHAN	R/W	0x4	Reserved

UART Mode

The UART Mode registers set the extended configuration parameters for the UART port.

Table 3-33 UART Mode Register 0 (LDN 0x02, Index 0xF0)

Bit	Name	Access	Default	Description
7	PRE_DIV_DIS	R/W	0	Baud-rate pre-divider disable. When set to 1 the by-8 pre-divider for the baud-rate generator is disabled. This bit should be cleared to 0 for standard 16550 operation.
6	DMA_EN	R/W	0	DMA enable. When set to 1 DMA functionality is enabled for the UART. This bit should be cleared to 0 for standard 16550 operation.
5	TEST_FE	R/W	0	Framing error test mode. When set to 1 the transmitted stop bit is truncated to ½ bit times in asynchronous mode, and is omitted altogether in synchronous mode. This bit must be cleared to 0 for normal operation.
4	TEST_PE	R/W	0	Parity error test mode. When set to 1 the transmitted parity bit is inverted. This bit must be cleared to 0 for normal operation.
3:2	FIFO_SIZE	R/W	0b00	Selects the size of the transmit and receive data FIFOs. 0b00: 16 bytes. 0b01: 64 bytes. 0b10: 256 bytes. 0b11: 1024 bytes.
1	TXCLK_SRC	R/W	0	Transmit clock source. 0: Internal baud-rate generator. 1: Receive clock.
0	SYNC	R/W	0	When 0 the UART will operate in standard asynchronous mode. When 1 the UART will operate in external clock synchronous mode.

Table 3-34 UART Mode Register 1 (LDN 0x02, Index 0xF1)

Bit	Name	Access	Default	Description
7:5	-	R	0b000	Reserved.
4	AUTO DIR	R/W	0	Automatic RS485 half-duplex direction control. 0: Tx/Rx direction controlled by RTS. 1: Tx/Rx direction controlled automatically.
3	HALF_DUPLEX	R/W	0	RS485 half/full-duplex control. 0: Full duplex. 1: Half duplex.
2	-	R	0b000	Reserved.
1	RS485	R/W	0	RS485/RS422 mode. 0: RS422. 1: RS485.
0	CLK_SEL	R/W	0	UART input reference clock select. 0: 14.7456 MHz. 1: 48.0 MHz.

UART Port Run-Time Registers

UART run-time registers are listed below. The address indicates the offset from the port base addresses programmed in the configuration registers.

Table 3-35 UART Run-Time Registers

Offset	DLAB	Name	Description
0x0	0	Receive Buffer Transmit Buffer	Receive data buffer (read). Transmit data buffer (write).
0x1	0	Interrupt Enable	Interrupt event enable/mask.
0x2	X	Interrupt Identification FIFO Control	Interrupt event status (read). FIFO control settings (write).
0x3	X	Line Control	Line control settings.
0x4	X	Modem Control	Modem control settings.
0x5	X	Line Status	Line status indications.
0x6	X	Modem Status	Modem status indications.
0x7	X	Scratchpad	Scratchpad data.
0x0	1	Divisor Latch (LSB)	Least-significant byte of baud-rate divisor.
0x1	1	Divisor Latch (MSB)	Most-significant byte of baud-rate divisor.

Receive Buffer

This register holds the incoming receive data after it has been transferred from the incoming shift register. In FIFO mode this register contains receive data byte pulled from the top of the memory buffer.

Table 3-36 UART Receive Buffer Register (Offset 0x0, DLAB=0)

Bit	Name	Access	Default	Description
7:0	RXDATA	R	0x00	Receive buffer data.

Transmit Buffer

This register contains the data to be transmitted out. Its contents are automatically transferred to the outgoing shift register after the previous byte has been shifted out. In FIFO mode, writes to this register are pushed into the bottom of the memory buffer.

Table 3-37 UART Transmit Buffer Register (Offset 0x0, DLAB=0)

Bit	Name	Access	Default	Description
7:0	TXDATA	W	N/A	Transmit buffer data.

Interrupt Enable

This register provides the means to enable or mask individual causes from generating an external UART interrupt. When set to 0 the interrupt cause is masked, and when set to 1 the interrupt cause is enabled. Access to the DMA interrupt and transfer enable bits is allowed only when DMA is enabled in the UART mode configuration register. Otherwise these bits are read-only and forced to zero.

Table 3-38 UART Interrupt Enable Register (Offset 0x1)

Bit	Name	Access	Default	Description
7	TX_XFR	R/W	0	Transmit DMA transfer enable. Automatically cleared when the transfer is complete (as indicated by the terminal count).
6	RX_XFR	R/W	0	Receive DMA transfer enable. Automatically cleared when the transfer is complete (as indicated by the terminal count).
5	TX_DMA	R/W	0	Transmit DMA transfer complete interrupt enable.
4	RX_DMA	R/W	0	Receive DMA transfer complete interrupt enable.
3	MODEM	R/W	0	Modem status interrupt enable.
2	LINE	R/W	0	Received line status interrupt enable.
1	TX	R/W	0	Transmit holding register empty interrupt enable.
0	RX	R/W	0	Received data available interrupt enable.

Interrupt Identification

This register provides the status and source of the highest-priority pending UART interrupt.

Table 3-39 UART Interrupt Identification Register (Offset 0x2)

Bit	Name	Access	Default	Description
7:6	FIFO	R	0b00	Set to 0b11 when FIFO mode is enabled.
5	TX_DMA	R	0	Transmit DMA transfer complete. The interrupt ID will be 0b001.
4	RX_DMA	R	0	Receive DMA transfer complete. The interrupt ID will be 0b010.
3:1	ID	R	0b000	Highest priority interrupt identification. 0b011 (1st): receiver line status. 0b010 (2nd): receiver data available. 0b110 (2nd): timeout indication (FIFO mode only). 0b001 (3rd): transmit holding register empty. 0b000 (4th): modem status.
0	NPEND	R	1	When 0 indicates that an interrupt is pending.

The various UART interrupt indications are cleared in different manners, depending upon the source of the interrupt. A receiver line status interrupt is cleared by reading the Line Status register. The receiver data available interrupt is cleared by reading the Receive Buffer register, or when the FIFO falls below the trigger level. The timeout interrupt is cleared by reading from the FIFO. A transmit holding register empty interrupt is cleared either by reading the Interrupt Identification Register (when it is the source of the interrupt) or by writing to the Transmit Data register. A modem status interrupt is cleared by reading the Modem Status register. Receive and transmit DMA interrupts are cleared by reading the Interrupt Identification Register when they are the source of the interrupt.

FIFO Control

This register is used to enable and clear the transmit and receive data FIFOs, and to set the trigger levels.

Table 3-40 UART FIFO Control Register (Offset 0x2)

Bit	Name	Access	Default	Description
7:6	RX_TRIG	W	0b00	Receive FIFO interrupt trigger level. 16-byte FIFO 0b00: 1 byte. 0b01: 4 bytes. 0b10: 8 bytes. 0b11: 14 bytes. 64-byte FIFO 0b00: 1 byte. 0b01: 16 byte 0b10: 32 bytes. 0b11: 56 bytes. 256-byte FIFO 0b00: 1 byte 0b01: 32 bytes 0b10: 64 bytes. 0b11: 128 bytes. 1024-byte FIFO 0b00: 1 byte. 0b01: 64 bytes. 0b10: 128 bytes. 0b11: 256 bytes.
5:4	TX_TRIG	W	0b00	Transmit FIFO trigger level. 16-byte FIFO 0bXX: 1 byte. 64-byte FIFO 0b00: 1 byte. 0b01: 16 bytes. 0b10: 56 bytes. 0b11: 64 bytes. 256-byte FIFO 0b00: 1 byte. 0b01: 64 bytes. 0b10: 224 bytes. 0b11: 256 bytes. 1024-byte FIFO 0b00: 1 byte. 0b01: 256 bytes. 0b10: 896 bytes. 0b11: 1024 bytes.
3	DMA_MODE	W	0	DMA mode select.
2	TX_CLR	W	0	Writing a 1 clears the transmit FIFO. This bit is self-clearing.
1	RX_CLR	W	0	Writing a 1 clears the receiver FIFO. This bit is self-clearing.
0	EN	W	0	FIFO enable.

UART transmit and receive DMA requests operate in either single-byte or block mode:

Single-byte (mode 0) is selected when the FIFOs are not enabled or the DMA_MODE bit is 0. A transmit DMA request is issued when the TX_XFR bit is set and the transmit holding register is empty or the transmit FIFO is below the trigger level. A receive DMA request is issued when the RX_XFR bit is set and there is at least one character in the receive buffer register of FIFO.

Block (mode 1) is selected when the FIFOs are enabled and the DMA_MODE bit is 1. In this case a transmit DMA request is issued when the TX_XFR bit is set and the transmit FIFO is below the trigger level. The request remains active until the transfer completes or the transmit FIFO becomes full. A receive DMA request is issued when the receive FIFO reaches the trigger level. The request remains active until the transfer completes or the receive FIFO becomes empty.

Line Control

This register specifies the format of the asynchronous or bit-synchronous data communication used. It also provides access to the baud-rate divisor registers.

Table 3-41 UART Line Control Register (Offset 0x3)

Bit	Name	Access	Default	Description
7	DLAB	R/W	0	Divisor latch access bit. 0: Normal registers are accessed at 0x0 and 0x1 offset. 1: Divisor latch registers are accessed.
6	BREAK	R/W	0	Break control. 0: Break is disabled. 1: Serial data out is forced to 0.
5	STICK_PAR	R/W	0	Stick parity. 0: Stick parity function disabled. 1: Parity is transmitted and checked as a 0 for odd parity, and as a 1 for even parity.
4	EVEN_PAR	R/W	0	Even parity select. 0: Odd number of 1s in data + parity. 1: Even number of 1s in data + parity.
3	PAR_EN	R/W	0	Parity enable. 0: No parity. 1: Parity bit is generated and appended to each outgoing character, and is checked on each incoming character.
2	STOP	R/W	0	Sets the number of generated stop bits 0: 1 stop bit. 1: 1½ stop bits for 5-bit character; 2 stop bits otherwise.
1:0	LENGTH	R/W	0b00	Selects the number of bits in each character. 0b00: 5 bits. 0b01: 6 bits. 0b10: 7 bits 0b11: 8 bits.

Modem Control

This register controls the UART interface to a modem.

Table 3-42 UART Modem Control Register (Offset 0x4)

Bit	Name	Access	Default	Description
7:5	-	R	0b000	Reserved.
4	LOOPBACK	R/W	0	Loopback mode. 0: Normal operation. 1: Loopback operation. In this mode the serial transmit output is set to 1, the transmit shift register is internally connected to the receive shift register, DTR is connected to DSR, RTS is connected to CTS, OUT1 is connected to RI, and OUT2 is connected to DCD.
3	OUT2	R/W	0	Output 2. In loopback mode, connected to Data Carrier Detect input.
2	OUT1	R/W	0	Output 1. In loopback mode, connected to Ring Indicator input.
1	RTS	R/W	0	External Request To Send signal control. 0: RTS is set to 1. 1: RTS is set to 0.
0	DTR	R/W	0	External Data Terminal Ready signal control. 0: DTR is set to 1. 1: DTR is set to 0.

Line Status

This register provides access to status indicators on the UART line interface.

Table 3-43 UART Line Status Register (Offset 0x5)

Bit	Name	Access	Default	Description
7	ERR_INF	R	0	Error in FIFO. Always cleared in register mode. In FIFO mode this bit indicates that at least one parity error, framing error, or break indication has been received and is inside the receive FIFO. Cleared on read if no more errors reside in the FIFO.
6	TEMPT	R	1	Transmitter empty. Set to 1 whenever both the transmit holding register and the transmit shift register are empty. In FIFO mode this bit indicates that both the transmit FIFO and the transmit shift register are empty.
5	THRE	R	1	Transmit holding register empty. Set to 1 to indicate that the transmit holding register is ready to accept a new character. In FIFO mode this bit indicates that the entire transmit FIFO is empty.
4	BI	R	0	Break indicator. Set to 1 whenever the receive data is held at logic 0 for at least one full character (start bit + data + parity + stop bit) time. In FIFO mode this applies to the character at the top of the FIFO. Generates a Receiver Line Status interrupt. Cleared when read.
3	FE	R	0	Framing error. Set to 1 when the received character does not have a valid stop bit. In FIFO mode this applies to the character at the top of the FIFO. Generates a Receiver Line Status interrupt. Cleared when read.
2	PE	R	0	Parity error. Set to 1 when the received character has incorrect parity. In FIFO mode this applies to the character at the top of the FIFO. Generates a Receiver Line Status interrupt. Cleared when read.
1	OE	R	0	Overrun error. Set to 1 when a new receive character is transferred to the transmit holding register before the prior character was read, or that the FIFO is full and a complete new character is received in the shift register. Generates a Receiver Line Status interrupt. Cleared when read.
0	DR	R	0	Data ready. Set to 1 whenever a complete incoming character has been received and transferred to the receive data buffer or receive FIFO. Cleared on a read from the receive buffer register, or when the FIFO is empty.

Modem Status

This register provides access to status indicators on the UART modem interface.

Table 3-44 UART Modem Status Register (Offset 0x6)

Bit	Name	Access	Default	Description
7	DCD	R	0	Complement of external DCD input. Equals OUT2 in loopback mode.
6	RI	R	0	Complement of external RI input. Equals OUT1 in loopback mode.
5	DSR	R	0	Complement of external DSR input. Equals DTR in loopback mode.
4	CTS	R	0	Complement of external CTS input. Equals RTS in loopback mode.
3	DDCD	R	0	Delta data carrier detect. Indicates that the DCD line has changed state.
2	TERI	R	0	Trailing edge of ring indicator. Indicates that the RI line has changed state from low to high.
1	DDSR	R	0	Delta data set ready. Indicates that the DSR line has changed state.
0	DCTS	R	0	Delta clear to send. Indicates that the CTS line has changed state.

Scratchpad

This register is an 8-bit read/write register for scratchpad data or test purposes. Writes have no impact on the operation of the UART. When the UART is configured for extended FIFO size (FIFO_SIZE ≠ 0b00) and FIFO mode is enabled, this register provides a secondary function - it indicates the actual number of bytes in the receive FIFO when a timeout interrupt is generated.

Table 3-45 UART Scratchpad Register (Offset 0x7)

Bit	Name	Access	Default	Description
7:0	SCRATCH	R/W	0x00	Scratchpad data / number of bytes in receive FIFO.

Divisor Latch

The UART contains a programmable baud-rate generator to divide the reference clock down to the serial data rate. The divisor is a 16-bit value contained in two byte-wide registers, one for the MSB and one for the LSB. For asynchronous mode the clock is set to 16× the bit rate, while for synchronous mode the clock is set to 1× the bit rate.

Table 3-46 UART Divisor (LSB) Register (Offset 0x0, DLAB=1)

Bit	Name	Access	Default	Description
7:0	DIV[7:0]	R/W	0x00	LSB of baud-rate generator divisor.

Table 3-47 UART Divisor (MSB) Register (Offset 0x1, DLAB=1)

Bit	Name	Access	Default	Description
7:0	DIV[15:8]	R/W	0x00	MSB of baud-rate generator divisor.

The following table shows the divisor values for some common serial data rates.

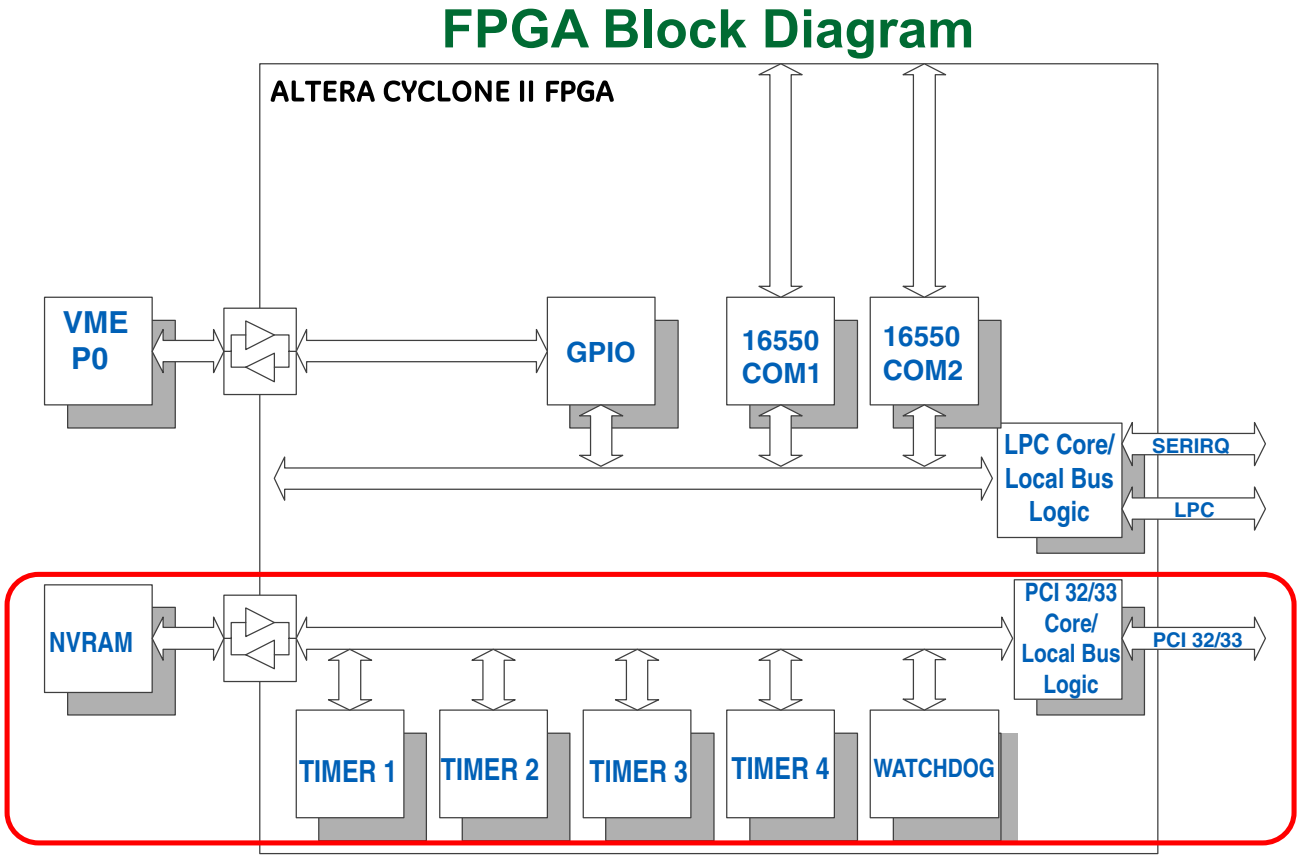
Table 3-48 Baud-Rate Divisor Settings

Baud Rate	Sync Mode	Clock Select	Pre-Divide Disable	Divisor
300	0	0	0	384
1200	0	0	0	96
2400	0	0	0	48
9600	0	0	0	12
19200	0	0	0	6
38400	0	0	0	3
57600	0	0	0	2
115.2k	0	0	0	1
230.4k	0	0	1	4
460.8k	0	0	1	2
500k	0	1	1	6
1.0M	0	1	1	3
2.0M	1	1	1	24

3.3 Embedded PCI Functions

The XVB601 provides non-volatile RAM (NVRAM), Timers and a Watchdog Timer via the PCI bus. These functions are required for embedded and real time applications. The block diagram for the FPGA is shown in the figure below with the Timers, Watchdog and NVRAM functions circled in red.

Figure 3-2 FPGA Block Diagram: PCI Functions



The PCI configuration space of these embedded functions is shown below.

Table 3-49 PCI Configuration Space Registers

31	16	15	00	Register Address
Device ID 0008		Vendor ID 114A		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
PCI Base Address 0 for Memory-Mapped 128 KB NVRAM (BAR0)				10h
PCI Base Address 1 for Memory-Mapped Watchdog and other timers (BAR1)				14h
Reserved				18h
Reserved				1Ch
Reserved				20h
Reserved				24h
Reserved				28h
Subsystem ID 7815		Subsystem Vendor ID 114A		2Ch
Reserved				30h
Reserved				34h
Reserved				38h
Max_Lat	Min_gnt	Interrupt Pin	Interrupt Line	3Ch

The “Device ID” field indicates that the device is for VME products (00) and indicates the supported embedded feature set.

The “Vendor ID” and “Subsystem Vendor ID” fields indicate GE’s PICMG® assigned Vendor ID (114A).

The “Subsystem ID” field indicates the model number of the product (7815).

NOTE

XVB601 boards with the 3 GByte memory option will begin to lose access to the physical memory if more than 128 KByte is chosen for VME.

3.3.1 NVRAM

The XVB601 provides 128 KByte of non-volatile RAM. This memory is mapped in 32K of address space starting at the address in BAR0. This memory is available at any time and supports byte, short word and long word accesses from the PCI bus. The contents of this memory are retained when the power to the board is removed.

3.3.2 Timers

General

The XVB601 provides four user-programmable timers (two 16-bit and two 32-bit) which are completely dedicated to user applications and are not required for any standard system function. Each timer is clocked by independent generators with selectable rates of 2 MHz, 1 MHz, 500 kHz and 250 kHz. Each timer may be independently enabled and each is capable of generating a system interrupt on timeout.

Events can be timed by either polling the timers or enabling the interrupt capability of the timer. A status register allows for application software to determine which timer is the cause of any interrupt.

Timer Control Status Register 1 (TCSR1)

The timers are controlled and monitored via the Timer Control Status Register 1 (TCSR1) located at offset 0x00 from the address in BAR2. The mapping of the bits in this register are as follows:

Table 3-50 Timer Control Register 1 (TCSR 1)

Field	Bits	Read or Write
Timer 1 Caused IRQ	TCSR1[0]	R/W
Timer 1 Enable	TCSR1[1]	R/W
Timer 1 IRQ Enable	TCSR1[2]	R/W
Timer 1 Clock Select	TCSR1[4..3]	R/W
Timer 2 Caused IRQ	TCSR1[8]	R/W
Timer 2 Enable	TCSR1[9]	R/W
Timer 2 IRQ Enable	TCSR1[10]	R/W
Timer 2 Clock Select	TCSR1[12..11]	R/W
Timer 3 Caused IRQ	TCSR1[16]	R/W
Timer 3 Enable	TCSR1[17]	R/W
Timer 3 IRQ Enable	TCSR1[18]	R/W
Timer 3 Clock Select	TCSR1[20..19]	R/W
Timer 4 Caused IRQ	TCSR1[24]	R/W
Timer 4 Enable	TCSR1[25]	R/W
Timer 4 IRQ Enable	TCSR1[26]	R/W
Timer 4 Clock Select	TCSR1[28..27]	R/W
Reserved	All Other Bits	R/W
All of these bits default to "0" after system reset.		

Each timer has an independently selectable clock source which is selected by the bit pattern in the "Timer x Clock Select" field as follows:

Table 3-51 Timer x Clock Select Field

Clock Rate	MSb	LSb
2 MHz	0	0
1 MHz	0	1
500 kHz	1	0
250 kHz	1	1

Each timer can be independently enabled by writing a “1” to the appropriate “Timer x Enable” field. Similarly, the generation of interrupts by each timer can be independently enabled by writing a “1” to the appropriate “Timer x IRQ Enable” field.

If an interrupt is generated by a timer, the source of the interrupt may be determined by reading the “Timer x Caused IRQ” fields. If the field is set to “1,” then the respective timer caused the interrupt. Note that multiple timers can cause a single interrupt. Therefore, the status of all timers must be read to ensure that all interrupt sources are recognized.

A particular timer interrupt can be cleared by writing a “0” to the appropriate “Timer x Caused IRQ” field. Alternately, a write to the appropriate Timer x IRQ Clear (TxIC) register will also clear the interrupt. When clearing the interrupt using the “Timer x Caused IRQ” fields, note that it is very important to ensure that a proper bit mask is used so that other register settings are not affected. The preferred method for clearing interrupts is to use the “Timer x IRQ Clear” registers described on page 82.

Timer Control Status Register 2 (TCSR2)

The timers are also controlled by bits in the Timer Control Status Register 2 (TCSR2) located at offset 0x04 from the address in BAR2. The mapping of the bits in this register are as follows:

Table 3-52 Timer Control Status Register 2 (TCSR2)

Field	Bits	Read or Write
Read Latch Select	TCSR2[0]	Read/Write
Reserved	All Other Bits	Read/Write
All of these bits default to “0” after system reset.		

The “Read Latch Select” bit is used to select the latching mode of the programmable timers. If this bit is set to “0,” then each timer output is latched upon a read of any one of its addresses. For example, a read to the TMRCCR12 register latches the count of timers 1 and 2. A read to the TMRCCR3 register latches the count of timer 3. This continues for every read to any one of these registers. As a result, it is not possible to capture the values of all four timers at a given instance in time. However, by setting this bit to “1”, all four timer outputs will be latched only on reads to the Timer 1 & 2 Current Count Register (TMRCCR12). Therefore, to capture the current count of all four timers at the same time, perform a read to the TMRCCR12 first (with a 32-bit read), followed by a read to TMRCCR3 and TMRCCR4. The first read (to the TMRCCR12 register) causes all four timer values to be latched at the same time. The subsequent reads to the TMRCCR3 and TMRCCR4 registers do not latch new count values, allowing the count of all timers at the same instance in time to be obtained.

Timer 1 and 2 Load Count Register (TMRLCR12)

Timers 1 & 2 are 16-bits wide and obtain their load count from the Timer 1 & 2 Load Count Register (TMRLCR12), located at offset 0x10 from the address in BAR2. The mapping of bits in this register are as follows:

Table 3-53 Timer 1 & 2 Load Count Register (TMRLCR12)

Field	Bits	Read or Write
Timer 2 Load Count	TMRLCR12[31..16]	Read/Write
Timer 1 Load Count	TMRLCR12[15..0]	Read/Write

When either of these fields are written (either by a single 32-bit write or separate 16-bit writes), the respective timer is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

Timer 3 Load Count Register (TMRLCR3)

Timer 3 is 32-bits wide and obtains its load count from the Timer 3 Load Count Register (TMRLCR3), located at offset 0x14 from the address in BAR2. The mapping of bits in this register are as follows:

Table 3-54 Timer 3 Load Count Register (TMRLCR3)

Field	Bits	Read or Write
Timer 3 Load Count	TMRLCR3[31..0]	Read/Write

When this field is written, Timer 3 is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

Timer 4 Load Count Register (TMRLCR4)

Timer 4 is 32-bits wide and obtains its load count from the Timer 4 Load Count Register (TMRLCR4), located at offset 0x18 from the address in BAR2. The mapping of bits in this register are as follows:

Table 3-55 Timer 4 Load Count Register (TMRLCR4)

Field	Bits	Read or Write
Timer 4 Load Count	TMRLCR4[31..0]	Read/Write

When this field is written, Timer 4 is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

Timer 1 and 2 Current Count Register (TMRCCR12)

The current count of timers 1 & 2 may be read via the Timer 1 & 2 Current Count Register (TMRCCR12), located at offset 0x20 from the address in BAR2. The mapping of bits in this register are as follows:

Table 3-56 Timer 1 & 2 Current Count Register (TMRCCR12)

Field	Bits	Read or Write
Timer 2 Count	TMRCCR12[31..16]	Read Only
Timer 1 Count	TMRCCR12[15..0]	Read Only

When either field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the "Read Latch Select" bit in the WDT Control Status Register (CSR2). See the CSR2 register description for more information on these two modes.

Timer 3 Current Count Register (TMRCCR3)

The current count of Timer 3 may be read via the Timer 3 Current Count Register (TMRCCR3), located at offset 0x24 from the address in BAR2. The mapping of bits in this register are as follows:

Table 3-57 Timer 3 Current Count Register (TMRCCR3)

Field	Bits	Read or Write
Timer 3 Count	TMRCCR3[31..0]	Read Only

When this field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the "Read Latch Select" bit in the WDT Control Status Register (CSR2). See the CSR2 register description for more information on these two modes.

Timer 4 Current Count Register (TMRCCR4)

The current count of Timer 4 may be read via the Timer 4 Current Count Register (TMRCCR4), located at offset 0x28 from the address in BAR2. The mapping of bits in this register are as follows:

Table 3-58 Timer 4 Current Count Register (TMRCCR4)

Field	Bits	Read or Write
Timer 4 Count	TMRCCR4[31..0]	Read Only

When this field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the "Read Latch Select" bit in the WDT Control Status Register (CSR2). See the CSR2 register description for more information on these two modes.

Timer 1 IRQ Clear (T1IC)

The Timer 1 IRQ Clear (T1IC) register is used to clear an interrupt caused by Timer 1. Writing to this register, located at offset 0x30 from the address in BAR2, causes the interrupt from Timer 1 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

Timer 2 IRQ Clear (T2IC)

The Timer 2 IRQ Clear (T2IC) register is used to clear an interrupt caused by Timer 2. Writing to this register, located at offset 0x34 from the address in BAR2, causes the interrupt from Timer 2 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

Timer 3 IRQ Clear (T3IC)

The Timer 3 IRQ Clear (T3IC) register is used to clear an interrupt caused by Timer 3. Writing to this register, located at offset 0x38 from the address in BAR2, causes the interrupt from Timer 3 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

Timer 4 IRQ Clear (T4IC)

The Timer 4 IRQ Clear (T4IC) register is used to clear an interrupt caused by Timer 4. Writing to this register, located at offset 0x3C from the address in BAR2, causes the interrupt from Timer 4 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

3.3.3 Watchdog Timer

General

The XVB601 provides a programmable Watchdog Timer (WDT) which can be used to reset the system if software integrity fails.

WDT Control Status Register (WCSR)

The WDT is controlled and monitored by the WDT Control Status Register (WCSR) which is located at offset 0x08 from the address in BAR2. The mapping of the bits in this register are as follows:

Table 3-59 WDT Control Status Register (WCSR)

Field	Bits	Read or Write
SERR/RST Select	WCSR[16]	Read/Write
WDT Timeout Select	WCSR[10..8]	Read/Write
WDT Enable	WCSR[0]	Read/Write
All of these bits default to "0" after system reset. All other bits are reserved.		

The "WDT Timeout Select" field is used to select the timeout value of the Watchdog Timer as follows

Table 3-60 WDT Timeout Select Field

Timeout	WCSR[10]	WCSR[9]	WCSR[8]
135 s	0	0	0
33.6 s	0	0	1
2.1 s	0	1	0
524 ms	0	1	1
262 ms	1	0	0
131 ms	1	0	1
32.768 ms	1	1	0
2.048 ms	1	1	1

The "SERR/RST Select" bit is used to select whether the WDT generates an SERR# on the local PCI bus or a system reset. If this bit is set to "0", the WDT will generate a system reset. Otherwise, the WDT will make the local PCI bus SERR# signal active.

The "WDT Enable" bit is used to enable the Watchdog Timer function. This bit must be set to "1" in order for the Watchdog Timer to function. Note that since all registers default to zero after reset, the Watchdog Timer is always disabled after a reset. The Watchdog Timer must be re-enabled by the application software after reset in order for the Watchdog Timer to continue to operate. Once the Watchdog Timer is enabled, the application software must refresh the Watchdog Timer within the selected timeout period to prevent a reset or SERR# from being generated. The Watchdog Timer is refreshed by performing a write to the WDT Keepalive register (WKPA). The data written is irrelevant.

WDT Keepalive Register (WKPA)

When enabled, the Watchdog Timer is prevented from resetting the system by writing to the WDT Keepalive Register (WKPA) located at offset 0x0C from the address in BAR2 within the selected timeout period. The data written to this location is irrelevant.

3.4 CompactFlash

The XVB601 features an optional onboard CompactFlash mass storage system with a capacity of up to 16 GByte. This CompactFlash appears to the user as an intelligent ATA (IDE) disk drive with the same functionality and capabilities as a “rotating media” IDE hard drive. The XVB601 BIOS includes an option to allow the board to boot from the CompactFlash.

The CompactFlash resides on the XVB601 as an IDE bus primary device.

3.5 Remote Ethernet Booting

The XVB601 is capable of booting from a server using the 10/100/1000 Mbit Ethernet ports over a network utilizing the Intel Boot Agent. The Intel Boot Agent gives you the ability to remotely boot the XVB601 using the PXE protocol. The Ethernet must be connected through one of the front panel (RJ45) connectors to boot remotely. This feature allows users to create systems without the worry of disk drive reliability, or the extra cost of adding CompactFlash drives.

BootWare Features:

- PXE boot support
- Unparalleled boot sector virus protection
- Detailed boot configuration screens
- Optional disabling of local boots
- Dual-boot option lets users select network or local booting

Maintenance

If a GE product malfunctions, please verify the following:

1. Software version resident on the product
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards are fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components or adjacent boards were disturbed when inserting or removing the board from the chassis
8. Quality of cables and I/O connections

If products must be returned, contact GE for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return from Customer Care.** RMA request forms can be obtained from:

repairs.huntsville.ip@ge.com

GE Customer Care is available at: 1-800-433-2682 in North America, or +1-780-401-7700 for international calls. Or, visit our website at:

www.ge-ip.com

Maintenance Prints

User level repairs are not recommended. The drawings and diagrams in this manual are for reference purposes only.

Compliance

This chapter provides the applicable information regarding regulatory compliance for the XVB601.

GE's XVB601 has been evaluated and has met the requirements for compliance to the following standards:

International Compliance

- EN55022:1998/CISPR 22:1997
- IEC61000-4-2
- IEC61000-4-3
- IEC61000-4-4
- IEC61000-4-5
- IEC61000-4-6

European Union (CE Mark)

- BS EN55024 (1998 w A1:01 & A2:03)
- BS EN55022 (Class A)

United States

- FCC Part 15, Subpart B, Section 109, Class A

Australia/New Zealand

- AS/NZS CISPR 22 (2002) Class A

Canada

- ICES-003 Class A

FCC Part 15

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Class A

NOTE

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

NOTE

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Canadian Regulations

The XVB601 Class A digital apparatus complies with Canadian ICES-003.

NOTE

Any equipment tested and found compliant with FCC Part 15 for unintentional radiators or EN55022 (previously CISPR 22) satisfies ICES-003.

A • Appendix A: Connectors and Pinouts

A.1 VME P1/P2

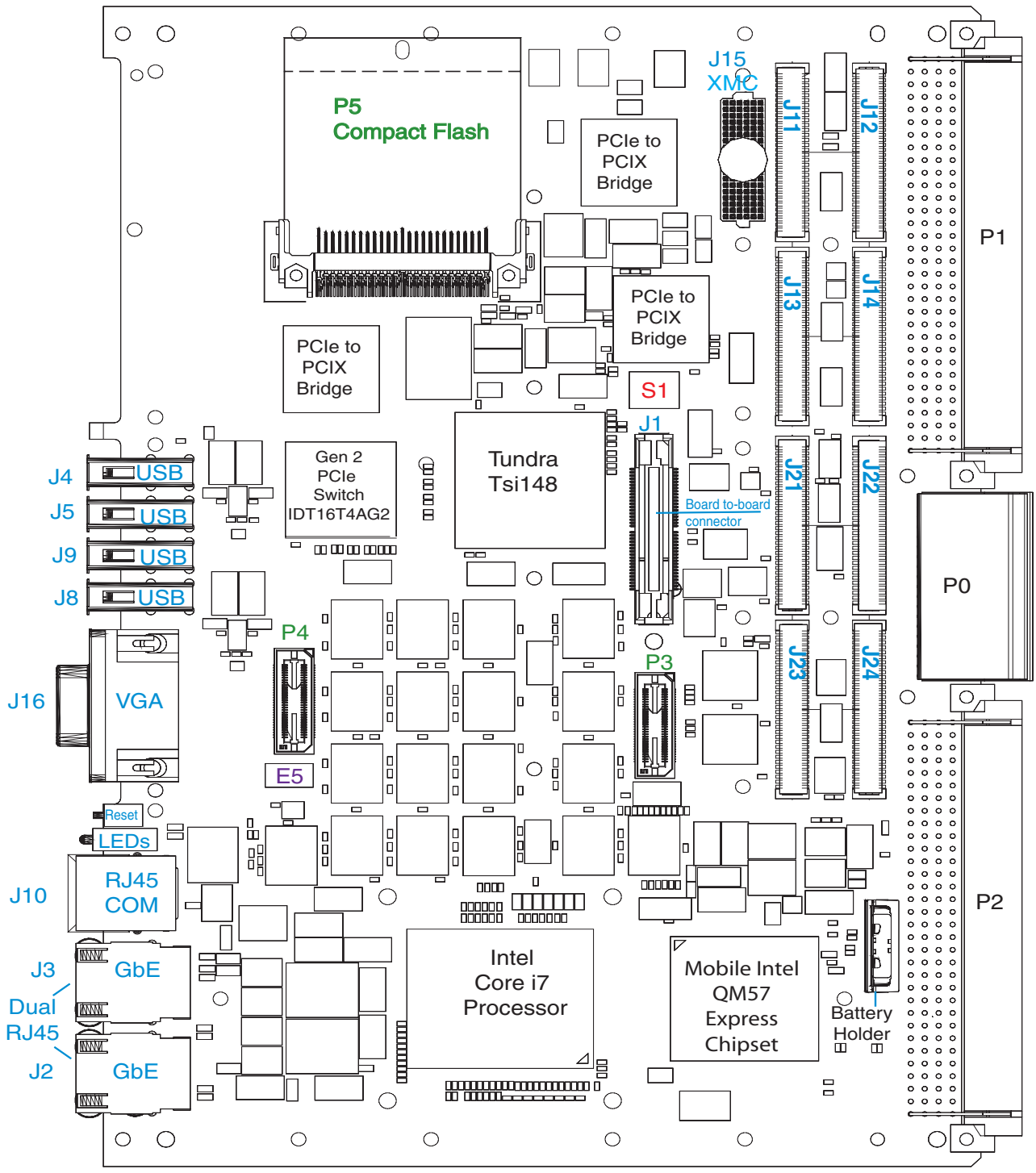
The XVB601 board contains two 5-row VMEbus connectors, as defined in the VITA 1.1-1997 specification, plus several connectors on the front panel. This appendix provides the contact signal assignments for these connectors.

Optionally, the XVB601 board contains a VMEbus VITA 1.1-1997 compatible P0 connector.

In the tables listed in this appendix, active low signals are identified with a trailing '-', '#', or 'N' attached to the signal name. Active high signals in a signal pair may have a trailing '+' or 'P' attached to the signal name.

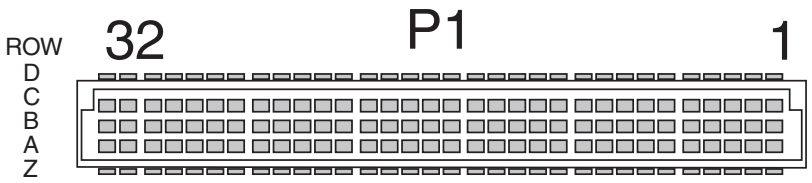
Internal board connectors and headers to support specific internal circuits such as the JTAG scan chain will be defined during design implementation and documented in the final product documents.

Figure A-1 XVB601 Connector Location Top Assembly



A.2 Backplane P1 Connector

Figure A-2 VME Connectors (P1)



The power, ground, and signal assignments on the backplane P1 connector are defined by the VITA 1 and VITA 1.1-1997 specifications. Note that the design is for a 5V-only backplane; the system does not provide power on the 3.3V rails assigned in the VITA specifications. The following table shows these signal assignments:

Table A-1 Backplane P1 Connector Signal Assignments

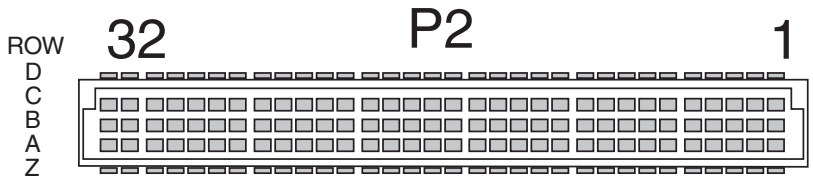
Pin	Row Z	Row A	Row B	Row C	Row D
1	N/C	D00	BBSY-	D08	5V (VPC)
2	GND	D01	BCLR-	D09	GND
3	N/C	D02	ACFAIL-	D10	N/C
4	GND	D03	BG0IN-	D11	N/C
5	N/C	D04	BG0OUT-	D12	N/C
6	GND	D05	BG1IN-	D13	N/C
7	N/C	D06	BG1OUT-	D14	N/C
8	GND	D07	BG2IN-	D15	N/C
9	N/C	GND	BG2OUT-	GND	GAP
10	GND	SYSCLK	BG3IN-	SYSFAIL-	GA0
11	N/C	GND	BG3OUT-	BERR-	GA1
12	GND	DS1-	BR0-	SYSRESET-	N/C
13	N/C	DS0-	BR1-	LWORD-	GA2
14	GND	WRITE-	BR2-	AM5	N/C
15	N/C	GND	BR3-	A23	GA3
16	GND	DTACK-	AM0	A22	N/C
17	N/C	GND	AM1	A21	GA4
18	GND	AS-	AM2	A20	N/C
19	N/C	GND	AM3	A19	N/C
20	GND	IACK-	GND	A18	N/C
21	N/C	IACKIN-	SERA	A17	N/C
22	GND	IACKOUT-	SERB	A16	N/C
23	N/C	AM4	GND	A15	N/C
24	GND	A07	IRQ7-	A14	N/C
25	N/C	A06	IRQ6-	A13	N/C
26	GND	A05	IRQ5-	A12	N/C
27	N/C	A04	IRQ4-	A11	N/C
28	GND	A03	IRQ3-	A10	N/C
29	N/C	A02	IRQ2-	A09	N/C
30	GND	A01	IRQ1-	A08	N/C
31	N/C	-12V	5V_STDBY	+12V	GND
32	GND	5V	5V	5V	5V (VPC)

Table A-2 Legend Backplane P1 Connector Signal Assignments

Legend	Description	Pin Count
	VME/VME64x Definitions (VITA 1 / 1.1)	123
	Not Used (Misc VITA 1.1 functions)	37
Total Pins		160

A.3 Backplane P2 Connector

Figure A-3 VME Connectors (P2)



The backplane P2 connector contains the upper 16-bits of the backplane VMEbus, additional power and ground leads, and port wiring for the rear access ports on the XVB601 (SATA ports, USB ports, RS232 COM port, and partial PMC rear I/O port). The VMEbus and power / ground signal assignments are specified in the VITA 1-1994 specification, and the partial PMC rear I/O signal assignments are defined in the VITA 35-2000 specification, Section 2.4. The following table shows these signal assignments:

Table A-3 Backplane P2 Connector Signal Assignments

Pin	Row z	Row a	Row b	Row c	Row d
1	PMC2_IO02	GND	5V	COM2_TX	PMC2_IO01
2	GND	USB_P7N	GND	COM2_RTS	PMC2_IO03
3	PMC2_IO05	USB_P7P	No Connect [1]	COM2_DTR	PMC2_IO04
4	GND	USB_OC7#	A24	COM2_RX	PMC2_IO06
5	PMC2_IO08	GND	A25	COM2_DCD	PMC2_IO07
6	GND	USB_P6N	A26	COM2_CTS	PMC2_IO09
7	PMC2_IO11	USB_P6P	A27	COM2_DSR	PMC2_IO10
8	GND	USB_OC6#	A28	COM2_RI	PMC2_IO12
9	PMC2_IO14	GND	A29	RTM_GPIO	PMC2_IO13
10	GND	USB_P5P	A30	P5V	PMC2_IO15
11	PMC2_IO17	USB_P5N	A31	N12V	PMC2_IO16
12	GND	USB_OC5#	GND	GND	PMC2_IO18
13	PMC2_IO20	GND	5V	SATA1_RXN	PMC2_IO19
14	GND	USB_P4N	D16	SATA1_RXP	PMC2_IO21
15	PMC2_IO23	USB_P4P	D17	GND	PMC2_IO22
16	GND	USB_OC4#	D18	SATA1_TXN	PMC2_IO24
17	PMC2_IO26	GND	D19	SATA1_TXP	PMC2_IO25
18	GND	P5V	D20	GND	PMC2_IO27
19	PMC2_IO29	P12V	D21	GND	PMC2_IO28
20	GND	GND	D22	SATA2_RXN	PMC2_IO30
21	PMC2_IO32	DVI_TXCN	D23	SATA2_RXP	PMC2_IO31
22	GND	DVI_TXCP	GND	GND	PMC2_IO33
23	PMC2_IO35	GND	D24	SATA2_TXN	PMC2_IO34
24	GND	DVI_TX0N	D25	SATA2_TXP	PMC2_IO36
25	PMC2_IO38	DVI_TX0P	D26	GND	PMC2_IO37
26	GND	GND	D27	GND	PMC2_IO39
27	PMC2_IO41	DVI_TX1N	D28	GND	PMC2_IO40
28	GND	DVI_TX1P	D29	GND	PMC2_IO42
29	PMC2_IO44	GND	D30	DVI_DDC_CLK	PMC2_IO43
30	GND	DVI_TX2N	D31	DVI_DDC DATA	PMC2_IO45
31	PMC2_IO46	DVI_TX2P	GND	DVI Hot Plug	GND
32	GND	GND	5V	RSVD 3.3V STBY	RSVD 5V (VPC)

Legend Backplane P2 Connector Signal Assignments

Legend	Description	Pin Count
	VME / VME64x Definitions (VITA 1/1.1)	50
	PMC0 Rear access (VITA 35, Sect 2.4.2)	46
	COM2 RS-232 Port	9
	DVI Port	11
	SATA Ports	8
	USB Ports	12
	Misc Power/GND or Unused Pins	24
Total Pins		160

A.4 Optional Vita 1.1 (P0) Connector

Figure A-4 P0 Connector

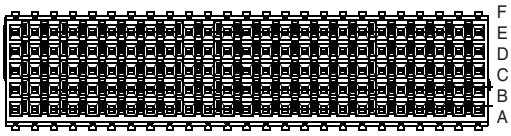


Table A-4 Optional VME P0 Connector Signal Assignments

Pos	P0 Row Z	P0 Row A	P0 Row B	P0 Row C	P0 Row D	P0 Row E	P0 Row F
1	GND	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	GND
2	GND			GPIO7	GPIO6	GPIO5	GND
3	GND						GND
4	GND	PMC1_IO05	PMC1_IO04	PMC1_IO03	PMC1_IO02	PMC1_IO01	GND
5	GND	PMC1_IO10	PMC1_IO09	PMC1_IO08	PMC1_IO07	PMC1_IO06	GND
6	GND	PMC1_IO15	PMC1_IO14	PMC1_IO13	PMC1_IO12	PMC1_IO11	GND
7	GND	PMC1_IO20	PMC1_IO19	PMC1_IO18	PMC1_IO17	PMC1_IO16	GND
8	GND	PMC1_IO25	PMC1_IO24	PMC1_IO23	PMC1_IO22	PMC1_IO21	GND
9	GND	SATA0_Tx+	SATA0_Tx-	GND	SATA0_Rx+	SATA0_Rx-	GND
10	GND	SATA1_Tx+	SATA1_Tx-	GND	SATA1_Rx+	SATA1_Rx-	GND
11	GND						GND
12	GND	PMC1_IO30	PMC1_IO29	PMC1_IO28	PMC1_IO27	PMC1_IO26	GND
13	GND	PMC1_IO35	PMC1_IO34	PMC1_IO33	PMC1_IO32	PMC1_IO31	GND
14	GND	PMC1_IO40	PMC1_IO39	PMC1_IO38	PMC1_IO37	PMC1_IO36	GND
15	GND	PMC1_IO45	PMC1_IO44	PMC1_IO43	PMC1_IO42	PMC1_IO41	GND
16	GND	PMC1_IO50	PMC1_IO49	PMC1_IO48	PMC1_IO47	PMC1_IO46	GND
17	GND	PMC1_IO55	PMC1_IO54	PMC1_IO53	PMC1_IO52	PMC1_IO51	GND
18	GND	PMC1_IO60	PMC1_IO59	PMC1_IO58	PMC1_IO57	PMC1_IO56	GND
19	GND	GND	PMC1_IO64	PMC1_IO63	PMC1_IO62	PMC1_IO61	GND

A.5 Serial Port Connector RJ45 (J10)

COM 1 Serial Port Connector is a standard RJ45 connector as shown in the figure and table below:

Figure A-5 Serial Connector (J10)

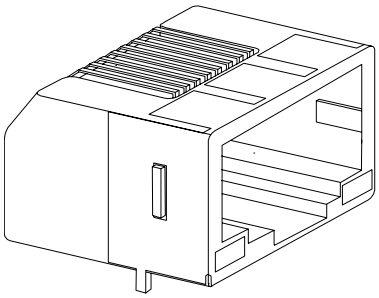


Table A-5 Serial Connector Pinout (J10)

Pin	RS232 Signal	RS422 Signal
1	DCD	RXD+
2	RTS	RTS-
3	GND	TXD+
4	TXD	TXD-
5	RXD	RXD-
6	GND	GND or CTS+ (jumper selectable)
7	CTS	CTS-
8	DTR	RTS+

NOTE: See the appropriate table of jumper and switch settings for configuring.

A.6 USB Connectors and Pinout (J4, J5, J8, J9)

The four USB ports are industry standard 4-position shielded connectors. The figure below depicts a representation of the connectors, and table that follows shows the pinout (same for each).

Figure A-6 USB Port

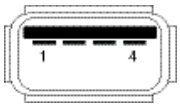


Table A-6 USB Connectors (J4, J5, J8, J9)

Pin	Signal	Function
1	USB_VCC	USB Power
2	USB-	USB Data -
3	USB+	USB Data +
4	USBG	USB Ground

A.7 Video Graphics Adapter and Pinout (J16)

The video port uses a standard high-density DB15 VGA connector. **Figure A-7** illustrates the pinout and **Table A-7** provides a description.

Figure A-7 VGA Connector and Pinout (J16)

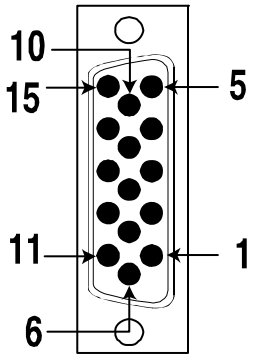


Table A-7 VGA Connector Pinout (J16)

Pin	Signal
1	VGA_Video1_Red
2	VGA_Video1_Green
3	VGA_Video1_Blue
4	N/C
5	GND
6	GND
7	GND
8	GND
9	VCC_5.0
10	GND
11	N/C
12	VGA_DDC_Data
13	VGA_HSYNC
14	VGA_VSYNC
15	VGA_DDC_CLK

N/C indicates No Connection

A.8 Gigabit Ethernet Connector and Pinout (J2, J3)

The pinout diagram for the Gigabit Ethernet connector and pinout are shown in the following figure and table:

Figure A-8 GbE Connector

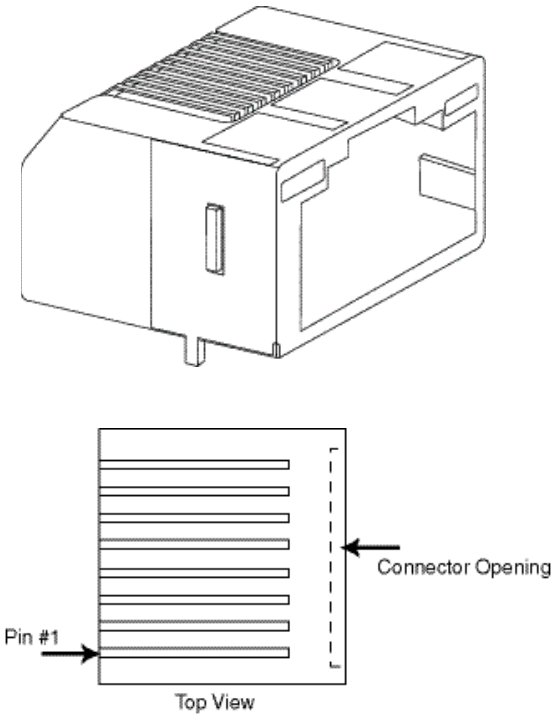


Table A-8 Ethernet Connectors 10/100/1000 Mbit (J2, J3)

Pin	Signals	Signals
1	MDI0+	TX/RX0+
2	MDI0-	TX/RX0-
3	MDI1+	TX/RX1-
4	MDI1-	TX/RX1+
5	MDI2+	TX/RX2-
6	MDI2-	TX/RX2+
7	MDI3+	TX/RX3-
8	MDI3-	TX/RX3+

A.9 PMC Site 1 Connector and Pinouts

The PCI Mezzanine Card (PMC) carries the same signals as the PCI standard; however, the PMC standard uses a completely different form factor. **Table A-9** through **Table A-12** are the pinouts for the XMC/PMC connectors (J11, J12, J13 and J14).

A.9.1 PMC Connector and Pinouts (J11)

Figure A-9 PMC Connector and Pinouts (J11)

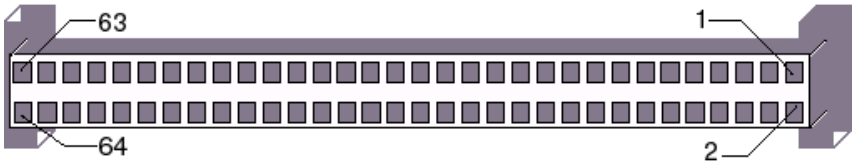


Table A-9 PMC Connector Pinouts (J11)

PMC Connector (J11)				PMC Connector (J11)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	JTAG.TCK	2	-12	33	FRAME#	34	GND
3	GND	4	INTA3	35	GND	36	IRDY#
5	INTB#	6	INTC#	37	DEVSEL#	38	+5 V
7	BMODE1	8	+5 V	39	PCIXCAP	40	LOCK#
9	INTD#	10	NC	41	SDONE#	42	+3.3V
11	GND	12	NC	43	PAR	44	GND
13	CLK	14	GND	45	PMC VIO*	46	AD[15]
15	GND	16	GNT#	47	AD[12]	48	AD[11]
17	REQ#	18	+5 V	49	AD[9]	50	+5 V
19	PMC VIO*	20	AD[31]	51	GND	52	C/BE[0]#
21	AD[28]	22	AD[27]	53	AD[6]	54	AD[5]
23	AD[25]	24	GND	55	AD[4]	56	GND
25	GND	26	C/BE[3]#	57	PMC VIO*	58	AD[3]
27	AD[22]	28	AD[21]	59	AD[2]	60	AD[1]
29	AD[19]	30	+5 V	61	AD[0]	62	+5 V
31	PMC VIO*	32	AD[17]	63	GND	64	REQ64#

NOTE: *PMC VIO is determined by the location of the PMC keypin.

A.9.2 PMC Connector and Pinouts (J12)

Figure A-10 PMC Connector and Pinouts (J12)

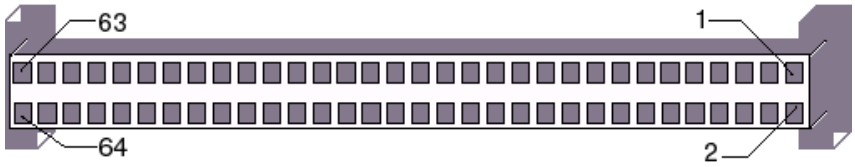


Table A-10 PMC Connector Pinouts (J12)

PMC Connector (J12)				PMC Connector (J12)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	+12 V	2	JTAG_TRST	33	GND	34	NC
3	JTAG_TMS_2	4	JTAG_TDO	35	TRDY#	36	+3.3V
5	JTAG_TDI	6	GND	37	GND	38	STOP#
7	GND	8	NC	39	PERR#	40	GND
9	NC	10	NC	41	+3.3V	42	SERR#
11	+3.3V	12	+3.3V	43	C/BE[1]#	44	GND
13	RST#	14	GND	45	AD[14]	46	AD[13]
15	+3.3V	16	GND	47	M66EN	48	AD[10]
17	PME#	18	GND	49	AD[8]	50	+3.3V
19	AD[30]	20	AD[29]	51	AD[7]	52	NC
21	GND	22	AD[26]	53	+3.3V	54	NC
23	AD[24]	24	+3.3V	55	NC	56	GND
25	IDSEL	26	AD[23]	57	NC	58	NC
27	+3.3V	28	AD[20]	59	GND	60	NC
29	AD[18]	30	GND	61	ACK64#	62	+3.3V
31	AD[16]	32	C/BE[2]#	63	GND	64	NC

A.9.3 PMC2 Connector and Pinouts (J13)

Figure A-11 PMC2 Connector and Pinouts (J13)

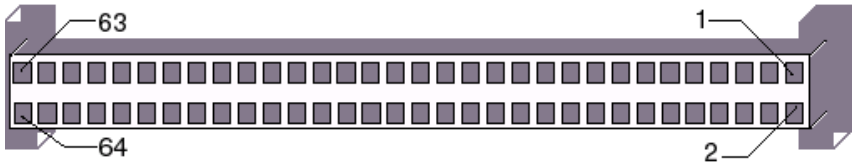


Table A-11 PMC2 Connector Pinouts (J13)

PMC2 Connector (J13)				PMC2 Connector (J13)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	NC	2	GND	33	GND	34	AD[48]
3	GND	4	CBE[7]#	35	AD[47]	36	AD[46]
5	CBE[6]#	6	CBE[5]	37	AD[45]	38	GND
7	CBE[4]#	8	GND	39	PMC VIO*	40	AD[44]
9	PMC VIO*	10	PAR64	41	AD[43]	42	AD[42]
11	AD[63]	12	AD[62]	43	AD[41]	44	GND
13	AD[61]	14	GND	45	GND	46	AD[40]
15	GND	16	AD[60]	47	AD[39]	48	AD[38]
17	AD[59]	18	AD[58]	49	AD[37]	50	GND
19	AD[57]	20	GND	51	GND	52	AD[36]
21	PMC VIO*	22	AD[56]	53	AD[35]	54	AD[34]
23	AD[55]	24	AD[54]	55	AD[33]	56	GND
25	AD[53]	26	GND	57	PMC VIO*	58	AD[32]
27	GND	28	AD[52]	59	NC	60	NC
29	AD[51]	30	AD[50]	61	NC	62	GND
31	AD[49]	32	GND	63	GND	64	NC

NOTE: *PMC VIO is determined by the location of the PMC keypin.

A.9.4 PMC1 Connector and Pinouts (J14)

Figure A-12 PMC1 Connector and Pinouts (J14)

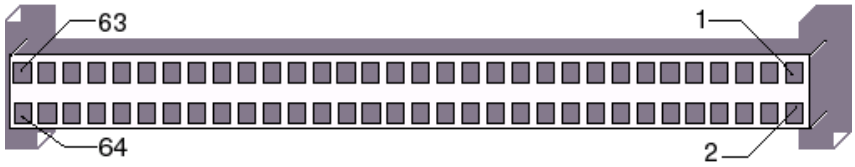


Table A-12 PMC1 Connector Pinouts (J14)

PMC1 Connector (J14)						PMC1 Connector (J14)					
Left Side			Right Side			Left Side			Right Side		
Pin	Name	Connected To	Pin	Name	Connected To	Pin	Name	Connected To	Pin	Name	Connected To
1	CONN[1]	P0 pin E4	2	CONN[2]	P0 pin D4	33	CONN[33]	P0 pin C13	34	CONN[34]	P0 pin B13
3	CONN[3]	P0 pin C4	4	CONN[4]	P0 pin B4	35	CONN[35]	P0 pin A13	36	CONN[36]	P0 pin E14
5	CONN[5]	P0 pin A4	6	CONN[6]	P0 pin E5	37	CONN[37]	P0 pin D14	38	CONN[38]	P0 pin C14
7	CONN[7]	P0 pin D5	8	CONN[8]	P0 pin C5	39	CONN[39]	P0 pin B14	40	CONN[40]	P0 pin A14
9	CONN[9]	P0 pin B5	10	CONN[10]	P0 pin A5	41	CONN[41]	P0 pin E15	42	CONN[42]	P0 pin D15
11	CONN[11]	P0 pin E6	12	CONN[12]	P0 pin D6	43	CONN[43]	P0 pin C15	44	CONN[44]	P0 pin B15
13	CONN[13]	P0 pin C6	14	CONN[14]	P0 pin B6	45	CONN[45]	P0 pin A15	46	CONN[46]	P0 pin E16
15	CONN[15]	P0 pin A6	16	CONN[16]	P0 pin E7	47	CONN[47]	P0 pin D16	48	CONN[48]	P0 pin C16
17	CONN[17]	P0 pin D7	18	CONN[18]	P0 pin C7	49	CONN[49]	P0 pin B16	50	CONN[50]	P0 pin A16
19	CONN[19]	P0 pin B7	20	CONN[20]	P0 pin A7	51	CONN[51]	P0 pin E17	52	CONN[52]	P0 pin D17
21	CONN[21]	P0 pin E8	22	CONN[22]	P0 pin D8	53	CONN[53]	P0 pin C17	54	CONN[54]	P0 pin B17
23	CONN[23]	P0 pin C8	24	CONN[24]	P0 pin B8	55	CONN[55]	P0 pin A17	56	CONN[56]	P0 pin E18
25	CONN[25]	P0 pin A8	26	CONN[26]	P0 pin E12	57	CONN[57]	P0 pin D18	58	CONN[58]	P0 pin C18
27	CONN[27]	P0 pin D12	28	CONN[28]	P0 pin C12	59	CONN[59]	P0 pin B18	60	CONN[60]	P0 pin A18
29	CONN[29]	P0 pin B12	30	CONN[30]	P0 pin A12	61	CONN[61]	P0 pin E19	62	CONN[62]	P0 pin D19
31	CONN[31]	P0 pin E13	32	CONN[32]	P0 pin D13	63	CONN[63]	P0 pin C19	64	CONN[64]	P0 pin B19

A.10 XMC Connector and Pinouts (J15)

Figure A-13 XMC Connector and Pinouts (J15)

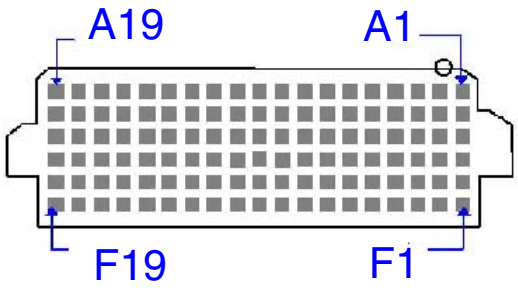


Table A-13 XMC Connector Pinouts (J15)

Row A		Row B		Row C		Row D		Row E		Row F	
1	TX8+	1	TX8-	1	3.3V	1	TX9+	1	TX9-	1	5V
2	GND	2	GND	2	TRST#	2	GND	2	GND	2	RST#
3	TX10+	3	TX10-	3	3.3V	3	TX11+	3	TX11-	3	5V
4	GND	4	GND	4	TCK	4	GND	4	GND	4	MRSTO#
5	NC	5	NC	5	3.3V	5	NC	5	NC	5	5V
6	GND	6	GND	6	TMS	6	GND	6	GND	6	12V
7	NC	7	NC	7	3.3V	7	NC	7	NC	7	5V
8	GND	8	GND	8	TDI	8	GND	8	GND	8	-12V
9	NC	9	NC	9	NC	9	NC	9	NC	9	5V
10	GND	10	GND	10	TDO	10	GND	10	GND	10	GA0
11	RX8+	11	RX8-	11	MBIST#	11	RX9+	11	RX9-	11	5V
12	GND	12	GND	12	GA1	12	GND	12	GND	12	PRS#
13	RX10+	13	RX10-	13	3.3V	13	RX11+	13	RX11-	13	5V
14	GND	14	GND	14	GA2	14	GND	14	GND	14	MSDA
15	NC	15	NC	15	NC	15	NC	15	NC	15	5V
16	GND	16	GND	16	MVRMO	16	GND	16	GND	16	MSCL
17	NC	17	NC	17	RSVD	17	NC	17	NC	17	NC
18	GND	18	GND	18	NC	18	GND	18	GND	18	NC
19	CLK+	19	CLK-	19	NC	19	WAKE#	19	ROOT#	19	NC

A.11 PMC Site 2 Connectors (J21, J22, J23, J24)

The PCI Mezzanine Card (PMC) carries the same signals as the PCI standard; however, the PMC standard uses a completely different form factor. **Table A-14** through **Table A-17** are the pinouts for the PMC connectors (J21, J22, J23 and J24).

A.11.1 PMC Connector and Pinouts (J21)

Figure A-14 PMC Connector and Pinouts (J21)

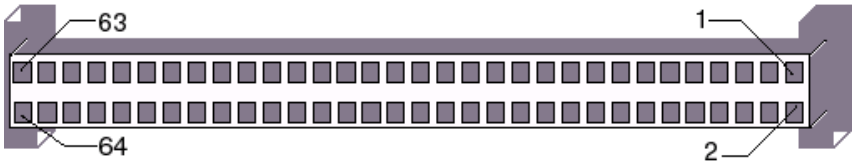


Table A-14 PMC Connector Pinouts (J21)

PMC Connector (J21)				PMC Connector (J21)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	JTAG.TCK	2	-12	33	FRAME#	34	GND
3	GND	4	INTA3	35	GND	36	IRDY#
5	INTB#	6	INTC#	37	DEVSEL#	38	+5 V
7	BMODE1	8	+5 V	39	PCIXCAP	40	LOCK#
9	INTD#	10	NC	41	SDONE#	42	+3.3V
11	GND	12	NC	43	PAR	44	GND
13	CLK	14	GND	45	PMC VIO*	46	AD[15]
15	GND	16	GNT#	47	AD[12]	48	AD[11]
17	REQ#	18	+5 V	49	AD[9]	50	+5 V
19	PMC VIO*	20	AD[31]	51	GND	52	C/BE[0]#
21	AD[28]	22	AD[27]	53	AD[6]	54	AD[5]
23	AD[25]	24	GND	55	AD[4]	56	GND
25	GND	26	C/BE[3]#	57	PMC VIO*	58	AD[3]
27	AD[22]	28	AD[21]	59	AD[2]	60	AD[1]
29	AD[19]	30	+5 V	61	AD[0]	62	+5 V
31	PMC VIO*	32	AD[17]	63	GND	64	REQ64#

NOTE: *PMC VIO is determined by the location of the PMC keypin.

A.11.2 PMC Connector and Pinouts (J22)

Figure A-15 PMC Connector and Pinouts (J22)

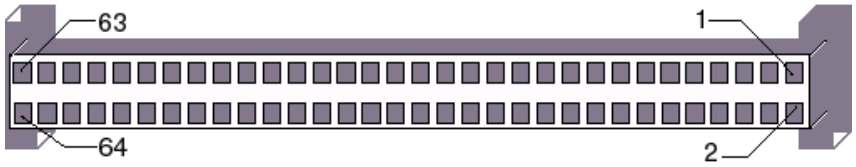


Table A-15 PMC Connector Pinouts (J22)

PMC Connector (J22)				PMC Connector (J22)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	+12 V	2	JTAG_TRST	33	GND	34	NC
3	JTAG_TMS_2	4	JTAG_TDO	35	TRDY#	36	+3.3V
5	JTAG_TDI	6	GND	37	GND	38	STOP#
7	GND	8	NC	39	PERR#	40	GND
9	NC	10	NC	41	+3.3V	42	SERR#
11	+3.3V	12	+3.3V	43	C/BE[1]#	44	GND
13	RST#	14	GND	45	AD[14]	46	AD[13]
15	+3.3V	16	GND	47	M66EN	48	AD[10]
17	PME#	18	GND	49	AD[8]	50	+3.3V
19	AD[30]	20	AD[29]	51	AD[7]	52	NC
21	GND	22	AD[26]	53	+3.3V	54	NC
23	AD[24]	24	+3.3V	55	NC	56	GND
25	IDSEL	26	AD[23]	57	NC	58	NC
27	+3.3V	28	AD[20]	59	GND	60	NC
29	AD[18]	30	GND	61	ACK64#	62	+3.3V
31	AD[16]	32	C/BE[2]#	63	GND	64	NC

A.11.3 PMC Connector and Pinouts (J23)

Figure A-16 PMC Connector and Pinouts (J23)

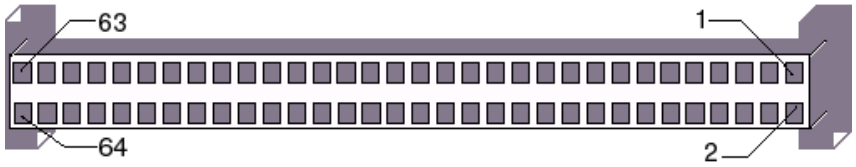


Table A-16 PMC Connector Pinouts (J23)

PMC Connector (J23)				PMC Connector (J23)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	NC	2	GND	33	GND	34	AD[48]
3	GND	4	CBE[7]#	35	AD[47]	36	AD[46]
5	CBE[6]#	6	CBE[5]	37	AD[45]	38	GND
7	CBE[4]#	8	GND	39	PMC VIO*	40	AD[44]
9	PMC VIO*	10	PAR64	41	AD[43]	42	AD[42]
11	AD[63]	12	AD[62]	43	AD[41]	44	GND
13	AD[61]	14	GND	45	GND	46	AD[40]
15	GND	16	AD[60]	47	AD[39]	48	AD[38]
17	AD[59]	18	AD[58]	49	AD[37]	50	GND
19	AD[57]	20	GND	51	GND	52	AD[36]
21	PMC VIO*	22	AD[56]	53	AD[35]	54	AD[34]
23	AD[55]	24	AD[54]	55	AD[33]	56	GND
25	AD[53]	26	GND	57	PMC VIO*	58	AD[32]
27	GND	28	AD[52]	59	NC	60	NC
29	AD[51]	30	AD[50]	61	NC	62	GND
31	AD[49]	32	GND	63	GND	64	NC

NOTE: *PMC VIO is determined by the location of the PMC keypin.

A.11.4 PMC Connector and Pinouts (J24)

Figure A-17 PMC Connector and Pinouts (J24)

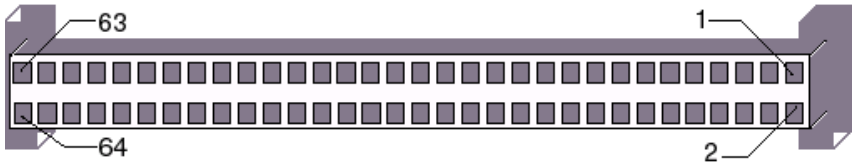


Table A-17 PMC Connector Pinouts (J24)

PMC Connector (J24)						PMC Connector (J24)					
Left Side			Right Side			Left Side			Right Side		
Pin	Name	Connected To	Pin	Name	Connected To	Pin	Name	Connected To	Pin	Name	Connected To
1	CONN[1]	P2 pin D1	2	CONN[2]	P2 pin Z1	33	CONN[33]	P2 pin D22	34	CONN[34]	P2 pin D23
3	CONN[3]	P2 pin D2	4	CONN[4]	P2 pin D3	35	CONN[35]	P2 pin Z23	36	CONN[36]	P2 pin D24
5	CONN[5]	P2 pin Z3	6	CONN[6]	P2 pin D4	37	CONN[37]	P2 pin D25	38	CONN[38]	P2 pin Z25
7	CONN[7]	P2 pin D5	8	CONN[8]	P2 pin Z5	39	CONN[39]	P2 pin D26	40	CONN[40]	P2 pin D27
9	CONN[9]	P2 pin D6	10	CONN[10]	P2 pin D7	41	CONN[41]	P2 pin Z27	42	CONN[42]	P2 pin D28
11	CONN[11]	P2 pin Z7	12	CONN[12]	P2 pin D8	43	CONN[43]	P2 pin D29	44	CONN[44]	P2 pin Z29
13	CONN[13]	P2 pin D9	14	CONN[14]	P2 pin Z9	45	CONN[45]	P2 pin D30	46	CONN[46]	P2 pin Z31
15	CONN[15]	P2 pin D10	16	CONN[16]	P2 pin D11	47	CONN[47]	NC	48	CONN[48]	NC
17	CONN[17]	P2 pin Z11	18	CONN[18]	P2 pin D12	49	CONN[49]	NC	50	CONN[50]	NC
19	CONN[19]	P2 pin D13	20	CONN[20]	P2 pin Z13	51	CONN[51]	NC	52	CONN[52]	NC
21	CONN[21]	P2 pin D14	22	CONN[22]	P2 pin D15	53	CONN[53]	NC	54	CONN[54]	NC
23	CONN[23]	P2 pin Z15	24	CONN[24]	P2 pin D16	55	CONN[55]	NC	56	CONN[56]	NC
25	CONN[25]	P2 pin D17	26	CONN[26]	P2 pin Z17	57	CONN[57]	NC	58	CONN[58]	NC
27	CONN[27]	P2 pin D18	28	CONN[28]	P2 pin D19	59	CONN[59]	NC	60	CONN[60]	NC
29	CONN[29]	P2 pin Z19	30	CONN[30]	P2 pin D20	61	CONN[61]	NC	62	CONN[62]	NC
31	CONN[31]	P2 pin D21	32	CONN[32]	P2 pin Z21	63	CONN[63]	NC	64	CONN[64]	NC

A.11.5 Board to Board Connector (J1)

The Board to Board Connector, J1 is only for use with GE expansion products designed for the XVB601. (See **Figure A-1 *XVB601 Connector Location Top Assembly*** on page 90). Please contact the GE sales representative for more information.

B • Appendix B: BIOS Setup Utility

This appendix gives a brief description of the setup options in the system BIOS firmware. Due to the custom nature of GE's SBCs, your BIOS firmware, options may vary from the options discussed in this appendix.

To Access the First Boot setup screen, press the F7 key at the beginning of boot.

To access the setup screens, press the DEL key at the beginning of boot.

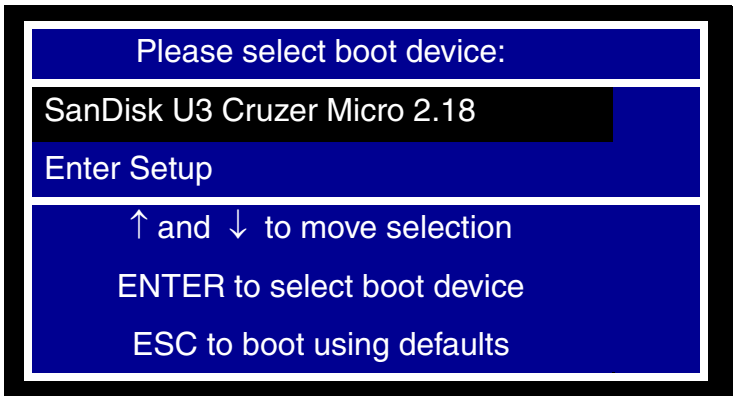
B.1 First Boot Menu

The XVB601 has a First Boot menu enabling the user to, *on a one time basis*, select a drive device to boot from. This feature is useful when installing from a bootable disk. For example, when installing an operating system from a CD, enter the First Boot menu and use the arrows keys to highlight ATAPI CD-ROM Drive. Press ENTER to continue with system boot.

This feature is accessed by pressing the F7 key at the very beginning of the boot cycle. The selection made from this screen applies to the current boot only, and will not be used during the next boot-up of the system.

If you have trouble accessing this feature, disable the QuickBoot Mode in the Main BIOS firmware, setup screen. Exit, saving changes and retry accessing the First Boot menu.

Table B-1 BIOS firmware, First Boot Menu



B.2 Main Menu

The **Main** next-generation BIOS firmware, setup menu screen has two main areas. The left frame displays the options that can be configured. The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white and a text message in the right frame gives a brief description of the option.

The Main menu reports the BIOS firmware, revision, processor type and clock speed, and allows the user to set the system's clock and calendar. Use the left and right arrow keys to select other screens.

NOTE

Below is a sample of the Main screen. The information displayed on your screen will reflect your actual system.

Table B-2 BIOS Main Menu

Aptio Setup Utility - Copyright (C) 2009 American Megatrends, Inc.

Main | Advanced | Chipset | Boot | Security | Save & Exit

BIOS Information

BIOS Vendor	American Megatrends
Core Version	4.6.3.5
Project Version	xvb6_413 x64
Build Date	02/08/2010 13:21:00
UnCore Information	
IGD VBIOS Version	1973
GMCH Version	12 [C2 Stepping]
Total Memory	8192 MB [DDR: 1067 MHz]
Memory Slot0	4096 MB (DDR3)
Memory Slot2	4096 MB (DDR3)
➢Platform Information	
System Language	[English]
System Date	[Wed 02/10/2010]
System Time	[15:55:32]
Access Level	Administrator

Platform Information

→← Select Screen
↑↓ Select Item
Enter: Select
+/- Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit

Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

B.3 Advanced Setup Menu

The **Advanced** BIOS firmware, Setup menu allows the user to configure some CPU settings, the IDE bus, SCSI devices and other external devices and internal drives.

Select the *Advanced* tab from the setup screen to enter the Advanced BIOS firmware, Setup screen. You can select the items in the left frame of the screen, such as Super I/O Configuration, to go to the sub menu for that item. You can display an Advanced BIOS firmware, Setup option by highlighting it using the <Arrow> keys. A sample of the Advanced BIOS firmware, Setup screen is shown below.

NOTE

Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the BIOS firmware. From the Exit menu select '`Load Failsafe Defaults`' and reboot the system. If the system failure prevents access to the BIOS firmware, screens, refer to Section **1.4.3** ***Clear CMOS/RTC/Password*** on page 31 for instructions on clearing the CMOS.

Table B-3 BIOS Advanced Menu

Aptio Setup Utility - Copyright (C) 2009 American Megatrends, Inc.

Main | Advanced | Chipset | Boot | Security | Save & Exit

Legacy OpROM Support
Launch Storage OpROM [Enabled]

- PCI Subsystem Settings
- ACPI Settings
- S5 RTC Wake Settings
- CPU Configuration
- Onboard Device
- Thermal Configuration
- Port 80h
- USB Configuration
- Super IO Configuration
- Serial Port Console Redirection
- Network Stack

Enable or Disable Boot Option for Legacy Mass Storage Devices with Option ROM.

→← Select Screen
↑↓ Select Item
Enter: Select
+/- Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit

Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

Options shown may not be available on your system.

B.4 Chipset Setup Menu

Select the various options for chipsets located in the system (for example, the CPU configuration and configurations for the North and South Bridge). The settings for the chipsets are processor dependent and care must be used when changing settings from the defaults set at the factory.

Below is a sample of the **Chipset** Setup screen; the actual options on your system may vary.

NOTE

Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the BIOS firmware. From the Exit menu select 'Load Failsafe Defaults' and reboot the system. If the system failure prevents access to the BIOS firmware, screens, refer to Section **1.4.3** ***Clear CMOS/RTC/Password*** on page 31 for instructions on clearing the CMOS.

Table B-4 BIOS Chipset Menu

Aptio Setup Utility - Copyright (C) 2009 American Megatrends, Inc.

Main | Advanced | Chipset | Boot | Security | Save & Exit

Enable CRID [Disabled]

➢ North Bridge Configuration

➢ South Bridge Configuration

Enable Compatible Revision ID

→← Select Screen
↑↓ Select Item
Enter: Select
+/- Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit

Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

B.4.1 Enabling/Disabling the GbE boot-from-LAN BIOS firmware

The Gigabit Ethernet boot-from-LAN BIOS firmware, provides support for booting over the network.

NOTE

In order to boot from the network, some operating systems require that the network driver be set to "boot" within the Control Panel.

The Gigabit Ethernet boot-from-LAN BIOS firmware, defaults to Disabled in the BIOS firmware, Setup Utility. The Chipset menu of the BIOS firmware, Setup Utility allows the boot-from-LAN BIOS firmware, to be Enabled or Disabled. **Table B-4 on page 111** shows the Chipset Menu. Use the arrow keys to highlight the Onboard Device Configuration. Select 'GigE Option ROM' in the submenu's list and enter <+> until the option is set to Enabled or Disabled. Press F10 to Save and Exit the BIOS firmware, Setup Utility.

B.5 Boot Setup Menu

Use the **Boot** Setup menu to set the priority of the boot devices, including booting from a remote network. The devices shown in this menu are the bootable devices detected during POST. If a drive is installed that does not appear, verify the hardware installation. Also available in this screen are "Boot Settings" which allow the user to set how the basic system will act, for example, support for PS/2 mouse and whether to use "Quick Boot" or not.

Table B-5 BIOS Boot Menu

Aptio Setup Utility - Copyright (C) 2009 American Megatrends, Inc.

Main | Advanced | Chipset | Boot | Security | Save & Exit

Boot Configuration		Enables/Disables Quiet Boot option.
UEFI Boot	[Disabled]	
Setup Prompt Timeout	2	
Bootup NumLock State	[On]	
CSM16 Module Version	07.60	
GateA20 Active	[Upon Request])	
Option ROM Messages	[Force BIOS]	
Interrupt 19 Capture	[Disabled]	
Boot Option Priorities		
➢ Delete Boot Option		→← Select Screen ↑↓ Select Item Enter: Select +/- Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save ESC: Exit

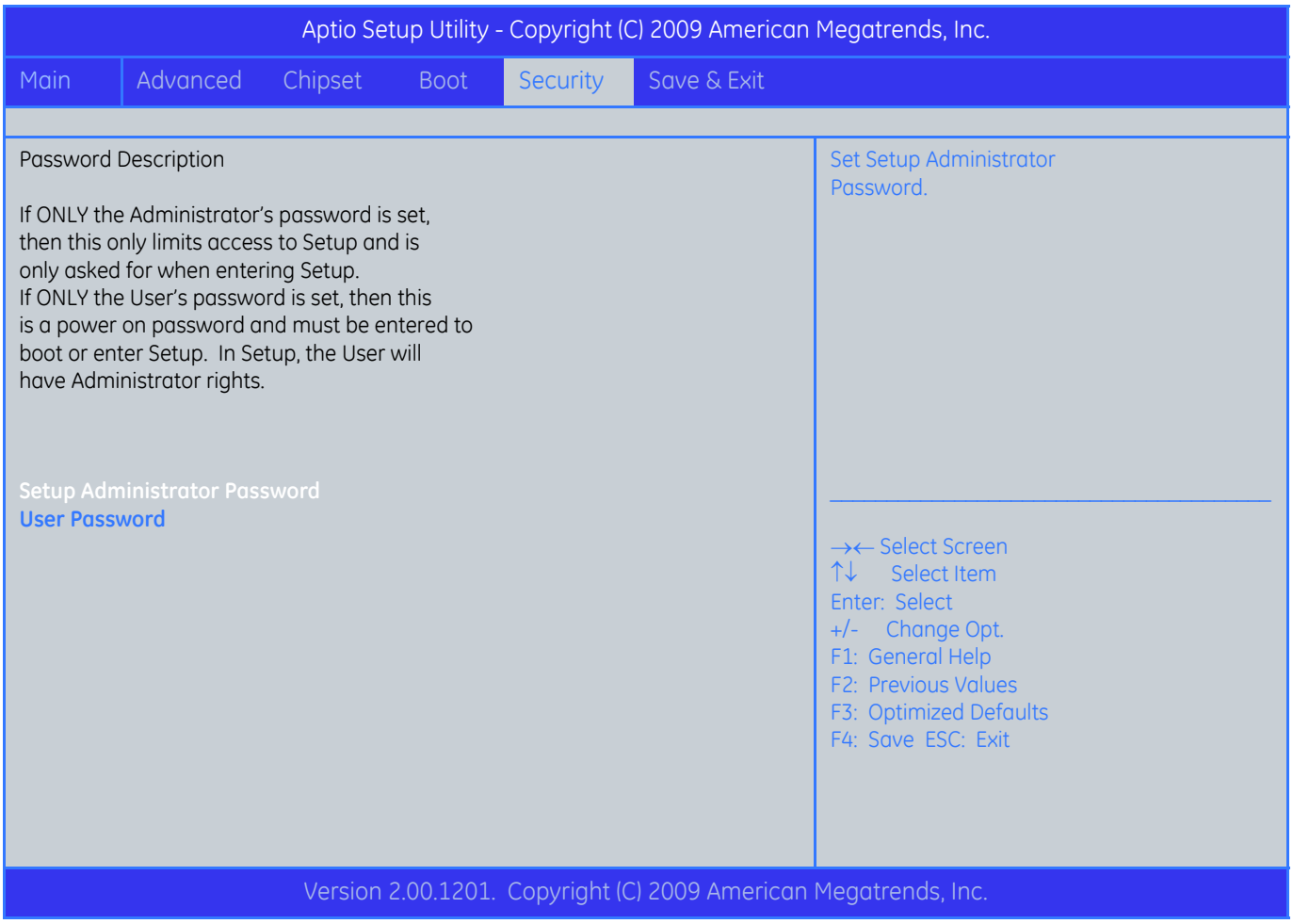
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

B.6 Security Setup Menu

The **Security** setup provides both a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when setup is executed, using either the Supervisor password or User password.

Table B-6 BIOS Security Menu



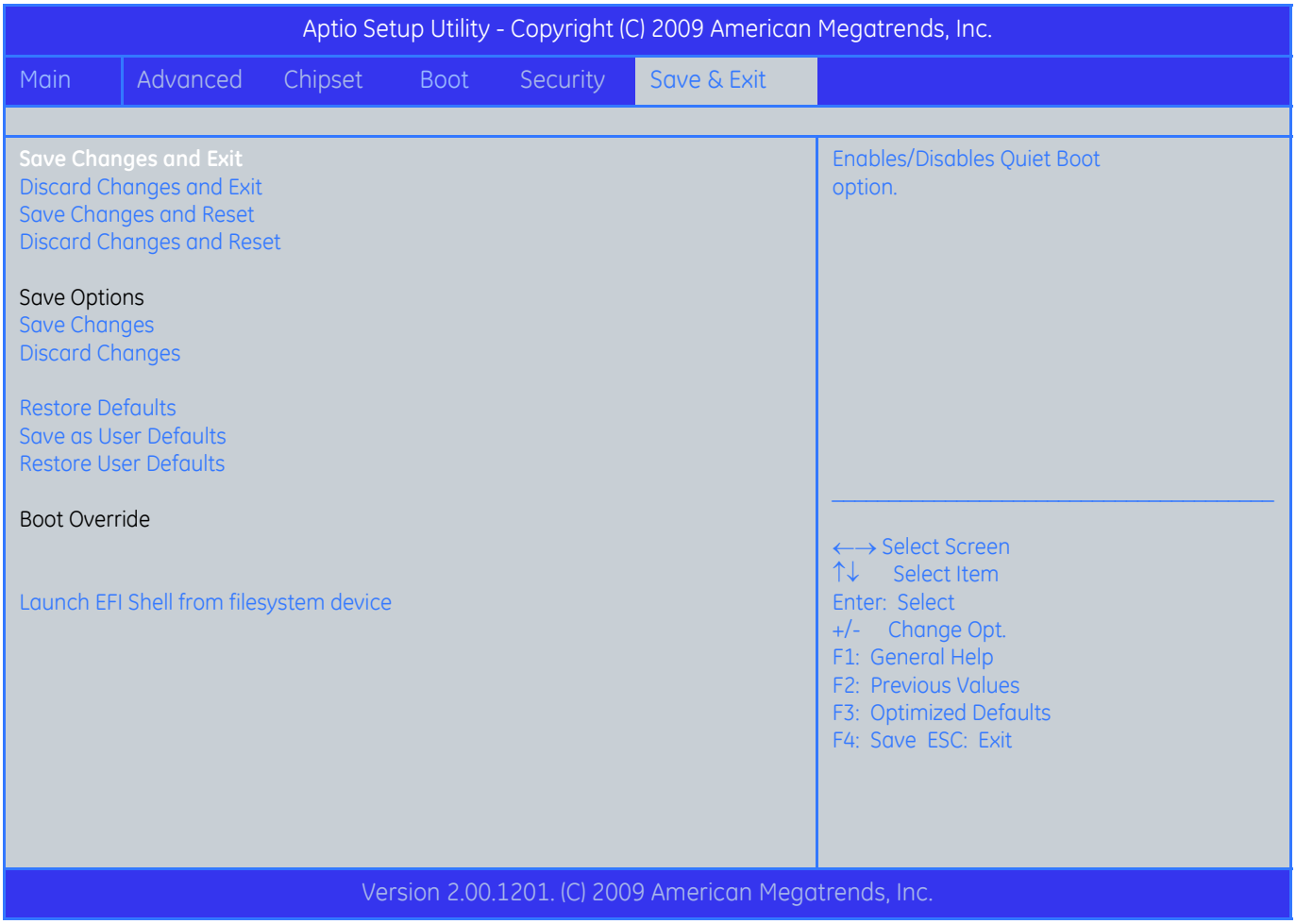
To reset the security in the case of a forgotten password, you must clear the NVRAM and reconfigure.

Refer to Section **1.4.3** ***Clear CMOS/RTC/Password*** on page 31 for instructions on clearing the CMOS.

B.7 Save & Exit Menu

Select the **Save & Exit** tab from the setup screen to enter the Save & Exit BIOS firmware, Setup screen. You can display a Save & Exit BIOS firmware, Setup option by highlighting it using the <Arrow> keys. The Save & Exit BIOS firmware, Setup screen is shown below.

Table B-7 BIOS Save & Exit Menu



If changes have previously been made in the BIOS firmware, and the system malfunctions, reboot the system and access this screen. Select 'Load Failsafe Defaults' and continue the reboot.

C • Appendix C: Specifications and Physical Description

The XVB601 assembly offers the ability of targeting multiple levels of environmental support. The following tables list Level 1 and Level 2 support:

C.1 Specifications

Table C-1 XVB601 Specifications Level 1

Cooling Method	Convection
Conformal Coating	Optional
Operational Temperature	0°C το 55°C (300 lfm)
Storage Temperature	-50°C to 100°C
Shock	20g peak sawtooth, 11 ms duration
Random Vibration	$0.002g^2$/Hz from 10-2000 Hz random and 2g sinusoidal from 5 - 100 Hz
Operational Humidity	Operating: Relative humidity 95% noncondensing without requiring IPC-830B conformal coating or underfill material.

Table C-2 XVB601 Specifications Level B

Cooling Method	Convection
Conformal Coating	Standard
Operational Temperature	-20°C το 55°C (300 lfm)
Storage Temperature	-50°C to 100°C
Shock	20g peak sawtooth, 11 ms duration
Random Vibration	$0.002g^2$/Hz from 10-2000 Hz random and 2g sinusoidal from 5 - 100 Hz
Operational Humidity	Operating: Relative humidity 95% noncondensing without requiring IPC-830B conformal coating or underfill material.

Table C-3 XVB601 Specifications Level 2

Cooling Method	Convection
Conformal Coating	Standard
Operational Temperature	-20°C το 65°C (300 lfm)
Storage Temperature	-50°C to 100°C
Shock	20g peak sawtooth, 11 ms duration
Random Vibration	$0.002g^2$/Hz from 10-2000 Hz random and 2g sinusoidal from 5 - 100 Hz
Operational Humidity	Operating: Relative humidity 95% noncondensing without requiring IPC-830B conformal coating or underfill material.

C.2 Heatsink and Conduction Plate Members

The heat sink or conduction cooled plate provided for the XVB601 are required to remove over 37W of heat from the Core i7 processor in addition to over 40W combined from the remainder of the board. The thermal relief solution is required to support the operating temperature ranges listed in **Table C-1** and **Table C-2** above, over silicon with Tjmax ratings of 100° C.

C.3 Reliability Requirements

- The XVB601 convection cooled assembly has a predicted MTBF rating that meets or exceeds 496 khours at 25C, GB using the MIL-217 parts-count method.
- The XVB601 assembly has obtained CE mark.
- The XVB601 is fully compliant with the European Union RoHS and WEEE directives.

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Additional Resources

For more information, please visit the GE Intelligent Platforms Embedded Systems web site at:

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