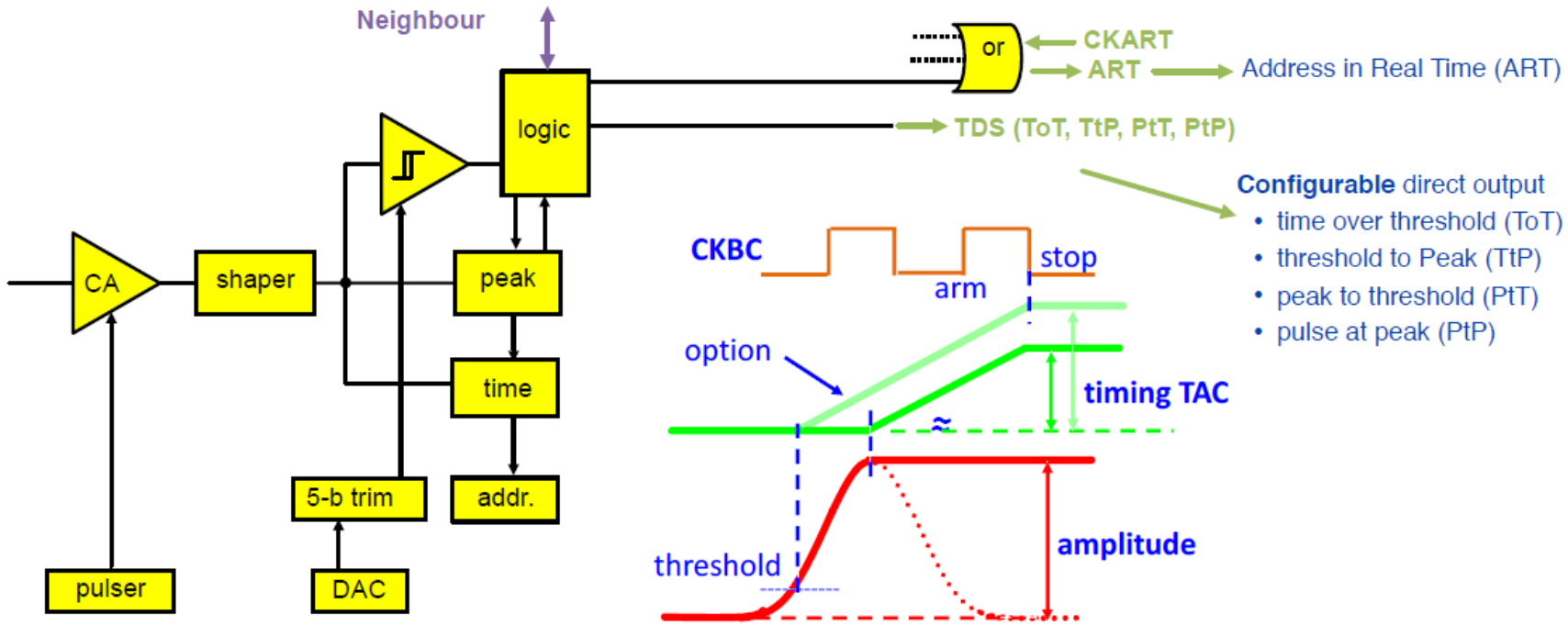
VMM3a **Discrimination, Charge and Time**



- Global 10-bit DAC for adjusting the **threshold** - **Discrimination** with sub-hysterisis (effective 2mV)
- Adjustable **5-bit discrimination** threshold **per channel** to adjust at ~mV level
- **Neighbour** logic to trigger sub-threshold channels with inter-chip communication
- Configurable **direct output** per channel and serial fast output of address as an OR of all channels
- **Peak detection**: measurement of peak **amplitude** and storage in analog memory
- **Time detection**: measurement of **peak/threshold** timing through a configurable time to amplitude converter (**TAC**: 60, 100, 350, 650 ns) and storage in analog memory
  - Clock working mode on **synchronous** machines but also as strobe for **asynchronous** operations

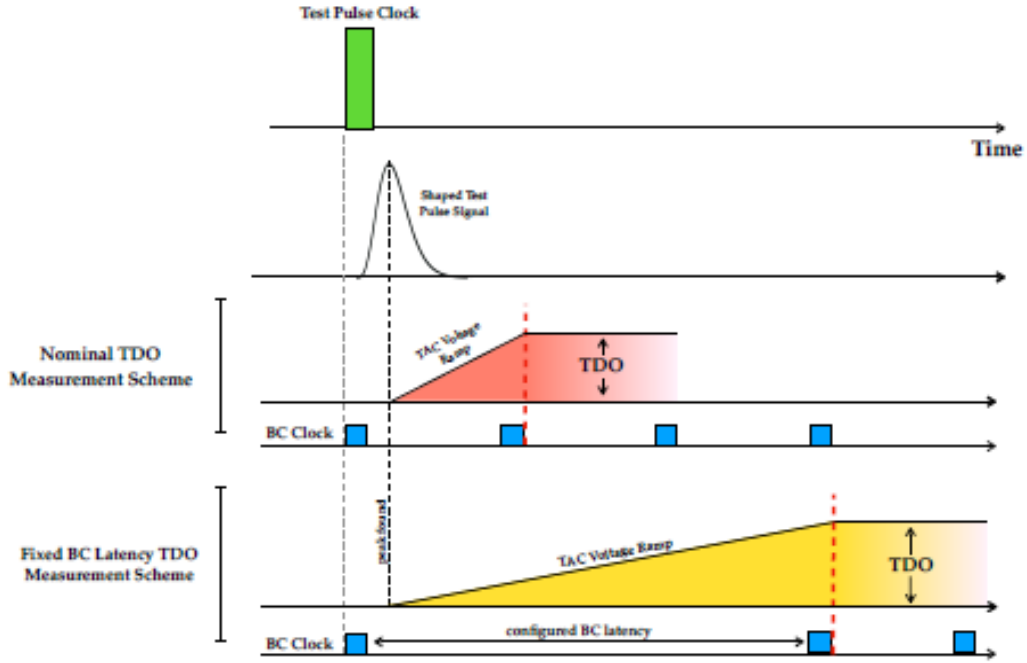


Figure 6.29: Illustration of the TDO measurement for an injected test pulse. The test pulse is injected following the test pulse clock (green), after which the subsequent shaped signal is formed. In the timing-at-peak scenario, once the peak-detector circuitry in the VMM fires, the TAC voltage ramp is initiated. In the nominal TDO measurement (red), the bunch crossing clock frequency remains unchanged and will be kept at its 40 MHz frequency in LHC conditions. In this configuration, the next falling edge of the bunch crossing clock after the TAC voltage ramp begins halts the ramp, and the TAC voltage is digitised as the TDO value. While in this mode, the TAC ramp is confined to times smaller than that given by the bunch crossing clock frequency (25 ns in the case of the LHC 40 MHz clock). In the fixed latency mode of acquiring the TDO measurement (yellow), the bunch crossing clock is halted for a configurable amount of time after which it is resumed and its next falling edge halts the TAC voltage ramp. In the fixed latency mode, the TAC can ramp to its maximal configured value (60, 100, 350, or 650 ns in the VMM3) if the configured BC latency is at least as large as this value.