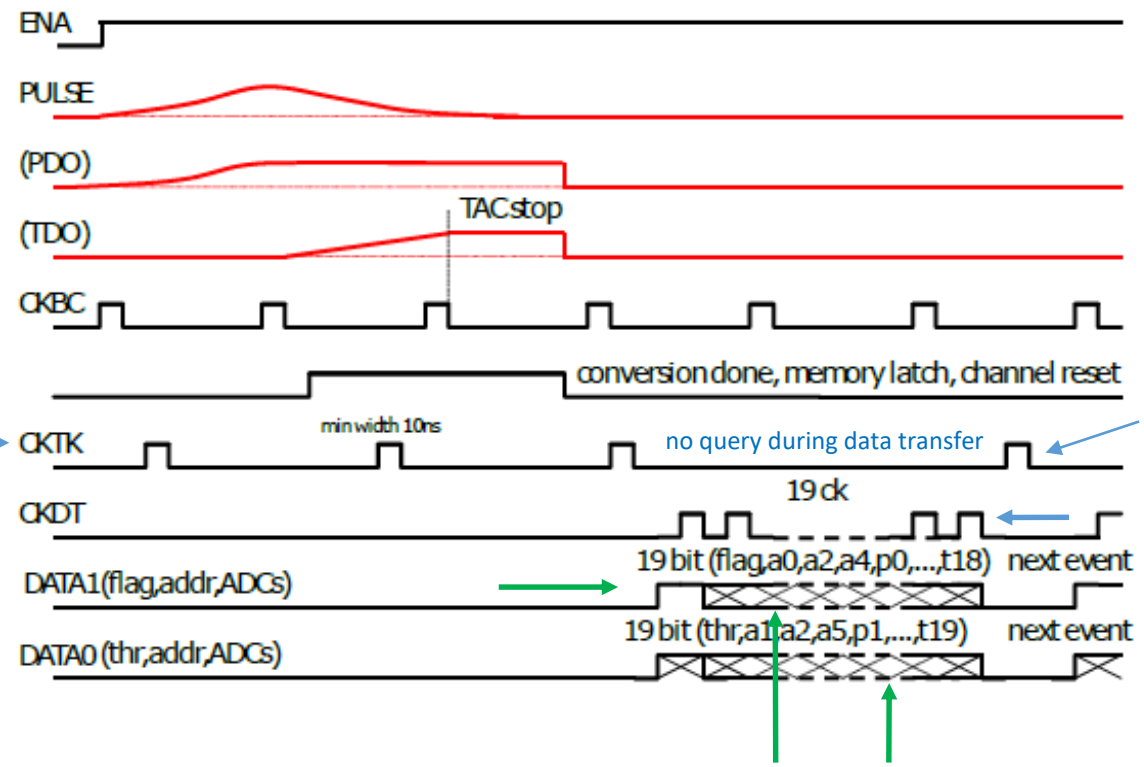
VMM Continuous Readout Mode (10 bit ADC)

(Reader = FPGA)

Reader enables acquisition



1 - Reader issues CKTK to query if data is available

2 - VMM asserts flag of DATA1 in response to query when data is available

transfers token to next channel with hit

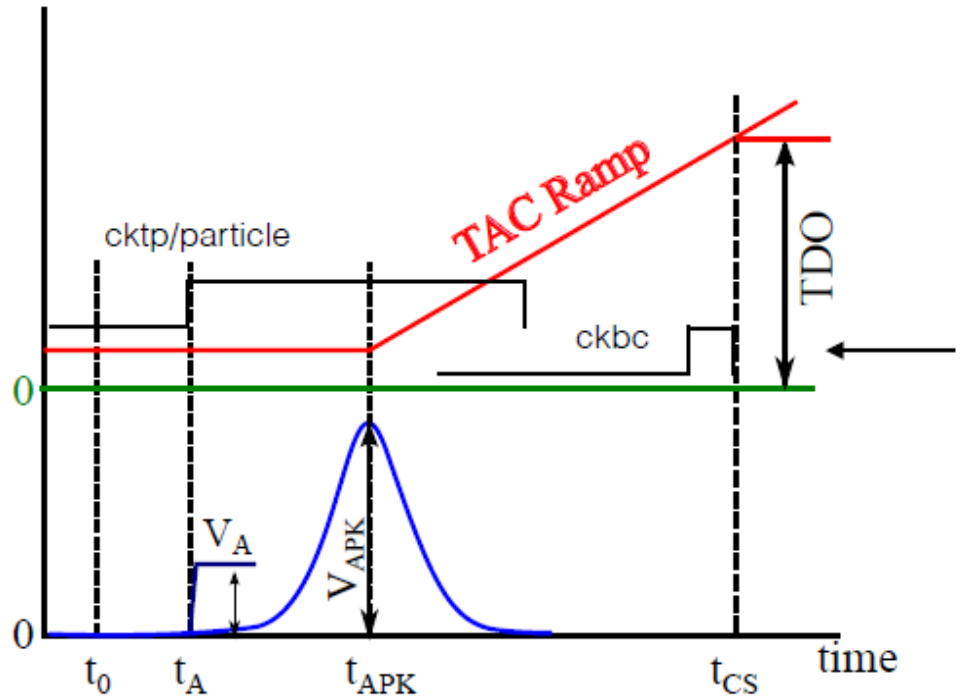
3 – Reader responds to asserted flag by issuing 19 clock burst on CKDT (160 MHz)

4 - VMM responds to CKDT burst by shifting out data bit pairs on DATA0 and DATA1 (38 bits total) (can be DDR)

Steps 1 - 4

Modes of operation - Continuous + ext trigger

- VMM design targets **synchronous** machines hence can be difficult to use in an environment like a **test beam where asynchronous operation** is needed but **precise timing** is needed to be measured (drift time)
- Most chips designed for synchronous machine **suffer from time jitter in such environment**
- On **VMM a mode was foreseen** to do such measurement where the **ckbc** can be used as a **strobe** and **not like a real clock**
- It can be **send as a trigger signal** with a **fixed latency** achieving precise time measurements



- Trigger signal from **external source**
- Can be combined with **register stcr** where **channel resets** if stop signal not occurs within the **TAC ramp**
- **Implies that trigger is propagated** within the TAC ramp up time (**60ns-650ns**)
- The **longer the TAC** though the **lower the resolution** on 8-bit information from the ADC
- Highly correlated trigger readout and noise subtraction