16-Channel Discriminator/Scaler VME Module
Revision B

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Overview

The 16-Channel Discriminator/Scaler Board contains 16 non-updating dual-threshold discriminators, programmable digital delays, and two 32-bit scalers per discriminator and threshold. The discriminator pulses are output as differential ECL logic levels through two front-panel headers. One group of outputs will connect to a TDC and the other group can be used as input to trigger logic. Both TDC and trigger output channels can individually be enabled/disabled with outputs widths and delays being user programmable. All programming is done through VME registers.

All discriminators and logic reside on a 6U standard VME mainboard. Each channel contains two analog receiver fast comparators (discriminator), and pulsers. Each discriminator channel has 2 programmable thresholds which can be programmed from VME. The output pulse width is also programmable from VME, but is common to the TDC and trigger discriminator channels separately. The digital delay circuit delays each discriminator pulse up to 512ns in 4ns steps (used for trigger output path and scaler input path when using external gate input). It is implemented with a high-speed (250MHz) FIFO for each discriminator channel. The delay is software selectable for the trigger output, trigger scaler input, and TDC scaler input.

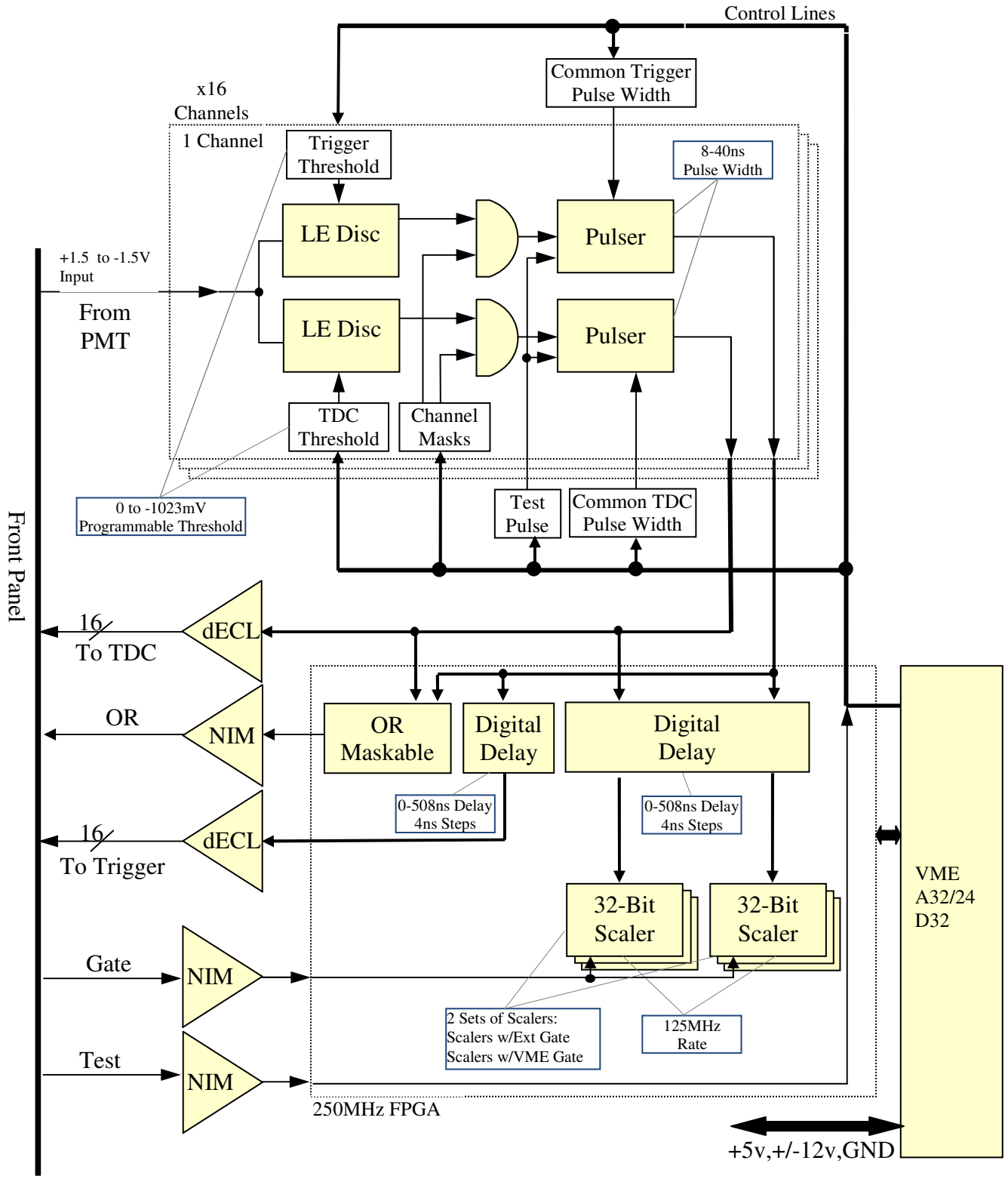
Each discriminator output pulse is recorded by a 32 bit counter (scaler) which can be gated with the external Gate (NIM) input. Scalers can be latched, read, and cleared through VME. There is a "OR" (NIM level) ouput that is the logical OR of all the unmasked discriminator outputs.

Discriminator outputs are provided as dECL levels on the front panel for interfacing with TDCs and trigger logic.

The VME interface is A32/A24/D32 with support for interrupts.

Discriminator/Scaler

Functional Block Diagram



Specifications

General	Spec
Power consumption	+/-12v, 500mA; +5v, 5.0A (30W typ.)
Fuses	+/-12v, 1.0A; +5v, 10.0A
Dimensions	6U VME, Single-wide; 160mm card depth
Front Panel I/O	Input Signals: 16 LEMO
	Gate Input: 1 LEMO
	Test Input: 1 LEMO
	Dual dECL Output: 2x34 Header
	OR Output: 1 LEMO
Onboard connectors	JTAG: 2x7pin 2mm Xilinx
LEDs	Green: VME Activity/Power
	Yellow: TDC Discriminator OR
	Red: TRG Discriminator OR
Analog Inputs	From PMT or coaxial detector signals
Channels	16
Signal Level	+/-1.5v, DC-coupled, clamped
Termination	50ohm
Gate,Test Inputs	Gates scalers, Pulses Discriminator Outputs (NIM)
OR Output	1 (NIM)
Discriminator Channels	
Dual threshold control	0 to -1023mV Threshold
	(for each TDC and TRG output)
Pulser	Non-updating
Pulser Width control	8ns to 40ns width +/-1ns accuracy
Pulser dead-time	~4ns w/8ns Pulse Width, ~10ns w/40ns Pulse Width
Maximum rate	80MHz w/8ns pulse setting
Channel-Channel Crosstalk	>65dB Isolation
Input Hysteresis	5mV
Input Noise band	<2mV RMS
Offset Error	<3mV max, <1mV typ.
dECL Outputs	
Channels	Dual 16 channel output
Connector	34pin header in LeCroy ECL format
1st group of 16 (TDC output)	Fast discriminator output
	Common width: 8 to 40ns
	Programmable mask register
2nd group of 16 (TRG output)	Common width 4 to 60ns
	Programmable mask register
Channel Threshold Control	10bit 1mV step (0 to -1023mV, +2048mV to -2047mV with firmware update)
Digital Delays	
Delay step size	4ns: Trigger Out, 8ns: Scaler Input VME controlled
Delay range	4ns: 0 to 508ns, 8ns: 0 to 1016ns
Uncertainty	4ns: Trigger Out, 8ns Scaler/Gate Input
Input/Gate timing alignment	Matched
Scalers	
Quantity	2 per threshold: 1 gated 1 free running

Width	32bit
Input source	Digital delay
Gating	External & free run scalers
Maximum Count rate	125MHz
Readout dead-time	None
Control	VME latch, read, clear, overflow

VME Interface

Protocols	A32/A24,D32
Address space	~2kbyte

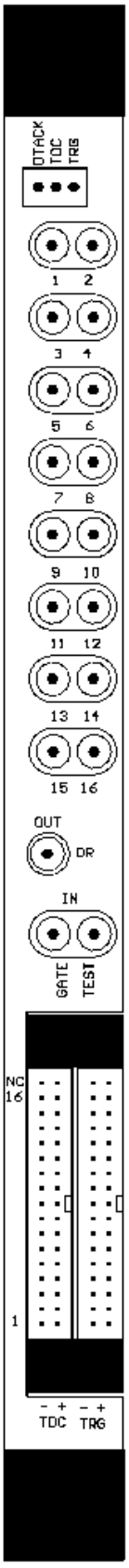
Misc

EEPROM	>1kbyte
Firmware Upgradable	Using VME

Delays

Input -> TDC Output	<6ns, <4.5ns typ.
Input-> TRG Output (min delay)	15ns

Front Panel



dECL Output Connector J1

(To TDC)

Pin	Function	Pin	Function
1	Ch 1 +	2	Ch 1 -
3	Ch 2 +	4	Ch 2 -
5	Ch 3 +	6	Ch 3 -
7	Ch 4 +	80	Ch 4 -
9	Ch 5 +	10	Ch 5 -
11	Ch 6 +	12	Ch 6 -
13	Ch 7 +	14	Ch 7 -
15	Ch 8 +	16	Ch 8 -
17	Ch 9 +	18	Ch 9 -
19	Ch 10 +	20	Ch 10 -
21	Ch 11 +	22	Ch 11 -
23	Ch 12 +	24	Ch 12 -
25	Ch 13 +	26	Ch 13 -
27	Ch 14 +	28	Ch 14 -
29	Ch 15 +	30	Ch 15 -
31	Ch 16 +	32	Ch 16 -
33	No Connect	34	No Connect

dECL Output Connector J2

(To Trigger Input)

Pin	Function	Pin	Function
1	Ch 1 +	2	Ch 1 -
3	Ch 2 +	4	Ch 2 -
5	Ch 3 +	6	Ch 3 -
7	Ch 4 +	80	Ch 4 -
9	Ch 5 +	10	Ch 5 -
11	Ch 6 +	12	Ch 6 -
13	Ch 7 +	14	Ch 7 -
15	Ch 8 +	16	Ch 8 -
17	Ch 9 +	18	Ch 9 -
19	Ch 10 +	20	Ch 10 -
21	Ch 11 +	22	Ch 11 -
23	Ch 12 +	24	Ch 12 -
25	Ch 13 +	26	Ch 13 -
27	Ch 14 +	28	Ch 14 -
29	Ch 15 +	30	Ch 15 -
31	Ch 16 +	32	Ch 16 -
33	No Connect	34	No Connect

VME Accessible Registers

All discriminator board registers can be accessed through the VME bus in the following modes:

- A24/A32 non-privileged/supervisory data access (AM Codes: 0x39, 0x3D, 0x09, 0x0D)
- 32bit aligned read or write access (register specific)

Future firmware release will enable support for 32/64bit block-level-transfers if needed.

Register Summary:

Register	Description:	Address Offset:
A_THRESHOLD_CH0	Threshold Control Ch0	0x0000
…	Threshold Control ChX	…
A_THRESHOLD_CH15	Threshold Control Ch15	0x003C
A_PULSEWIDTH	Pulse Width Control	0x0080
A_CH_ENABLE	Channel Control	0x0088
A_OR_MASK	OR Output Control	0x008C
A_DELAY	Input/Output Delays	0x0090
A_VME_LATCH	VME Scaler Latch	0x0098
A_LATCH	Gated Scaler Latch	0x009C
A_TRG_SCALER_CH0	Ext. Gate Trigger Scaler Ch0	0x0100
…	Ext. Gate Trigger Scaler ChX	…
A_TRG_SCALER_CH15	Ext. Gate Trigger Scaler Ch15	0x013C
A_TDC_SCALER_CH0	Ext. Gate TDC Scaler Ch0	0x0140
…	Ext. Gate TDC Scaler ChX	…
A_TDC_SCALER_CH15	Ext. Gate TDC Scaler Ch15	0x017C
A_TRG_VME_SCALER_CH0	VME Gate Trigger Scaler Ch0	0x0180
…	VME Gate Trigger Scaler ChX	…
A_TRG_VME_SCALER_CH15	VME Gate Trigger Scaler Ch15	0x01BC
A_TDC_VME_SCALER_CH0	VME Gate TDC Scaler Ch0	0x01C0
…	VME Gate TDC Scaler ChX	…
A_TDC_VME_SCALER_CH15	VME Gate TDC Scaler Ch15	0x01FC
A_REF_SCALER	VME Gate Ref Scaler	0x0200
A_REF_SCALER_GATE	Ext. Gate Ref Scaler	0x0204
A_FIRMWARE_REV	Firmware Revision	0x0400
A_BOARDID	Board Identifier	0x0404
A_CAL_ADDR_SET	Calibration Address Set	0x8000
A_CAL_ADDR_DATA	Read/Write Calibration Data	0x8004
A_FORCE_DAC_UPDATE	Force DAC Update	0x8008

Register: A_THREHOLD_CH0 -> A_THRESHOLD_CH15

Address Offset: 0x0000, 0x0004, …0x003C
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	TRG Threshold	
23	22	21	20	19	18	17	16
TRG Threshold							
15	14	13	12	11	10	9	8
-	-	-	-	-	-	TDC Threshold	
7	6	5	4	3	2	1	0
TDC Threshold							

TDC Threshold (R/W):
TDC CHx Threshold (in -1mV units)

TRG Threshold (R/W):
TRG CHx Threshold (in -1mV units)

Notes:
1) TRG threshold should be >25mV above TDC threshold (for same channel) to avoid introducing jitter onto timing sensitive TDC comparator

Register: A_PULSEWIDTH

Address Offset: 0x0080
Size: 32bits
Reset State: 0xF03F003F

31	30	29	28	27	26	25	24
TRG Output Pulse Width				-	-	-	-
23	22	21	20	19	18	17	16
-	-	TRG Pulser Width					
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	TDC Pulser Width					

TDC Pulser Width (R/W):
Controls pulser width (in units ns) for all TDC channels.
Will be calibrated from 8ns to 40ns (500ps accuracy). Values outside this range are not guaranteed to be calibrated.

TRG Pulser Width (R/W):
Controls pulser width (in units ns) for all TRG channels.
Will be calibrated from 8ns to 40ns (500ps accuracy). Values outside this range are not guaranteed to work.

TRG Output Pulse Width (R/W):
Digitally delayed/pulse stretched trigger output pulse width in 4ns counts.

Notes:
1) When TRG output delay (see corresponding register) is set to 0, the native TRG pulser width will appear on the TRG output as opposed to the digitally shaped pulse set be “TRG Output Pulse Width”

Register: A_CH_ENABLE

Address Offset: 0x0088
Size: 32bits
Reset State: 0xFFFFFFFF

31	30	29	28	27	26	25	24
TRG15EN	TRG14EN	TRG13EN	TRG12EN	TRG11EN	TRG10EN	TRG9EN	TRG8EN
23	22	21	20	19	18	17	16
TRG7EN	TRG6EN	TRG5EN	TRG4EN	TRG3EN	TRG2EN	TRG1EN	TRG0EN
15	14	13	12	11	10	9	8
TDC15EN	TDC14EN	TDC13EN	TDC12EN	TDC11EN	TDC10EN	TDC9EN	TDC8EN
7	6	5	4	3	2	1	0
TDC7EN	TDC6EN	TDC5EN	TDC4EN	TDC3EN	TDC2EN	TDC1EN	TDC0EN

TDCENx (R/W):
TDC Channel X: 1 = Enable, 0 = Disable

TRGENx (R/W):
Trigger Channel X: 1 = Enable, 0 = Disable

Register: A_OR_MASK

Address Offset: 0x008C
Size: 32bits
Reset State: 0x0000FFFF

31	30	29	28	27	26	25	24
TRG15EN	TRG14EN	TRG13EN	TRG12EN	TRG11EN	TRG10EN	TRG9EN	TRG8EN
23	22	21	20	19	18	17	16
TRG7EN	TRG6EN	TRG5EN	TRG4EN	TRG3EN	TRG2EN	TRG1EN	TRG0EN
15	14	13	12	11	10	9	8
TDC15EN	TDC14EN	TDC13EN	TDC12EN	TDC11EN	TDC10EN	TDC9EN	TDC8EN
7	6	5	4	3	2	1	0
TDC7EN	TDC6EN	TDC5EN	TDC4EN	TDC3EN	TDC2EN	TDC1EN	TDC0EN

TDCxEN (R/W):
TDC Channel X: 1 = Enable in front-panel OR output, 0 = Not used in OR

TRGENx (R/W):
Trigger Channel X: 1 = Enable in front-panel OR output, 0 = Not used in OR

Notes:

1) All TDC channels enabled in the above MASK are used to display the TDC front-panel LED
2) All TRG channels enabled in the above MASK are used to display the TRG front-panel LED

Register: A_DELAY

Address Offset: 0x0090
Size: 32bits
Reset State: 0x00080008

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	TRGOutputDelay						
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	ScalerDelay						

ScalerDelay (R/W):
Scaler Input Delay 0-127 count (in 8ns ticks)

TRGOutputDelay (R/W):
Trigger Output Delay 0-127 count (in 4ns ticks)

Notes:
1) See note in register A_PULSEWIDTH. When TRGOutputDelay = 0, the digital delay and pulse reshaping is bypassed providing a minimal delay output from the trigger channels using the TRG pulser width setting.

Register: A_VME_LATCH

Address Offset: 0x0098
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
VME_SCALER_LATCH							
23	22	21	20	19	18	17	16
VME_SCALER_LATCH							
15	14	13	12	11	10	9	8
VME_SCALER_LATCH							
7	6	5	4	3	2	1	0
VME_SCALER_LATCH							

VME_SCALER_LATCH(WO):
Write any value to latch VME scalers.

Notes:
1) After latching scalers for readout, hardware scalers will be reset.

Register: A_LATCH

Address Offset: 0x009C
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
GATED_SCALER_LATCH							
23	22	21	20	19	18	17	16
GATED_SCALER_LATCH							
15	14	13	12	11	10	9	8
GATED_SCALER_LATCH							
7	6	5	4	3	2	1	0
GATED_SCALER_LATCH							

GATED_SCALER_LATCH(WO):

Write any value to latch gated scalers.

Notes:

1) After latching scalers for readout, hardware scalers will be reset.

Register: A_TRG_SCALER_CH0 -> A_ TRG_SCALER _CH15

Address Offset: 0x0100, 0x0104, …0x013C
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
TRG SCALER							
23	22	21	20	19	18	17	16
TRG SCALER							
15	14	13	12	11	10	9	8
TRG SCALER							
7	6	5	4	3	2	1	0
TRG SCALER							

TRG SCALER(RO):

Latched trigger threshold scaler for CHx. 32bit value indicates an overflow when count is saturated (at 0xFFFFFFFF). Scaler is incremented on discriminator channel event and when external input gate = NIM logic 1.

Notes:

1) A scaler latch must be performed (by writing to register A_LATCH) to update these registers with current scaler counts

Register: A_TDC_SCALER_CH0 -> A_ TDC_SCALER _CH15

Address Offset: 0x0140, 0x0144, …0x017C
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
TDC SCALER							
23	22	21	20	19	18	17	16
TDC SCALER							
15	14	13	12	11	10	9	8
TDC SCALER							
7	6	5	4	3	2	1	0
TDC SCALER							

TDC SCALER(RO):

Latched TDC threshold scaler for CHx. 32bit value indicates an overflow when count is saturated (at 0xFFFFFFFF) . Scaler is incremented on discriminator channel event and when external input gate = NIM logic 1.

Notes:

1) A scaler latch must be performed (by writing to register A_LATCH) to update these registers with current scaler counts

Register: A_TRG_VME_SCALER_CH0 -> A_ TRG_ VME_SCALER _CH15

Address Offset: 0x0180, 0x0184, …0x01BC
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
TRG VME SCALER							
23	22	21	20	19	18	17	16
TRG VME SCALER							
15	14	13	12	11	10	9	8
TRG VME SCALER							
7	6	5	4	3	2	1	0
TRG VME SCALER							

TRG SCALER(RO):

Latched trigger threshold scaler for CHx. 32bit value indicates an overflow when count is saturated (at 0xFFFFFFFF). Scaler is incremented on discriminator channel event.

Notes:

1) A scaler latch must be performed (by writing to register A_VME_LATCH) to update these registers with current scaler counts

Register: A_TDC_VME_SCALER_CH0 -> A_ TDC_VME_SCALER _CH15

Address Offset: 0x01C0, 0x01C4, …0x01FC
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
TDC VME SCALER							
23	22	21	20	19	18	17	16
TDC VME SCALER							
15	14	13	12	11	10	9	8
TDC VME SCALER							
7	6	5	4	3	2	1	0
TDC VME SCALER							

TDC SCALER(RO):

Latched TDC threshold scaler for CHx. 32bit value indicates an overflow when count is saturated (at 0xFFFFFFFF) . Scaler is incremented on discriminator channel event.

Notes:

1) A scaler latch must be performed (by writing to register A_VME_LATCH) to update these registers with current scaler counts

Register: A_REF_SCALER

Address Offset: 0x0200
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
REF VME SCALER							
23	22	21	20	19	18	17	16
REF VME SCALER							
15	14	13	12	11	10	9	8
REF VME SCALER							
7	6	5	4	3	2	1	0
REF VME SCALER							

REF VME SCALER(RO):

Latched reference scaler for VME gated scalers. 32bit value indicates an overflow when count is saturated (at 0xFFFFFFFF). Scaler is incremented at board clock rate (125MHz) and provides an accurate measurement of elapsed time since last latch of VME gated scalers.

Notes:

1) A scaler latch must be performed (by writing to register A_VME_LATCH) to update these registers with current scaler counts

Register: A_REF_SCALER_GATE

Address Offset: 0x0204
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
REF GATE SCALER							
23	22	21	20	19	18	17	16
REF GATE SCALER							
15	14	13	12	11	10	9	8
REF GATE SCALER							
7	6	5	4	3	2	1	0
REF GATE SCALER							

REF GATE SCALER(RO):

Latched reference scaler for external gated scalers. 32bit value indicates an overflow when count is saturated (at 0xFFFFFFFF). Scaler is incremented at board clock rate (125MHz) and provides an accurate measurement of elapsed time since last latch of externally gated scalers.

Notes:

1) A scaler latch must be performed (by writing to register A_LATCH) to update these registers with current scaler counts

Register: A_FIRMWARE_REV

Address Offset: 0x0400
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
FIRMWARE_REV_MAJOR							
7	6	5	4	3	2	1	0
FIRMWARE_REV_MINOR							

FIRMWARE_REV_MAJOR(RO):

Major firmware revision

FIRMWARE_REV_MINOR(RO):

Minor firmware revision

Register: A_BOARDID

Address Offset: 0x0404
Size: 32bits
Reset State: 0x44534332

31	30	29	28	27	26	25	24
BOARD_ID							
23	22	21	20	19	18	17	16
BOARD_ID							
15	14	13	12	11	10	9	8
BOARD_ID							
7	6	5	4	3	2	1	0
BOARD_ID							

BOARD_ID(RO):

0x44534332 = "DSC2" in ASCII

Register: A_CAL_ADDR_SET

Address Offset: 0x8000
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	CAL_ADDR			
7	6	5	4	3	2	1	0
CAL_ADDR							

CAL_ADDR(WO):

12bit Calibration Address. Set to calibration table address before reading or writing calibration table (done accessing A_CAL_ADDR_DATA register). Only should be used for calibration processes.

Register: A_CAL_ADDR_DATA

Address Offset: 0x8004
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	CAL_DATA			
7	6	5	4	3	2	1	0
CAL_DATA							

CAL_DATA(R/W):

12bit Calibration Data. Set to calibration table address before reading or writing calibration table (done accessing A_CAL_ADDR_SET register). Only should be used for calibration processes.

Register: A_FORCE_DAC_UPDATE

Address Offset: 0x8008

Size: 32bits

31	30	29	28	27	26	25	24
FORCE_DAC_UPDATE							
23	22	21	20	19	18	17	16
FORCE_DAC_UPDATE							
15	14	13	12	11	10	9	8
FORCE_DAC_UPDATE							
7	6	5	4	3	2	1	0
FORCE_DAC_UPDATE							

FORCE_DAC_UPDATE(WO):

Write any value to this register to force updates to all threshold and pulse width DACs based on updated calibration table RAM. Only should be used for calibration processes.