SAMPA_V5 Data Sheet

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Contents

1. Overview

1.1. Documentation Overview

This document offers a brief summary of the SAMPA_V5 ASIC, a new prototype specially designed for read-out of low amplification GEM-based detectors. The SAMPA_V5 is a modified version of SAMPA_V4, with new faster peaking time configurations.

1.2. Device Description

The SAMPA_V5 prototype is a front-end ASIC implemented in a commercial 130nm CMOS process from TSMC, with 1.25V nominal voltage supply. It integrates 32 channels per chip that concurrently digitize and process the input signals. SAMPA_V5 contains negative and positive polarity front-end, which transforms the charge signal into a differential semi-Gaussian voltage signal that is then digitized by a 10-bit 18.5 MSamples/s full differential ADC. After the ADC a digital signal processor eliminates signal perturbations, distortion of the pulse shape, offset and signal variation due to temperature variations. The data read-out takes place continuously at a speed of up to 3.52 Gbps by eleven 320 Mb/s e-links.

The functional block diagram for the SAMPA_V5 ASIC is shown in Figure 1.

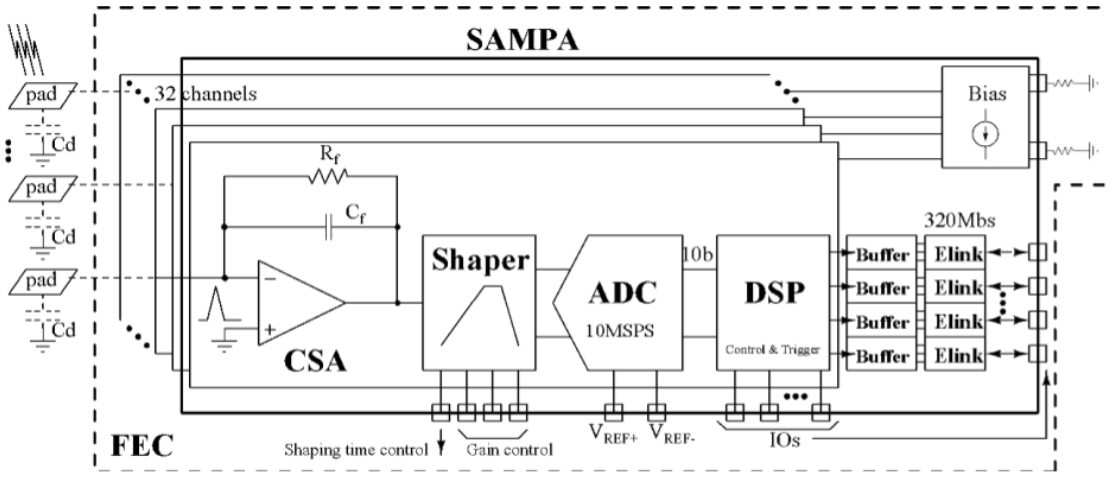


Figure 1: ***Block diagram for the SAMPA chip.***

1.2.1. Analog front-end

The front-end block is composed of a Charge Sensitive Amplifier (CSA), which accept both positive and negative charge, followed by two shapers. The CSA has a capacitive feedback C_f and a resistive feedback R_f connected in parallel, a Pole-Zero Cancellation (PZC) network, a high pass filter, two bridged-T second order low pass filters, a non-inverting stage, as shown in Figure 2.

The first shaper is a scaled-down version of the CSA and generates the two first poles and one zero. A copy of the first shaper connected in unity gain configuration is implemented in order to provide a differential mode input to the next stage.

The second stage of the shaper is a fully differential second order bridged-T filter and it includes a Common-Mode Feed-Back network (CMFB). The non-inverting stage adapts the DC voltage level of the shaper output to use the full dynamic range of the ADC. It consists of a parallel connection of two equally designed Miller compensated amplifier.

The SAMPA V5 front-end circuit is a modified version of the one from SAMPA V4, with new configurations of reduced peaking time. The CSA feedback array was modified to allow a faster peaking time of 80ns at the expense of the configuration with 300ns of peaking time and 4mV/fC gain, which is not available anymore.

With these modifications, SAMPA_V5 supports two new configurations, which combines the sensitivity gain of 20 mV/fC or 30 mV/fC with a new, faster peaking time of 80ns. The 160ns peaking time and 20 mV/fC or 30 mV/fC sensitivity configurations were maintained equivalent to the respective configurations of SAMPA_V4. The performance of SAMPA_V5 front-end is summarized in the Performance Section.

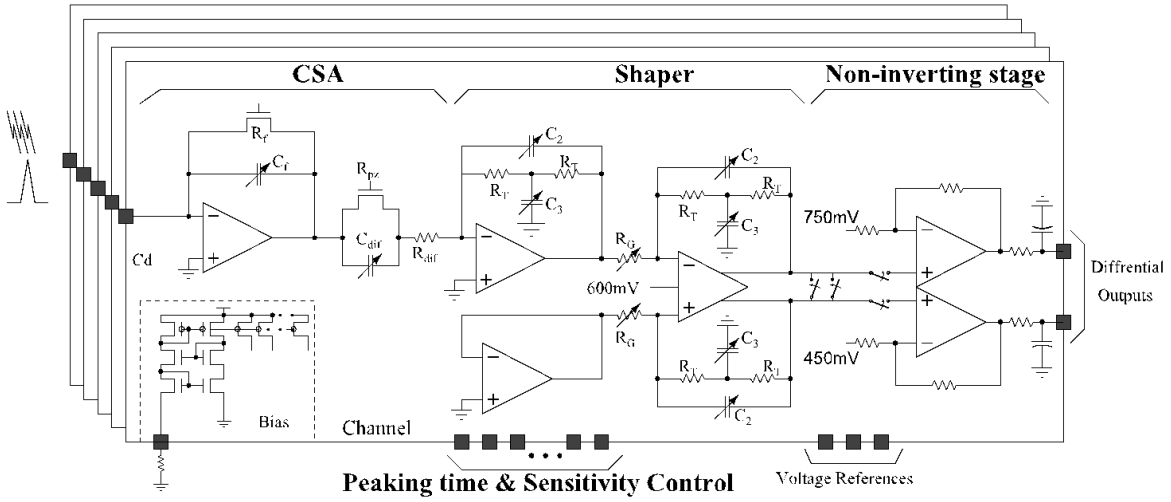


Figure 2: Block diagram of the analog front-end.

The analog front-end can be configured to operate at two shaping time settings controlled by the CTS pin, two sensitivity settings controlled by the CG[1:0] pins and positive/negative input charge polarity controlled by the POL pin. Table 1 summarizes the possible configurations.

Table 1: Analog Front-end Configurations

Polarity	POL
Positive	low
Negative	high

(a) Pulse polarity configuration

Gain	Shaping time	CTS	CG0	CG1
30 mV/fC	160 ns	high	high	high
20 mV/fC	160 ns	high	low	high
30 mV/fC	80 ns	low	low	high
20 mV/fC	80 ns	low	low	low

(b) Gain and shaping time configuration

1.2.2.Analog to digital converter

The ADC is based on a split capacitor fully differential successive approximation (SAR) topology. The SAR topology allows for low power with reasonable sample rates and resolution. The ADC has a resolution of 10-bit and a sample rate up to 20 MSamples/s. The block diagram of the ADC is shown in Figure 3. The main parts of the circuit are: capacitive array, switches, comparator and the SAR control logic. The capacitor array is used to perform sample & hold and the digital to analog converter functions. And Figure 4 shows the time diagram for the ADC.

The ADC circuit was slightly modified when compared to SAMPA_V4 ASIC, providing an improved bootstrap sampling circuitry. With this modification, the ADC v5 was fabricated in an MPW (Multi-Project-Wafer) run and the measurement results showed an ENOB of 9.5 bits, as illustrated in Figure 5. The static performance of the ADC, measured by its DNL and INL with the testchip, also were improved and are shown in figures 6 and 7.

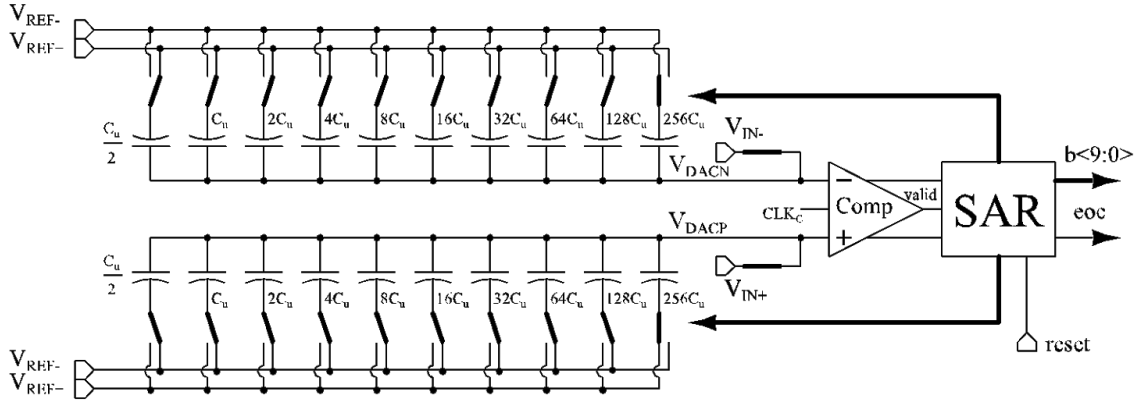


Figure 3: Block diagram of the ADC.

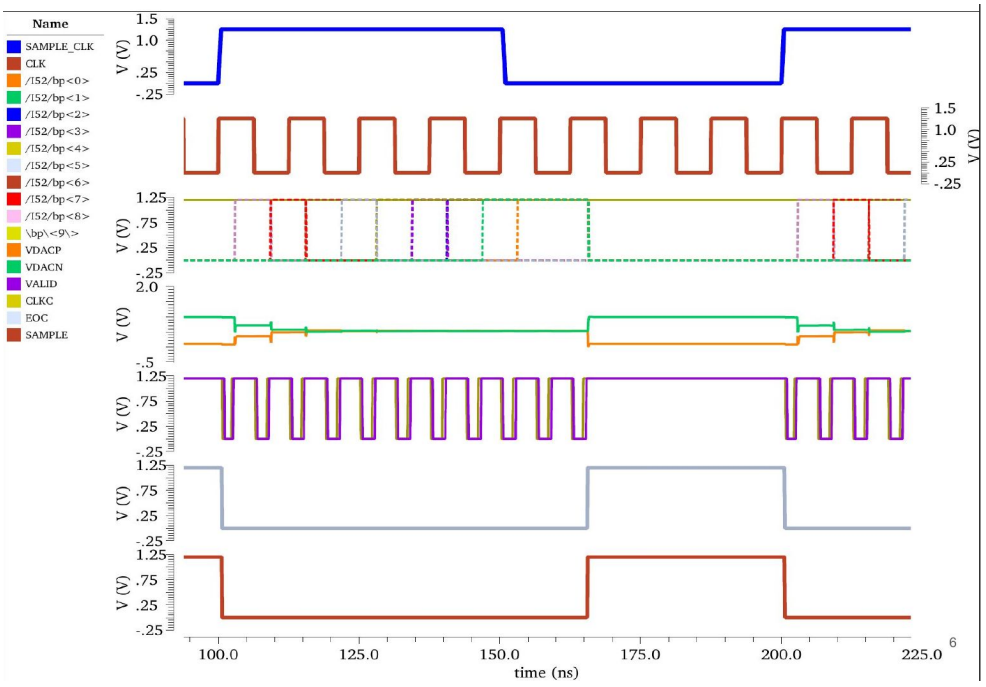


Figure 4. ADC Time diagram.

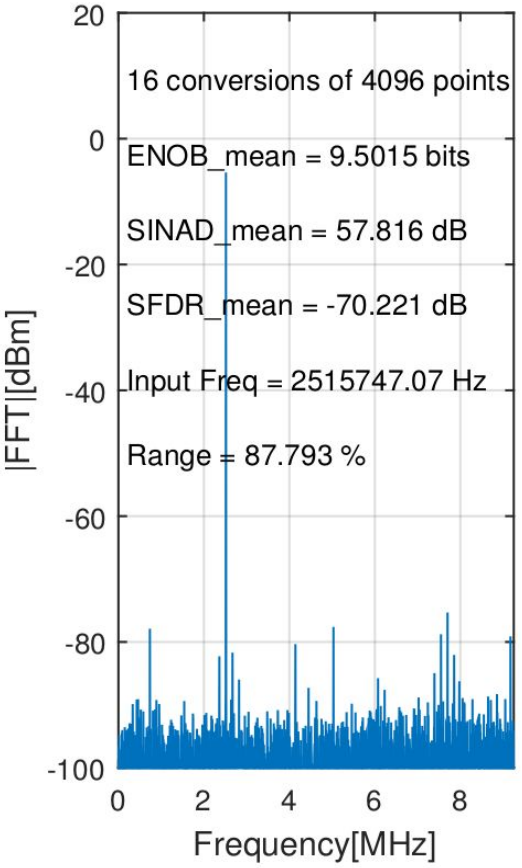


Figure 5. ADC v5 testchip measured @ 18.5MSPS, 4096 samples, input frequency of 2,515,747.075 Hz, 90% input range- ENOB of 9.5 bits.

The ADC shows a low code spreading and no missing codes, as can be seen in Figure 6. Figure 6 shows the results of DNL measurements of one of the ADC v5 testchips. DNL is below 0.8 LSB, which is a result of no missing codes events and low spread between even and odd codes quantity. The INL, shown in Figure 7, is below 0.6 LSB and there is no third order distortion evidence.

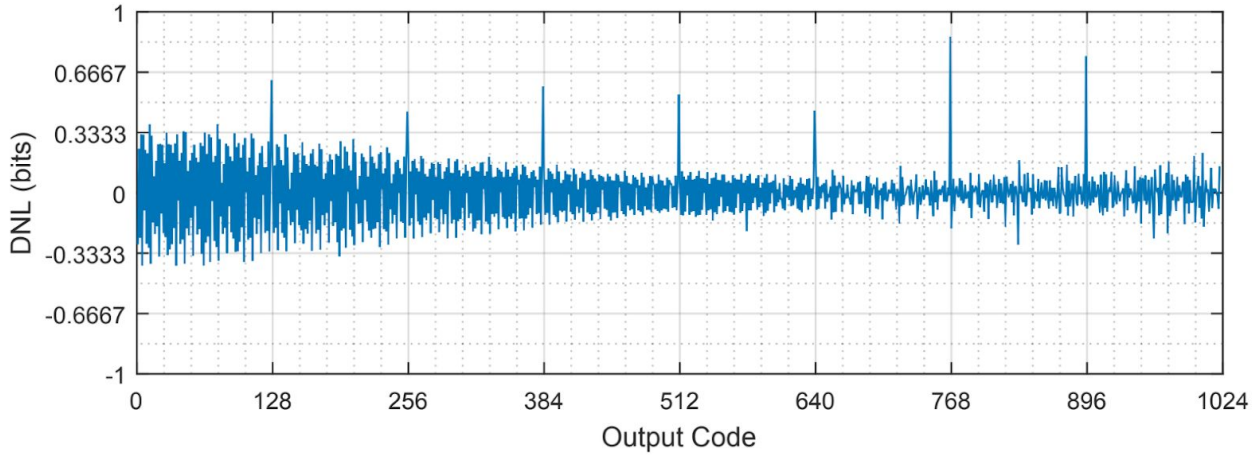


Figure 6. ADC v5 testchip measured DNL. DNL < 0.8 LSB.

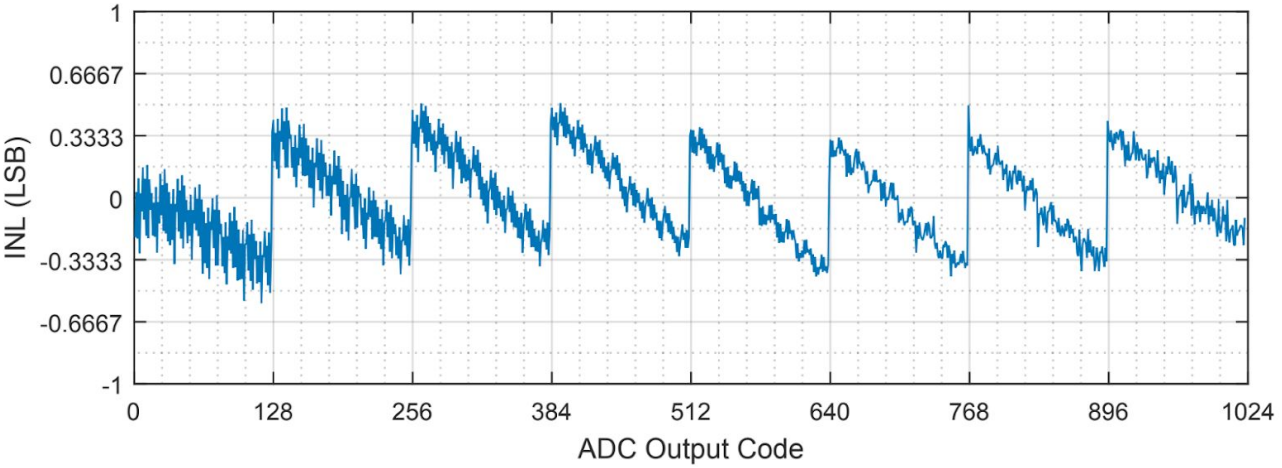


Figure 7. ADC v5 testchip measured INL. INL < 0.6 LSB.

1.2.3.Digital Signal Processing

The Digital Signal Processing (DSP) part is composed by digital filters, a data format unit, a ring buffer, a trigger manager block, a configuration register bank, a control state machine, and eleven 320 Mb/s e-links.

The data read-out takes place continuously at a speed of up to 3.52 Gbps by eleven 320 Mb/s serialization links (e-links). The data read-out can be performed in continuous mode or in triggered mode. In continuous mode the read-out of a programmable number of samples is performed

trigger-less if the input signal exceeds the programmable threshold value. Software triggers are accepted in continuous mode for calibration and synchronization purposes.

In triggered mode, the data read-out of programmable number of samples is performed only upon reception of an external trigger with a maximum latency of 9.6 μs. Triggers arriving during an active readout will be accepted. In that case the active readout will be extended by the new arriving trigger for the programmable number of samples and status information is sent to acknowledge the read-out extension. Optionally a programmable number of presamples from 0 to 3 and up to 7 postsamples can be recorded around the samples where input signal crossed the thresholds.

Digital signal conditioning

The objective of the Digital Signal Condition (DSC) is to increase the efficiency of the data compression algorithms (e. g. zero suppression). The DSC implements, in several subsequent stages (pipeline), different algorithms to condition and shape the signal. The DSC comprises four main building blocks

Baseline Correction I (BCI)

It is the first stage of the data processor. Its main task is to remove the low frequency perturbations and systematic effects. This filter has different modes of operation depending on the application.

Digital Shaper (DS)

DS can be used for two different applications; tail cancellation or peaking time correction. A fourth order IIR filter is implemented. The choice of the filter parameters configure the system for one of the applications:

- Tail cancellation: an accurate cancellation of the signal tail is required in order to perform the zero suppression efficiently. Since the filter coefficients for each channel are fully programmable and reconfigurable, the circuit is able to cancel a wide range of signal tail shapes.
- Peaking time correction: modification of the peaking time according to the application

Baseline Correction II (BCII)

This unit applies a baseline correction based on a moving average filter. This scheme removes non-systematic perturbations of the baseline that are superimposed to the signal. At the output of this block, the signal baseline is constant with an accuracy of 1 Least Significant Bit (LSB).

Baseline Correction III (BCIII)

This unit applies a baseline correction through a slope based filter. It is provided as an alternative to the BCII filter as the BCII filter can potentially get stuck outside its thresholds in cases of very large perturbations.

The digital word length can be changed only in steps of 1 bit, the addition of 1 bit to the data-path reduces the size of quantification error analysis by a factor of 2. Table 3 shows the calculated signal to noise ratio of the system. Following a commitment between system accuracy and hardware complexity, two extra bits (LBS) in the data path are added.

In Sampa V5 all memories used are Dual Port Memory. Dual Port Memories allow to read and write different cells simultaneously and seem to be more robust regarded to Single-Event-Latchup. For instance, the pre-trigger samples delay module uses a 10 x 192 bit dual port memory to provide a programmable delay chain for the samples to compensate for any delay in the trigger signal.

Table 3: Signal to noise ratio of the filter

Resolution	NR
ADC (10 bits)	66.22 dB
ADC (10 bits) + Shaper (10bits)	53.99 dB
ADC (10 bits) + Shaper (11bits)	59.30 dB
ADC (10 bits) + Shaper (12bits)	63.25 dB
ADC (10 bits) + Shaper (13bits)	65.27dB

1.3. Configurable Reference Voltage Source

The Configurable Reference Voltage Source provides 3 output voltage tap values: 750mV, 600mV and 450 mV, which works with less than 3% variation on a temperature range between -20°C and 70°C and a power supply range 1.05V and 1.35V.

The circuit topology is based on the one proposed by Banba and others [Huang et al.,2006], as shown in Figure 9 below. Additional resistors are used in the M3 current branch to provide two additional voltages. To allow for trimming, the resistor connected to ground is adjustable with 3 NMOS transistors.

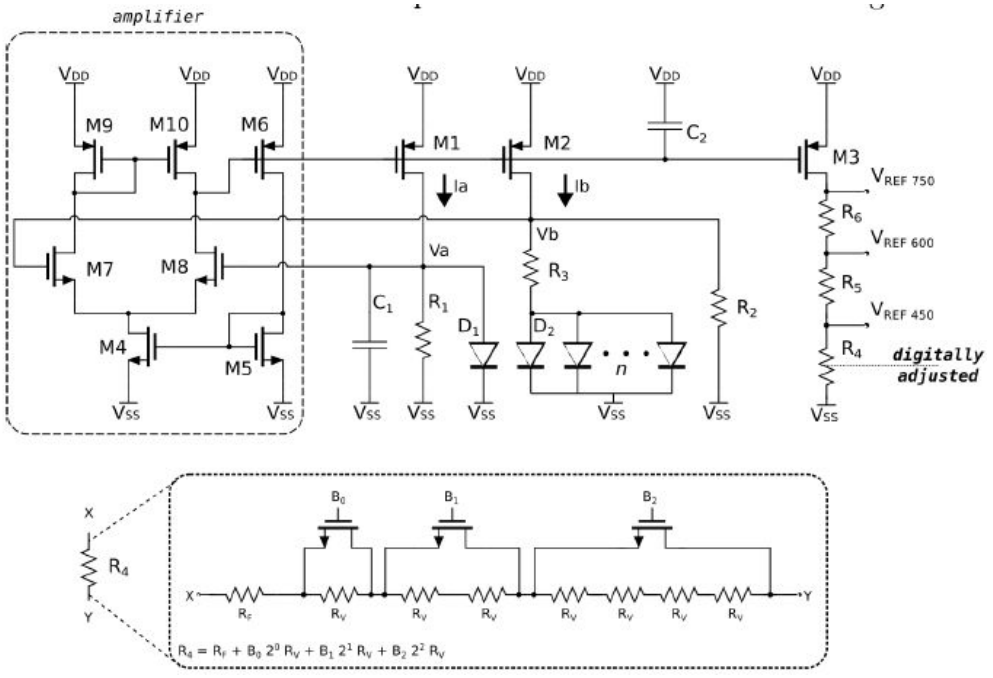


Figure 9. Voltage Reference schematic.

The main reference voltages are named according to its nominal expected values respectively 450 mV, 600 mV, 750 mV, for the signals *V*450, *V*600 and *V*750. The Monte Carlo simulation results are described in table 4.

Table 4: Monte Carlo Simulation Result for the Reference Voltage Source circuit.

Characteristics	Min	Max	Mean	Sigma	Unit
Line Regulation	245.8u	465.5u	346u	35.35u	V/V
PSSR	180.8	183.3	182.1	390.3m	dB
TC	7.364	21.86	13.37	2.721	ppm
Vref_750mV	741.1m	764.2m	752.2m	3.923m	V
Vref_600mV	592.9m	611.6m	601.8m	3.142m	V
Vref_450mV	449m	458.9m	451.5m	2.363m	V

The reference voltage source is configured using three I2C configurable bits available on the global register unit. The expected levels for each possible configuration are shown on the table 5. The voltages can be adjusted in steps of about 25mV, allowing to compensate for the effect of process variation.

Table 5: Simulated results for the Bandgap output voltage, for 1.25V of VDD and 40ºC temperature.

Setting	Bit 2	Bit 1	Bit 0	V600 [mV]	V750 [mV]	V450 [mV]
0	0	0	0	698.4	847.7	549.1
1	0	0	1	674.0	823.4	524.6
2	0	1	0	649.1	798.6	499.6
3	0	1	1	624.5	774.1	474.9
4	**1**	**0**	**0**	**599.3**	**749.0**	**449.6**
5	1	0	1	574.5	724.3	424.7
6	1	1	0	549.5	699.3	399.6
7	1	1	1	524.7	674.6	374.7

1.4. Performance Specification

Tables 6, 7, 8 and 9 below summarize the post layout simulations for the four different gain and peaking time configurations of the SAMPA_V5: 20N160 (20mV/fC gain, 160ns peaking time and negative input polarity), 30N160 (30 mV/fC gain, 160ns peaking time and negative input polarity) 20N80 (20mV/fC gain, 80ns peaking time and negative input polarity) and 30N810 (30mV/fC gain, 80ns peaking time and negative input polarity).

The simulation was performed including layout extracted parasitics and considering an input charge of 50fC (Qin=50fC), a detector capacitance of 18.5pF (Cd =18.5pF) and corners of process variations and temperature sweep from 0 to 80 degrees Celsius.

SAMPA_V5 has an increased input rate and an improved pileup performance. The pileup simulations were performed by applying at input of the Charge Amplifier (CSA) a series of charges (voltage step over a 1pF injection capacitor) simulating a stream of charge injections using nominal corner to find the saturation point.

Table 6: Post layout simulations for SAMPA_V5 circuit, considering 20 mV/fC and 160 ns configuration and the worst case for process and temperature variation.

	20N160 (SAMPA V5)		
	Min	Typ (40 °C)	Max
I_{REF}<1:32> (bias 01)	191.2 uA (SLOW_0)	260.4 uA	357.4 uA (FAST_80C)
V_{BC} (bias 01)	661.3 mV(FSSF_80C)	776.8 mV	897.6 mV (SFFS_0C)
Sensitivity	15.76 mV/fC (SFFS_80C)	20.23 mV/fC	22.71 mV/fC (FSSF_40C)
Peaking Time	100 ns (FAST_80C)	149.6 ns	200 ns (SLOW_0C)
IREFS<1:32> (bias 02)	34.01 uA (SLOW_0C)	58.32 uA	109.7 uA (SFFS_80C)
ENC* @ Cd=25pF	454.9 e- (SLOW_0C)	541.4 e-	613.5 e- (FAST_80C)

*These ENC values only consider Analog Front-End noise and not ADC quantization noise.

Table 7: Post layout simulations for SAMPA_V5 circuit, considering 30 mV/fC and 160 ns configuration and the worst case for process and temperature variation.

	30N160 (SAMPA V5)		
	Min	Typ (40 °C)	Max
I_{REF}<1:32> (bias 01)	191.2 uA (SLOW_0)	260.4 uA	357.4 uA (FAST_80C)
V_{BC} (bias 01)	661.3 mV (FSSF_80C)	776.8 mV	897.6 mV (SFFS_0C)
Sensitivity	24 mV/fC (SFFS_80C)	30.77 mV/fC	34.21 mV/fC(FSSF_40C)
Peaking Time	109.1 ns (FAST_40C)	149.6 ns	200 ns (SLOW_0C)
IREFS<1:32> (bias 02)	34.01 uA (SLOW_0C)	58.32 uA	109.7 uA (SFFS_80C)
ENC * @ Cd=25pF	440.7 e- (SLOW_0C)	528.1 e-	613.5 e- (FAST_80C)

*These ENC values only consider Analog Front-End noise and not ADC quantization noise.

Table 8: Post layout simulations for SAMPA_V5 circuit, considering 20 mV/fC and 80 ns configuration and the worst case for process and temperature variation.

	20N80 (SAMPA V5)		
	Min	Typ (40 °C)	Max
I_{REF}<1:32> (bias 01)	191.2 uA (SLOW_0)	260.4 uA	357.4 uA (FAST_80C)
V_{BC} (bias 01)	661.3 mV (FSSF_80C)	776.8 mV	897.6 mV (SFFS_0C)
Sensitivity	16.01 mV/fC (SFFS_80C)	20.64 mV/fC	22.9 mV/fC (FSSF_0C)
Peaking Time	63.36 ns (FAST_0C)	88.55 ns	110.7 ns (SLOW_0C)
IREFS<1:32> (bias 02)	34.01 uA (SLOW_0C)	58.32 uA	109.7 uA (SFFS_80C)
ENC * @ Cd=25pF	491 e- (SLOW_0C)	621.1 e-	748.9 e- (FAST_80C)

*These ENC values only consider Analog Front-End noise and not ADC quantization noise.

Table 9: Post layout simulations for SAMPA V5 circuit, considering 30 mV/fC and 80 ns configuration and the worst case for process and temperature variation.

	30N80 (SAMPA V5)		
	Min	Typ (40 °C)	Max
I_{REF}<1:32> (bias 01)	191.2 uA (SLOW_0)	260.4 uA	357.4 uA (FAST_80C)
V_{BC} (bias 01)	661.3 mV (FSSF_80C)	776.8 mV	897.6 mV (SFFS_0C)
Sensitivity	24.25 mV/fC (SFFS_80C)	31.02 mV/fC	34.18 mV/fC (FSSF_0C)
Peaking Time	60.5 ns (FAST_80C)	86.05 ns	114.9 ns (SLOW_0C)
IREFS<1:32> (bias 02)	34.01 uA (SLOW_0C)	58.32 uA	109.7 uA (SFFS_80C)
ENC * @ Cd=25pF	475 e- (SLOW_0C)	602 e-	742 e- (FAST_80C)

*These ENC values only consider Analog Front-End noise and not ADC quantization noise.

As conclusion of those simulations, for 5 fC continuous charge stream with a final 90 fC pulse after 256 pulses, 400ns of pulse spacing caused agglutination of semi-gaussian pulses but no saturation was observed in SAMPA V5. Considering a 10 fC continuous charge stream and a final 90 fC pulse after 256 pulses, no saturation was observed but the results show a small gain variations due to baseline variations, especially after the 90 fC charge peak.

For 100 charge injections with 50 fC peak it was observed saturation in 2 stages: (a) strong saturation in 45 nA which implies a continuous degradation of sensitivity and (b) weak saturation in 33 nA and 40 nA with small sensitivity degradation at the beginning until a steady state is reached, after that the sensitivity is stable. These simulations were performed for typical extraction at typical process corner and 40 degrees Celsius.

Furthermore, a testchip of the new front-end V5 was fabricated and measured. The obtained results from the tests are shown in table 10.

Table 10: Measurements results obtained for the Front End v5 Testchip.

Front-End Testchip Summarized Measurements									
	Gain [mV/fC]			**Time to Peak [ns]**			**ENC* [e-] @ Cd=18.5pF**		
Config.	min	avg	max	min	avg	max	min	avg	max
30N160	26.8	28.9	31.3	146	150	154	517	535	549
20N160	17.5	18.8	20.4	142	145	149	522	533	547
30N80	25.1	28.8	32.7	79	81	83	536	556	568
20N80	16.5	18.8	20.9	78	80	81	549	565	581

*These ENC values only consider Analog Front-End noise and not ADC quantization noise.

2. Pad Definitions

2.1 Die physical dimensions

SAMPA V5 occupies an area of 9.534 mm x 8.944 mm ASIC with 32 input channels implemented in a commercial 130 nm CMOS process. The full layout is displayed in Figure 10. Its main physical characteristics are described below.

Die size:	9534μm x 8944μm
Dice uncertainty	40μm per side
Die thickness:	300μm
Input bonding pads:	One column
Pad size:	50μm x 66μm
Pad pitch:	100μm

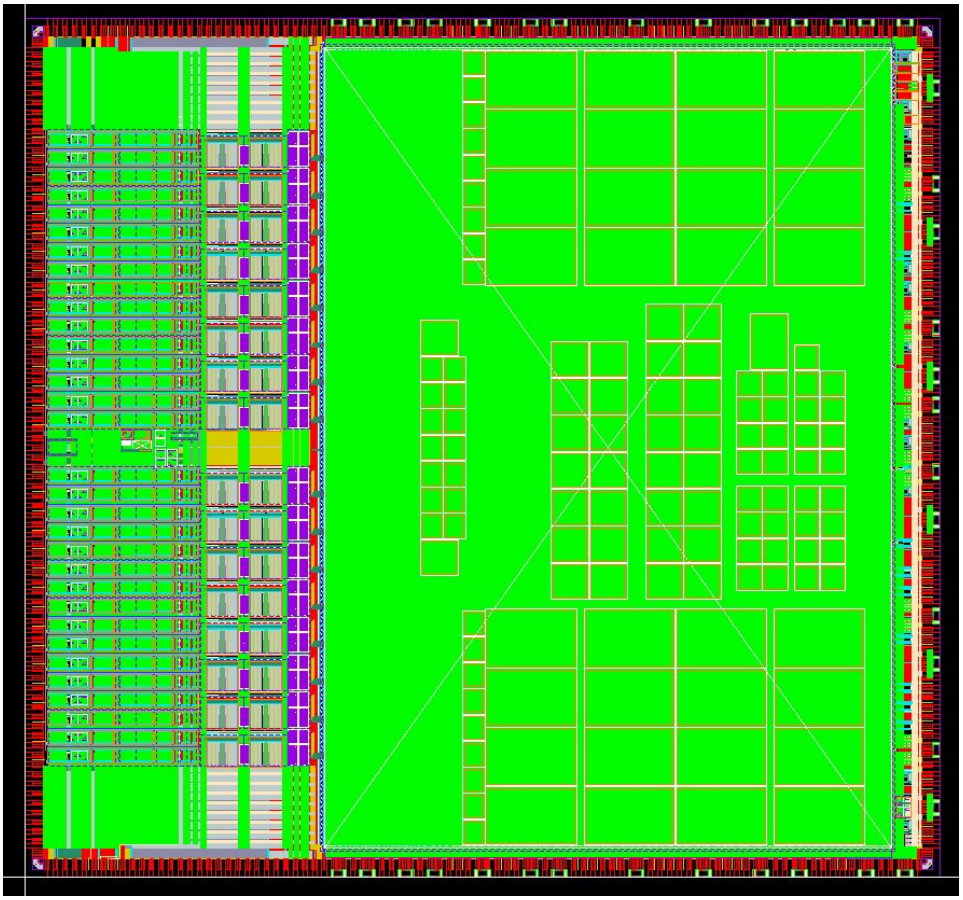


Figure 10: SAMPA V5 full layout.

The full chip is composed by several analog and digital blocks. Their position in the full chip is shown in Figure 11 and the size of each block is shown in Table 11.

The input pads are located on the left side. The output pads are on the right side. The top and bottom pads corresponds to the bias and power pads. The chip input, output and power pads are shown on Figure 12.

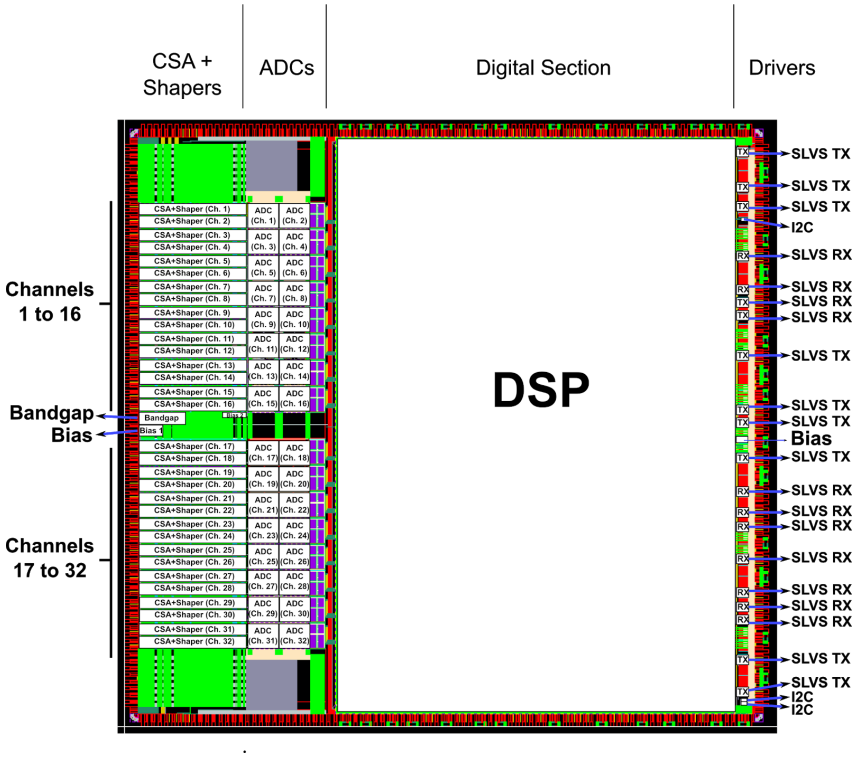


Figure 11: Full-chip with highlighted blocks

Table 11: Area of the full chip and of each block

Full Area:	9534 µm x 8944 µm
FE Channel area:	1559 µm x 193 µm
ADC area:	451 µm x 323 µm
DSP area:	5897 µm x 8536 µm
SLVS Tx area:	154 µm x 112 µm
SLVS Rx area:	142 µm x 82 µm
I2C area:	72 µm x 41 µm
Bandgap area:	305 µm x 222 µm
Bias01 area:	294 µm x 168 µm
Bias02 area:	270 µm x 71 µm
BiasTx area:	270 µm x 71 µm
POR area:	159 µm x 229 µm

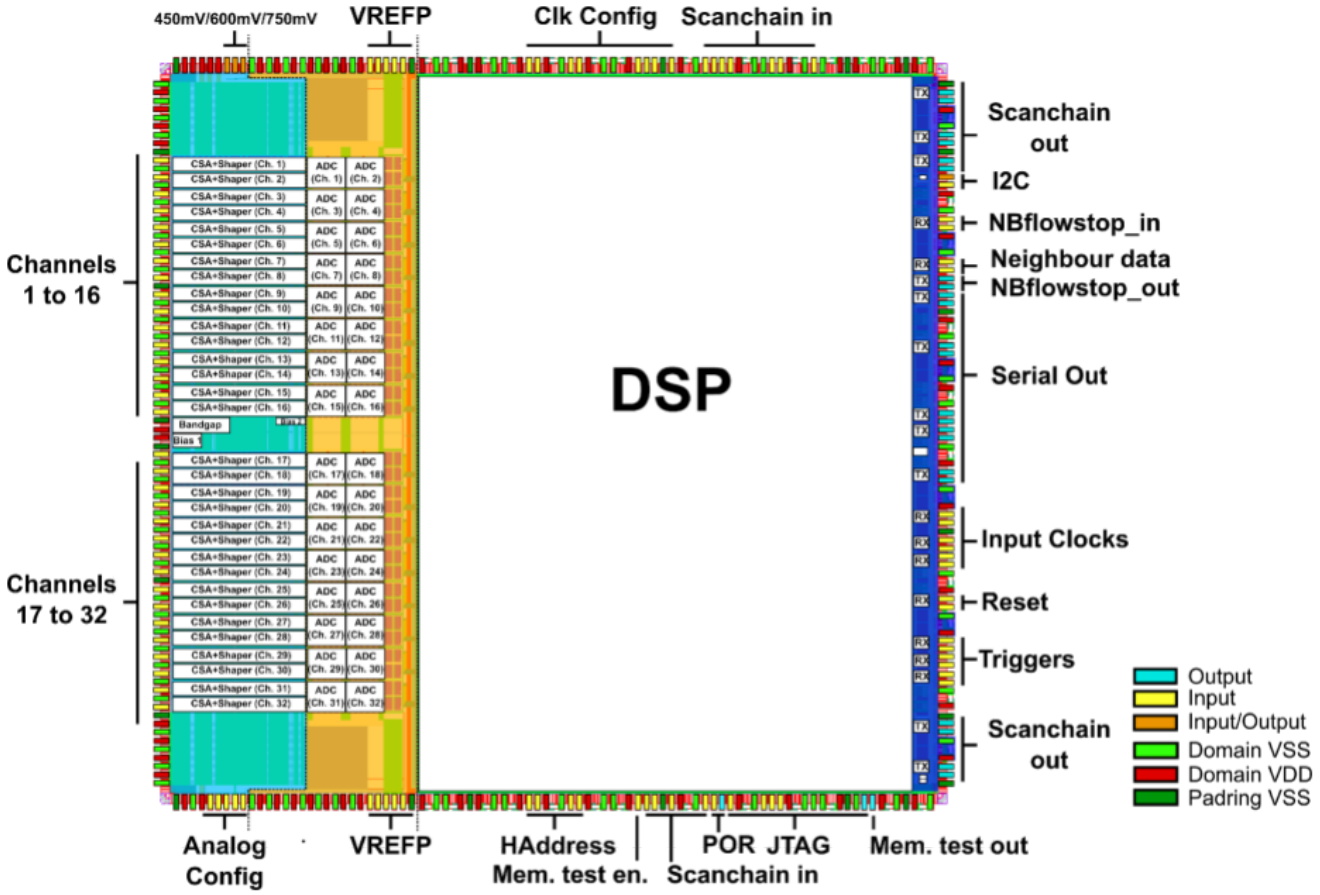


Figure 12: Inputs and outputs of the SAMPA V5 chip.

2.2 Pad assignments

The SAMPA V5 IC has 350 pads that are shown in Figure 13.

Pin assignments are defined in Table 12, Table 13, Table 14, Table 15 in this session.

When used as a die, the back should be connected to the PCB ground plane via conductive glue to the PCB analog ground plane.

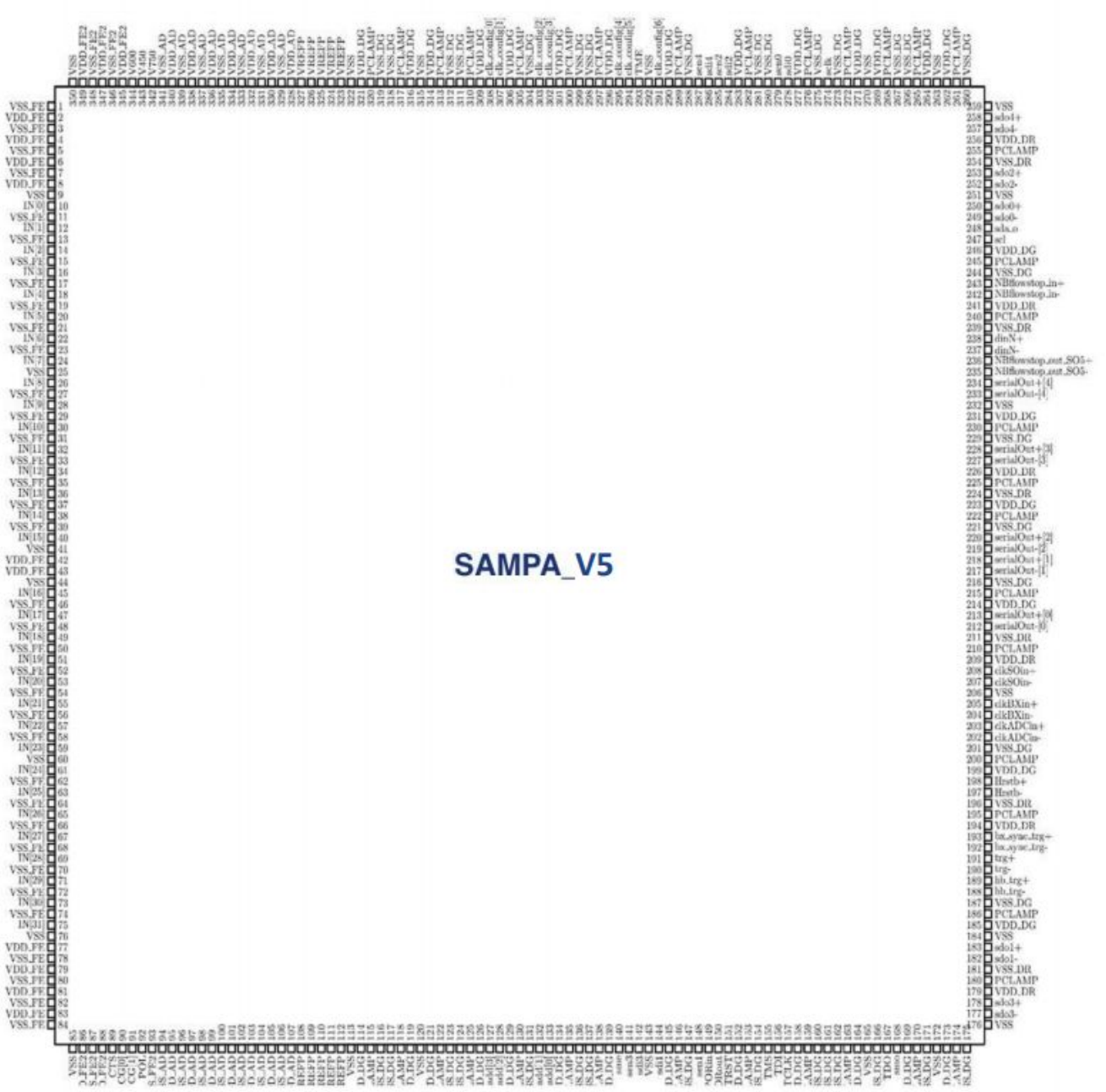


Figure 13: SAMPA V5 pad names.

2.3 Pad Description

Type definitions:

AI = Analog Input

AO = Analog output

DI = Digital input

DNC = Do not connect

DO = Digital output

P = Power or ground

Table 12: Pad description part1.

Pad #	Pad Name	IO type	Pad Description	Pad #	Pad Name	IO type	Pad Description
1	VSS_FE	P	Analog ground FS and CSA	43	VDD_FE	P	Analog core voltage FS and CSA
2	VDD_FE	P	Analog core voltage FS and CSA	44	VSS	P	PADRING ground
3	VSS_FE	P	Analog ground FS and CSA	45	IN[16]	AI	Analog channel 16
4	VDD_FE	P	Analog core voltage FS and CSA	46	VSS_FE	P	Analog ground FS and CSA
5	VSS_FE	P	Analog ground FS and CSA	47	IN[17]	AI	Analog channel 17
6	VDD_FE	P	Analog core voltage FS and CSA	48	VSS_FE	P	Analog ground FS and CSA
7	VSS_FE	P	Analog ground FS and CSA	49	IN[18]	AI	Analog channel 18
8	VDD_FE	P	Analog core voltage FS and CSA	50	VSS_FE	P	Analog ground FS and CSA
9	VSS	P	PADRING ground	51	IN[19]	AI	Analog channel 19
10	IN[0]	AI	Analog channel 0	52	VSS_FE	P	Analog ground FS and CSA
11	VSS_FE	P	Analog ground FS and CSA	53	IN[20]	AI	Analog channel 20
12	IN[1]	AI	Analog channel 1	54	VSS_FE	P	Analog ground FS and CSA
13	VSS_FE	P	Analog ground FS and CSA	55	IN[21]	AI	Analog channel 21
14	IN[2]	AI	Analog channel 2	56	VSS_FE	P	Analog ground FS and CSA
15	VSS_FE	P	Analog ground FS and CSA	57	IN[22]	AI	Analog channel 22
16	IN[3]	AI	Analog channel 3	58	VSS_FE	P	Analog ground FS and CSA
17	VSS_FE	P	Analog ground FS and CSA	59	IN[23]	AI	Analog channel 23
18	IN[4]	AI	Analog channel 4	60	VSS	P	PADRING ground
19	VSS_FE	P	Analog ground FS and CSA	61	IN[24]	AI	Analog channel 24
20	IN[5]	AI	Analog channel 5	62	VSS_FE	P	Analog ground FS and CSA
21	VSS_FE	P	Analog ground FS and CSA	63	IN[25]	AI	Analog channel 25
22	IN[6]	AI	Analog channel 6	64	VSS_FE	P	Analog ground FS and CSA
23	VSS_FE	P	Analog ground FS and CSA	65	IN[26]	AI	Analog channel 26
24	IN[7]	AI	Analog channel 7	66	VSS_FE	P	Analog ground FS and CSA
25	VSS	P	PADRING ground	67	IN[27]	AI	Analog channel 27
26	IN[8]	AI	Analog channel 8	68	VSS_FE	P	Analog ground FS and CSA
27	VSS_FE	P	Analog ground FS and CSA	69	IN[28]	AI	Analog channel 28
28	IN[9]	AI	Analog channel 9	70	VSS_FE	P	Analog ground FS and CSA
29	VSS_FE	P	Analog ground FS and CSA	71	IN[29]	AI	Analog channel 29
30	IN[10]	AI	Analog channel 10	72	VSS_FE	P	Analog ground FS and CSA
31	VSS_FE	P	Analog ground FS and CSA	73	IN[30]	AI	Analog channel 30
32	IN[11]	AI	Analog channel 11	74	VSS_FE	P	Analog ground FS and CSA
33	VSS_FE	P	Analog ground FS and CSA	75	IN[31]	AI	Analog channel 31
34	IN[12]	AI	Analog channel 12	76	VSS	P	PADRING ground
35	VSS_FE	P	Analog ground FS and CSA	77	VDD_FE	P	Analog core voltage FS and CSA
36	IN[13]	AI	Analog channel 13	78	VSS_FE	P	Analog ground FS and CSA
37	VSS_FE	P	Analog ground FS and CSA	79	VDD_FE	P	Analog core voltage FS and CSA
38	IN[14]	AI	Analog channel 14	80	VSS_FE	P	Analog ground FS and CSA
39	VSS_FE	P	Analog ground FS and CSA	81	VDD_FE	P	Analog core voltage FS and CSA
40	IN[15]	AI	Analog channel 15	82	VSS_FE	P	Analog ground FS and CSA
41	VSS	P	PADRING ground	83	VDD_FE	P	Analog core voltage FS and CSA
42	VDD_FE	P	Analog core voltage FS and CSA	84	VSS_FE	P	Analog ground FS and CSA

Table 13: Pad description part 2.

Pad #	Pad Name	IO type	Pad Description	Pad #	Pad Name	IO type	Pad Description
85	VSS	P	PADRING ground	131	VSS_DG	P	Digital ground
86	VDD_FE2	P	Analog core voltage SS and output buffer	132	hadd[1]	DI	Chip address (Static)
87	VSS_FE2	P	Analog ground SS and output buffer	133	hadd[0]	DI	Chip address (Static)
88	VDD_FE2	P	Analog core voltage SS and output buffer	134	VDD_DG	P	Digital core voltage
89	CTS	AI	Shaping configuration (Static)	135	PCLAMP	DNC	POWER CUT RESERVED SPACE
90	CG0	AI	Gain configuration (Static)	136	VSS_DG	P	Digital ground
91	CG1	AI	Gain configuration (Static)	137	VSS_DG	P	Digital ground
92	POL	AI	Polarity configuration (Static)	138	PCLAMP	DNC	POWER CUT RESERVED SPACE
93	VSS_FE2	P	Analog ground SS and output buffer	139	VDD_DG	P	Digital core voltage
94	VSS_AD	P	ADC supply ground	140	sme	DI	MEM Test En (CMOS)
95	VDD_AD	P	ADC supply voltage	141	sen3	DI	Scanchain test Scan Enable (CMOS)
96	VSS_AD	P	ADC supply ground	142	sdi3	DI	Scanchain test Scan In (CMOS)
97	VDD_AD	P	ADC supply voltage	143	VSS	P	PADRING ground
98	VSS_AD	P	ADC supply ground	144	sdi1	DI	Scanchain test Scan In (CMOS)
99	VDD_AD	P	ADC supply voltage	145	VDD_DG	P	Digital core voltage
100	VSS_AD	P	ADC supply ground	146	PCLAMP	DNC	POWER CUT RESERVED SPACE
101	VDD_AD	P	ADC supply voltage	147	VSS_DG	P	Digital ground
102	VSS_AD	P	ADC supply ground	148	sen1	DI	Scanchain test Scan Enable (CMOS)
103	VDD_AD	P	ADC supply voltage	149	PORin	DI	Power on reset input (CMOS)
104	VSS_AD	P	ADC supply ground	150	PORout	DO	Power on reset output (CMOS)
105	VDD_AD	P	ADC supply voltage	151	TRST	DI	JTAG (CMOS)
106	VSS_AD	P	ADC supply ground	152	VDD_DG	P	Digital core voltage
107	VDD_AD	P	ADC supply voltage	153	PCLAMP	DNC	POWER CUT RESERVED SPACE
108	VREFP	P	Voltage reference p	154	VSS_DG	P	Digital ground
109	VREFP	P	Voltage reference p	155	TMS	DI	JTAG (CMOS)
110	VREFP	P	Voltage reference p	156	TDI	DI	JTAG (CMOS)
111	VREFP	P	Voltage reference p	157	TCLK	DI	JTAG (CMOS)
112	VREFP	P	Voltage reference p	158	VDD_DG	P	Digital core voltage
113	VSS	P	PADRING ground	159	PCLAMP	DNC	POWER CUT RESERVED SPACE
114	VDD_DG	P	Digital core voltage	160	VSS_DG	P	Digital ground
115	PCLAMP	DNC	POWER CUT RESERVED SPACE	161	VSS_DG	P	Digital ground
116	VSS_DG	P	Digital ground	162	VSS_DG	P	Digital ground
117	VSS_DG	P	Digital ground	163	PCLAMP	DNC	POWER CUT RESERVED SPACE
118	PCLAMP	DNC	POWER CUT RESERVED SPACE	164	VDD_DG	P	Digital core voltage
119	VDD_DG	P	Digital core voltage	165	VSS	P	PADRING ground
120	VSS	P	PADRING ground	166	VSS_DG	P	Digital ground
121	VDD_DG	P	Digital core voltage	167	TDO	DO	JTAG (CMOS)
122	PCLAMP	DNC	POWER CUT RESERVED SPACE				
123	VSS_DG	P	Digital ground	169	VDD_DG	P	Digital core voltage
124	VSS_DG	P	Digital ground	170	PCLAM	DNC	POWER CUT RESERVED

					P		SPACE
125	PCLAMP	DNC	POWER CUT RESERVED SPACE	171	VSS_DG	P	Digital ground
126	VDD_DG	P	Digital core voltage	172	VSS	P	PADRING ground
127	hadd[3]	DI	Chip address (Static)	173	VDD_DG	P	Digital core voltage
128	hadd[2]	DI	Chip address (Static)	174	PCLAMP	DNC	POWER CUT RESERVED SPACE
129	VDD_DG	P	Digital core voltage	175	VSS_DG	P	Digital ground
130	PCLAMP	DNC	POWER CUT RESERVED SPACE				

Table 14: Pad description part 3

Pad #	Pad Name	IO type	Pad Description	Pad #	Pad Name	IO type	Pad Description
176	VSS	P	PADRING ground	218	serialOut+[1]	DO	Serial data link 1 p (SLVS)
177	sdo3-	DO	Scanchain test Scan Out (SLVS)	219	serialOut-[2]	DO	Serial data link 2 n (SLVS)
178	sdo3+	DO	Scanchain test Scan Out (SLVS)	220	serialOut+[2]	DO	Serial data link 2 p (SLVS)
179	VDD_DR	P	Digital SLVS drivers voltage	221	VSS_DG	P	Digital ground
180	PCLAMP	DNC	POWER CUT RESERVED SPACE	222	PCLAMP	DNC	POWER CUT RESERVED SPACE
181	VSS_DR	P	Digital SLVS drivers ground	223	VDD_DG	P	Digital core voltage
182	sdo1-	DO	Scanchain test Scan Out (SLVS)	224	VSS_DR	P	Digital SLVS drivers ground
183	sdo1+	DO	Scanchain test Scan Out (SLVS)	225	PCLAMP	DNC	POWER CUT RESERVED SPACE
184	VSS	P	PADRING ground	226	VDD_DR	P	Digital SLVS drivers voltage
185	VDD_DG	P	Digital core voltage	227	serialOut-[3]	DO	Serial data link 3 n (SLVS)
186	PCLAMP	DNC	POWER CUT RESERVED SPACE	228	serialOut+[3]	DO	Serial data link 3 p (SLVS)
187	VSS_DG	P	Digital ground	229	VSS_DG	P	Digital ground
188	hb_trg-	DI	Heartbeat trigger n (SLVS)	230	PCLAMP	DNC	POWER CUT RESERVED SPACE
189	hb_trg+	DI	Heartbeat trigger p (SLVS)	231	VDD_DG	P	Digital core voltage
190	trg-	DI	Event trigger n (SLVS)	232	VSS	P	PADRING ground
191	trg+	DI	Event trigger p (SLVS)	233	serialOut-[4]	DO	Serial data link 4 n (SLVS)
192	bx_sync_trg-	DI	Bunchcrossing counter sync n (SLVS)	234	serialOut+[4]	DO	Serial data link 4 p (SLVS)
193	bx_sync_trg+	DI	Bunchcrossing counter sync p (SLVS)	235	Nbflowstop_out_SO5-	DO	Stop neighbour data out or serial data link 5 n (SLVS)
194	VDD_DR	P	Digital SLVS drivers voltage	236	Nbflowstop_out_SO5+	DO	Stop neighbour data out or serial data link 5 p (SLVS)
195	PCLAMP	DNC	POWER CUT RESERVED SPACE	237	dinN-	DI	Neigbour chip data n (SLVS)
196	VSS_DR	P	Digital SLVS drivers ground	238	dinN+	DI	Neigbour chip data p (SLVS)
197	Hrstb-	DI	Reset n (SLVS)	239	VSS_DR	P	Digital SLVS drivers ground
198	Hrstb+	DI	Reset p (SLVS)	240	PCLAMP	DNC	POWER CUT RESERVED SPACE
199	VDD_DG	P	Digital core voltage	241	VDD_DR	P	Digital SLVS drivers voltage
200	PCLAMP	DNC	POWER CUT RESERVED SPACE	242	Nbflowstop_in-	DI	Stop neighbour data in n (SLVS)
201	VSS_DG	P	Digital ground	243	Nbflowstop_in+	DI	Stop neighbour data in p (SLVS)
202	clkADCin-	DI	ADC clock n (SLVS)	244	VSS_DG	P	Digital ground
203	clkADCin+	DI	ADC clock p (SLVS)	245	PCLAMP	DNC	POWER CUT RESERVED SPACE
204	clkBXin-	DI	Bunchcrossing clock n (SLVS)	246	VDD_DG	P	Digital core voltage
205	clkBXin+	DI	Bunchcrossing clock p (SLVS)	247	scl	I2C	I2C clock
206	VSS	DI	PADRING ground	248	sda_o	I2C	I2C data

207	clkSOin-	DI	Serial out clock n (SLVS)	249	sdo0-	DO	Scanchain test Scan Out (SLVS)
208	clkSOin+	DI	Serial out clock p (SLVS)	250	sdo0+	DO	Scanchain test Scan Out (SLVS)
209	VDD_DR	P	Digital SLVS drivers voltage	251	VSS	P	PADRING ground
210	PCLAMP	DNC	POWER CUT RESERVED SPACE	252	sdo2-	DO	Scanchain test Scan Out (SLVS)
211	VSS_DR	P	Digital SLVS drivers ground	253	sdo2+	DO	Scanchain test Scan Out (SLVS)
212	serialOut-[0]	DO	Serial data link 0 n (SLVS)	254	VSS_DR	P	Digital SLVS drivers ground
213	serialOut+[0]	DO	Serial data link 0 p (SLVS)	255	PCLAMP	DNC	POWER CUT RESERVED SPACE
214	VDD_DG	P	Digital core voltage	256	VDD_DR	P	Digital SLVS drivers voltage
215	PCLAMP	DNC	POWER CUT RESERVED SPACE	257	sdo4-	DO	Scanchain test Scan Out (SLVS)
216	VSS_DG	P	Digital ground	258	sdo4+	DO	Scanchain test Scan Out (SLVS)
217	serialOut-[1]	DO	Serial data link 1 n (SLVS)	259	VSS	P	PADRING ground

Table 15: Pad description part 4.

Pad #	Pad Name	IO type	Pad Description	Pad #	Pad Name	IO type	Pad Description
260	VSS_DG	P	Digital ground	306	VDD_DG	P	Digital core voltage
261	PCLAMP	DNC	POWER CUT RESERVED SPACE	307	clk_config[1]	DI	Clock configuration (Static)
262	VDD_DG	P	Digital core voltage	308	clk_config[0]	DI	Clock configuration (Static)
263	VSS	P	PADRING ground	309	VDD_DG	P	Digital core voltage
264	VDD_DG	P	Digital core voltage	310	PCLAMP	DNC	POWER CUT RESERVED SPACE
265	PCLAMP	DNC	POWER CUT RESERVED SPACE	311	VSS_DG	P	Digital ground
266	VSS_DG	P	Digital ground	312	VSS_DG	P	Digital ground
267	VSS_DG	P	Digital ground	313	PCLAMP	DNC	POWER CUT RESERVED SPACE
268	PCLAMP	DNC	POWER CUT RESERVED SPACE	314	VDD_DG	P	Digital core voltage
269	VDD_DG	P	Digital core voltage	315	VSS	P	PADRING ground
270	VSS	P	PADRING ground	316	VDD_DG	P	Digital core voltage
271	VDD_DG	P	Digital core voltage	317	PCLAMP	DNC	POWER CUT RESERVED SPACE
272	PCLAMP	DNC	POWER CUT RESERVED SPACE	318	VSS_DG	P	Digital ground
273	VSS_DG	P	Digital ground	319	VSS_DG	P	Digital ground
274	sclk	DI	Scanchain test clock (CMOS)	320	PCLAMP	DNC	POWER CUT RESERVED SPACE
275	VSS_DG	P	Digital ground	321	VDD_DG	P	Digital core voltage
276	PCLAMP	DNC	POWER CUT RESERVED SPACE	322	VSS	P	PADRING ground
277	VDD_DG	P	Digital core voltage	323	VREFP	P	Voltage reference p
278	sdi0	DI	Scanchain test Scan In (CMOS)	324	VREFP	P	Voltage reference p
279	sen0	DI	Scanchain test Scan Enable (CMOS)	325	VREFP	P	Voltage reference p
280	VSS_DG	P	Digital ground	326	VREFP	P	Voltage reference p
281	VSS_DG	P	Digital ground	327	VREFP	P	Voltage reference p
282	PCLAMP	DNC	POWER CUT RESERVED SPACE	328	VDD_AD	P	ADC supply voltage
283	VDD_DG	P	Digital core voltage	329	VSS_AD	P	ADC supply ground
284	sdi2	DI	Scanchain test Scan In (CMOS)	330	VDD_AD	P	ADC supply voltage
285	sen2	DI	Scanchain test Scan Enable (CMOS)	331	VSS_AD	P	ADC supply ground
286	sdi4	DI	Scanchain test Scan In (CMOS)	332	VDD_AD	P	ADC supply voltage
287	sen4	DI	Scanchain test Scan Enable (CMOS)	333	VSS_AD	P	ADC supply ground
288	VSS_DG	P	Digital ground	334	VDD_AD	P	ADC supply voltage
289	PCLAMP	DNC	POWER CUT RESERVED SPACE	335	VSS_AD	P	ADC supply ground
290	VDD_DG	P	Digital core voltage	336	VDD_AD	P	ADC supply voltage
291	clk_config[6]	DI	Clock configuration (Internal DSP Clock Gatting) (Static)	337	VSS_AD	P	ADC supply ground
292	VSS	P	PADRING ground	338	VDD_AD	P	ADC supply voltage
293	TME	DI	Scanchain test ? TEST MODE EN (CMOS)	339	VSS_AD	P	ADC supply ground
294	clk_config[5]	DI	Clock configuration (Static)	340	VDD_AD	P	ADC supply voltage
295	clk_config[4]	DI	Clock configuration (Static)	341	VSS_AD	P	ADC supply ground
296	VDD_DG	P	Digital core voltage	342	V750	P	Bandgap voltage reference (750mV)
297	PCLAMP	DNC	POWER CUT RESERVED SPACE	343	V450	P	Bandgap voltage reference (450mV)
298	VSS_DG	P	Digital ground	344	V600	P	Bandgap voltage reference (600mV)
299	VSS_DG	P	Digital ground	345	VDD_FE2	P	Analog core voltage SS and output buffer
300	PCLAMP	DNC	POWER CUT RESERVED SPACE	346	VSS_FE2	P	Analog ground SS and output buffer
301	VDD_DG	P	Digital core voltage	347	VDD_FE2	P	Analog core voltage SS and output buffer
302	clk_config[3]	DI	Clock configuration (Static)	348	VSS_FE2	P	Analog ground SS and output buffer

303	clk_config[2]	DI	Clock configuration (Static)	349	VDD_FE2	P	Analog core voltage SS and output buffer
304	VSS_DG	P	Digital ground	350	VSS	P	PADRING ground
305	PCLAMP	DNC	POWER CUT RESERVED SPACE				

2.4 Pad Coordinates

Table 16: Pad coordinates left side.

Pad #	Pad Name	X-coordinate	Y-coordinate	Pad #	Pad Name	X-coordinate	Y-coordinate
1	VSS_FE	35	8621.8	43	VDD_FE	35	4421.8
2	VDD_FE	35	8521.8	44	VSS	35	4321.8
3	VSS_FE	35	8421.8	45	IN[16]	35	4221.8
4	VDD_FE	35	8321.8	46	VSS_FE	35	4121.8
5	VSS_FE	35	8221.8	47	IN[17]	35	4021.8
6	VDD_FE	35	8121.8	48	VSS_FE	35	3921.8
7	VSS_FE	35	8021.8	49	IN[18]	35	3821.8
8	VDD_FE	35	7921.8	50	VSS_FE	35	3721.8
9	VSS	35	7821.8	51	IN[19]	35	3621.8
10	IN[0]	35	7721.8	52	VSS_FE	35	3521.8
11	VSS_FE	35	7621.8	53	IN[20]	35	3421.8
12	IN[1]	35	7521.8	54	VSS_FE	35	3321.8
13	VSS_FE	35	7421.8	55	IN[21]	35	3221.8
14	IN[2]	35	7321.8	56	VSS_FE	35	3121.8
15	VSS_FE	35	7221.8	57	IN[22]	35	3021.8
16	IN[3]	35	7121.8	58	VSS_FE	35	2921.8
17	VSS_FE	35	7021.8	59	IN[23]	35	2821.8
18	IN[4]	35	6921.8	60	VSS	35	2721.8
19	VSS_FE	35	6821.8	61	IN[24]	35	2621.8
20	IN[5]	35	6721.8	62	VSS_FE	35	2521.8
21	VSS_FE	35	6621.8	63	IN[25]	35	2421.8
22	IN[6]	35	6521.8	64	VSS_FE	35	2321.8
23	VSS_FE	35	6421.8	65	IN[26]	35	2221.8
24	IN[7]	35	6321.8	66	VSS_FE	35	2121.8
25	VSS	35	6221.8	67	IN[27]	35	2021.8
26	IN[8]	35	6121.8	68	VSS_FE	35	1921.8
27	VSS_FE	35	6021.8	69	IN[28]	35	1821.8
28	IN[9]	35	5921.8	70	VSS_FE	35	1721.8
29	VSS_FE	35	5821.8	71	IN[29]	35	1621.8
30	IN[10]	35	5721.8	72	VSS_FE	35	1521.8
31	VSS_FE	35	5621.8	73	IN[30]	35	1421.8
32	IN[11]	35	5521.8	74	VSS_FE	35	1321.8
33	VSS_FE	35	5421.8	75	IN[31]	35	1221.8
34	IN[12]	35	5321.8	76	VSS	35	1121.8
35	VSS_FE	35	5221.8	77	VDD_FE	35	1021.8
36	IN[13]	35	5121.8	78	VSS_FE	35	921.8
37	VSS_FE	35	5021.8	79	VDD_FE	35	821.8
38	IN[14]	35	4921.8	80	VSS_FE	35	721.8
39	VSS_FE	35	4821.8	81	VDD_FE	35	621.8
40	IN[15]	35	4721.8	82	VSS_FE	35	521.8
41	VSS	35	4621.8	83	VDD_FE	35	421.8
42	VDD_FE	35	4521.8	84	VSS_FE	35	321.8

Table 17: Pad coordinates bottom side.

Pad #	Pad Name	X-coordinate	Y-coordinate	Pad #	Pad Name	X-coordinate	Y-coordinate
85	VSS	266.8	35	131	VSS_DG	4866.8	35
86	VDD_FE2	366.8	35	132	hadd[1]	4966.8	35
87	VSS_FE2	466.8	35	133	hadd[0]	5066.8	35
88	VDD_FE2	566.8	35	134	VDD_DG	5166.8	35
89	CTS	666.8	35	135	PCLAMP	5266.8	35
90	CG$<0>$	766.8	35	136	VSS_DG	5366.8	35
91	CG$<1>$	866.8	35	137	VSS_DG	5466.8	35
92	POL	966.8	35	138	PCLAMP	5566.8	35
93	VSS_FE2	1066.8	35	139	VDD_DG	5666.8	35
94	VSS_AD	1166.8	35	140	sme	5766.8	35
95	VDD_AD	1266.8	35	141	sen3	5866.8	35
96	VSS_AD	1366.8	35	142	sdi3	5966.8	35
97	VDD_AD	1466.8	35	143	VSS	6066.8	35
98	VSS_AD	1566.8	35	144	sdi1	6166.8	35
99	VDD_AD	1666.8	35	145	VDD_DG	6266.8	35
100	VSS_AD	1766.8	35	146	PCLAMP	6366.8	35
101	VDD_AD	1866.8	35	147	VSS_DG	6466.8	35
102	VSS_AD	1966.8	35	148	sen1	6566.8	35
103	VDD_AD	2066.8	35	149	PORin	6666.8	35
104	VSS_AD	2166.8	35	150	PORout	6766.8	35
105	VDD_AD	2266.8	35	151	TRST	6866.8	35
106	VSS_AD	2366.8	35	152	VDD_DG	6966.8	35
107	VDD_AD	2466.8	35	153	PCLAMP	7066.8	35
108	VREFP	2566.8	35	154	VSS_DG	7166.8	35
109	VREFP	2666.8	35	155	TMS	7266.8	35
110	VREFP	2766.8	35	156	TDI	7366.8	35
111	VREFP	2866.8	35	157	TCLK	7466.8	35
112	VREFP	2966.8	35	158	VDD_DG	7566.8	35
113	VSS	3066.8	35	159	PCLAMP	7666.8	35
114	VDD_DG	3166.8	35	160	VSS_DG	7766.8	35
115	PCLAMP	3266.8	35	161	VSS_DG	7866.8	35
116	VSS_DG	3366.8	35	162	VSS_DG	7966.8	35
117	VSS_DG	3466.8	35	163	PCLAMP	8066.8	35
118	PCLAMP	3566.8	35	164	VDD_DG	8166.8	35
119	VDD_DG	3666.8	35	165	VSS	8266.8	35
120	VSS	3766.8	35	166	VSS_DG	8366.8	35
121	VDD_DG	3866.8	35	167	TDO	8466.8	35
122	PCLAMP	3966.8	35	168	smo	8566.8	35
123	VSS_DG	4066.8	35	169	VDD_DG	8666.8	35
124	VSS_DG	4166.8	35	170	PCLAMP	8766.8	35
125	PCLAMP	4266.8	35	171	VSS_DG	8866.8	35
126	VDD_DG	4366.8	35	172	VSS	8966.8	35
127	hadd[3]	4466.8	35	173	VDD_DG	9066.8	35
128	hadd[2]	4566.8	35	174	PCLAMP	9166.8	35
129	VDD_DG	4666.8	35	175	VSS_DG	9266.8	35
130	PCLAMP	4766.8	35				

Table 18: Pad coordinates right side.

Pad #	Pad Name	X-coordinate	Y-coordinate	Pad #	Pad Name	X-coordinate	Y-coordinate
176	VSS	9498.6	321.8	218	serialOut+[1]	9498.6	100
177	sdo3-	9498.6	421.8	219	serialOut-[2]	9498.6	200
178	sdo3+	9498.6	521.8	220	serialOut+[2]	9498.6	300
179	VDD_DR	9498.6	621.8	221	VSS_DG	9498.6	400
180	PCLAMP	9498.6	721.8	222	PCLAMP	9498.6	500
181	VSS_DR	9498.6	821.8	223	VDD_DG	9498.6	600
182	sdo1-	9498.6	921.8	224	VSS_DR	9498.6	700
183	sdo1+	9498.6	1021.8	225	PCLAMP	9498.6	800
184	VSS	9498.6	1121.8	226	VDD_DR	9498.6	900
185	VDD_DG	9498.6	1221.8	227	serialOut-[3]	9498.6	1000
186	PCLAMP	9498.6	1321.8	228	serialOut+[3]	9498.6	1100
187	VSS_DG	9498.6	1421.8	229	VSS_DG	9498.6	1200
188	hb_trg-	9498.6	1521.8	230	PCLAMP	9498.6	1300
189	hb_trg+	9498.6	1621.8	231	VDD_DG	9498.6	1400
190	trg-	9498.6	1721.8	232	VSS	9498.6	1500
191	trg+	9498.6	1821.8	233	serialOut-[4]	9498.6	1600
192	bx_sync_trg-	9498.6	1921.8	234	serialOut+[4]	9498.6	1700
193	bx_sync_trg+	9498.6	2021.8	235	Nbflowstop_out_SO5-	9498.6	1800
194	VDD_DR	9498.6	2121.8	236	Nbflowstop_out_SO5+	9498.6	1900
195	PCLAMP	9498.6	2221.8	237	dinN-	9498.6	2000
196	VSS_DR	9498.6	2321.8	238	dinN+	9498.6	2100
197	Hrstb-	9498.6	2421.8	239	VSS_DR	9498.6	2200
198	Hrstb+	9498.6	2521.8	240	PCLAMP	9498.6	2300
199	VDD_DG	9498.6	2621.8	241	VDD_DR	9498.6	2400
200	PCLAMP	9498.6	2721.8	242	Nbflowstop_in-	9498.6	2500
201	VSS_DG	9498.6	2821.8	243	Nbflowstop_in+	9498.6	2600
202	clkADCin-	9498.6	2921.8	244	VSS_DG	9498.6	2700
203	clkADCin+	9498.6	3021.8	245	PCLAMP	9498.6	2800
204	clkBXin-	9498.6	3121.8	246	VDD_DG	9498.6	2900
205	clkBXin+	9498.6	3221.8	247	scl	9498.6	3000
206	VSS	9498.6	3321.8	248	sda_o	9498.6	3100
207	clkSOin-	9498.6	3421.8	249	sdo0-	9498.6	3200
208	clkSOin+	9498.6	3521.8	250	sdo0+	9498.6	3300
209	VDD_DR	9498.6	3621.8	251	VSS	9498.6	3400
210	PCLAMP	9498.6	3721.8	252	sdo2-	9498.6	3500
211	VSS_DR	9498.6	3821.8	253	sdo2+	9498.6	3600
212	serialOut-[0]	9498.6	3921.8	254	VSS_DR	9498.6	3700
213	serialOut+[0]	9498.6	4021.8	255	PCLAMP	9498.6	3800
214	VDD_DG	9498.6	4121.8	256	VDD_DR	9498.6	3900
215	PCLAMP	9498.6	4221.8	257	sdo4-	9498.6	4000
216	VSS_DG	9498.6	4321.8	258	sdo4+	9498.6	4100
217	serialOut-[1]	9498.6	4421.8	259	VSS	9498.6	4200

Table 19: Pad coordinates top side.

Pad #	Pad Name	X-coordinate	Y-coordinate	Pad #	Pad Name	X-coordinate	Y-coordinate
260	VSS_DG	9266.8	8908.6	306	VDD_DG	4666.8	8908.6
261	PCLAMP	9166.8	8908.6	307	clk_config[1]	4566.8	8908.6
262	VDD_DG	9066.8	8908.6	308	clk_config[0]	4466.8	8908.6
263	VSS	8966.8	8908.6	309	VDD_DG	4366.8	8908.6
264	VDD_DG	8866.8	8908.6	310	PCLAMP	4266.8	8908.6
265	PCLAMP	8766.8	8908.6	311	VSS_DG	4166.8	8908.6
266	VSS_DG	8666.8	8908.6	312	VSS_DG	4066.8	8908.6
267	VSS_DG	8566.8	8908.6	313	PCLAMP	3966.8	8908.6
268	PCLAMP	8466.8	8908.6	314	VDD_DG	3866.8	8908.6
269	VDD_DG	8366.8	8908.6	315	VSS	3766.8	8908.6
270	VSS	8266.8	8908.6	316	VDD_DG	3666.8	8908.6
271	VDD_DG	8166.8	8908.6	317	PCLAMP	3566.8	8908.6
272	PCLAMP	8066.8	8908.6	318	VSS_DG	3466.8	8908.6
273	VSS_DG	7966.8	8908.6	319	VSS_DG	3366.8	8908.6
274	sclk	7866.8	8908.6	320	PCLAMP	3266.8	8908.6
275	VSS_DG	7766.8	8908.6	321	VDD_DG	3166.8	8908.6
276	PCLAMP	7666.8	8908.6	322	VSS	3066.8	8908.6
277	VDD_DG	7566.8	8908.6	323	VREFP	2966.8	8908.6
278	sdi0	7466.8	8908.6	324	VREFP	2866.8	8908.6
279	sen0	7366.8	8908.6	325	VREFP	2766.8	8908.6
280	VSS_DG	7266.8	8908.6	326	VREFP	2666.8	8908.6
281	VSS_DG	7166.8	8908.6	327	VREFP	2566.8	8908.6
282	PCLAMP	7066.8	8908.6	328	VDD_AD	2466.8	8908.6
283	VDD_DG	6966.8	8908.6	329	VSS_AD	2366.8	8908.6
284	sdi2	6866.8	8908.6	330	VDD_AD	2266.8	8908.6
285	sen2	6766.8	8908.6	331	VSS_AD	2166.8	8908.6
286	sdi4	6666.8	8908.6	332	VDD_AD	2066.8	8908.6
287	sen4	6566.8	8908.6	333	VSS_AD	1966.8	8908.6
288	VSS_DG	6466.8	8908.6	334	VDD_AD	1866.8	8908.6
289	PCLAMP	6366.8	8908.6	335	VSS_AD	1766.8	8908.6
290	VDD_DG	6266.8	8908.6	336	VDD_AD	1666.8	8908.6
291	clk_config[6]	6166.8	8908.6	337	VSS_AD	1566.8	8908.6
292	VSS	6066.8	8908.6	338	VDD_AD	1466.8	8908.6
293	TME	5966.8	8908.6	339	VSS_AD	1366.8	8908.6
294	clk_config[5]	5866.8	8908.6	340	VDD_AD	1266.8	8908.6
295	clk_config[4]	5766.8	8908.6	341	VSS_AD	1166.8	8908.6
296	VDD_DG	5666.8	8908.6	342	V750	1066.8	8908.6
297	PCLAMP	5566.8	8908.6	343	V450	966.8	8908.6
298	VSS_DG	5466.8	8908.6	344	V600	866.8	8908.6
299	VSS_DG	5366.8	8908.6	345	VDD_FE2	766.8	8908.6
300	PCLAMP	5266.8	8908.6	346	VSS_FE2	666.8	8908.6
301	VDD_DG	5166.8	8908.6	347	VDD_FE2	566.8	8908.6
302	clk_config[3]	5066.8	8908.6	348	VSS_FE2	466.8	8908.6
303	clk_config[2]	4966.8	8908.6	349	VDD_FE2	366.8	8908.6
304	VSS_DG	4866.8	8908.6	350	VSS	266.8	8908.6
305	PCLAMP	4766.8	8908.6				

3. Electrical Specifications

3.1 Power Domains

The SAMPA ASIC has five power-domains, as follows:

FE Analogue front-end: First Shaper and Charge Sensitive Amplifier

FE2 Analogue Front-end: Second Shaper and Output Buffer

AD ADC

DG Core digital logic

DR SLVS IO drivers

Each power domain has its corresponding VDD and VSS net. Additionally there is a separate IO padring ground for the IO pad ESD diodes named just VSS. Figure 14 shows how the domains are separated through the padring and which blocks are connected to each domain. Table 20 describes the power nets, names, nominal voltages and observations for each domain

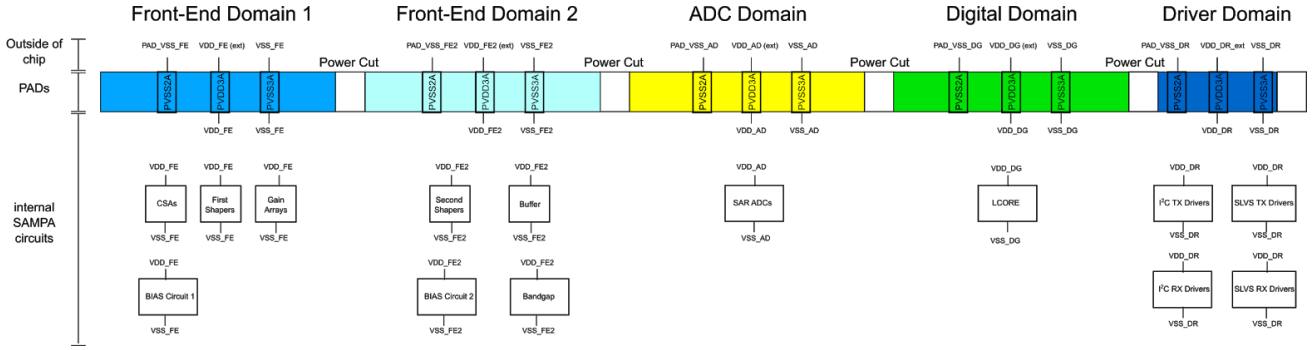


Figure 14: Power domains.

Table 20: Power nets per domain.

Power Net	Name	Nominal Voltage	Observation
Frontend Domain 1			
Ground	VSS_FE	0 V	
Supply Voltage	VSS_FE	1.25 V	
PADRING ground	VSS	0 V	common to all domains
Frontend Domain 1			
Ground	VSS_FE2	0 V	
Supply Voltage	VSS_FE2	1.25 V	
PADRING ground	VSS	0 V	common to all domains
ADC Domain			
Ground	VSS_AD	0 V	
Supply Voltage	VSS_AD	1.25 V	
PADRING ground	VSS	0 V	common to all domains

3.2 DSP Domain

Table 21: DSP Power nets.

Ground	VSS_DC	0 V	
Supply Voltage	VSS_DC	1.25 V	
PADRING ground	VSS	0 V	common to all domains
Driver Domain			
Ground	VSS_DR	0 V	
Supply Voltage	VSS_DR	1.25 V	
PADRING ground	VSS	0 V	common to all domains

3.3 Absolute maximum ratings

The nominal supply voltage of the SAMPA V5 chip is 1.25V with variation range of 5%, being: 1.1875V < 1.25V < 1.325V.

Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating range (table 20).

Operating the SAMPA V5 under conditions beyond its absolute maximum ratings may damage the device and affect the device reliability.

Table 22: Absolute maximum ratings

	Parameter	Rating
VDD_FE, VDD_FE2	Power supply voltage	1.18V to 1.33V
VDD_AD, VDD_DG, VDD_DR	Power supply voltage	1.18V to 1.33V
V_{IN}	Voltage applied to any input or output pin	-0.5V to 1.25V
T_S	Storage temperature	-55°C to +150°C
V_{HBM}	Electrostatic discharge rating, human body model	1500V
V_{CDM}	Electrostatic discharge rating, charge device model	200V

4. Package

The SAMPA_V5 mechanical specifications are presented in this chapter, including its physical dimensions and visible markings.

4.1. Package description

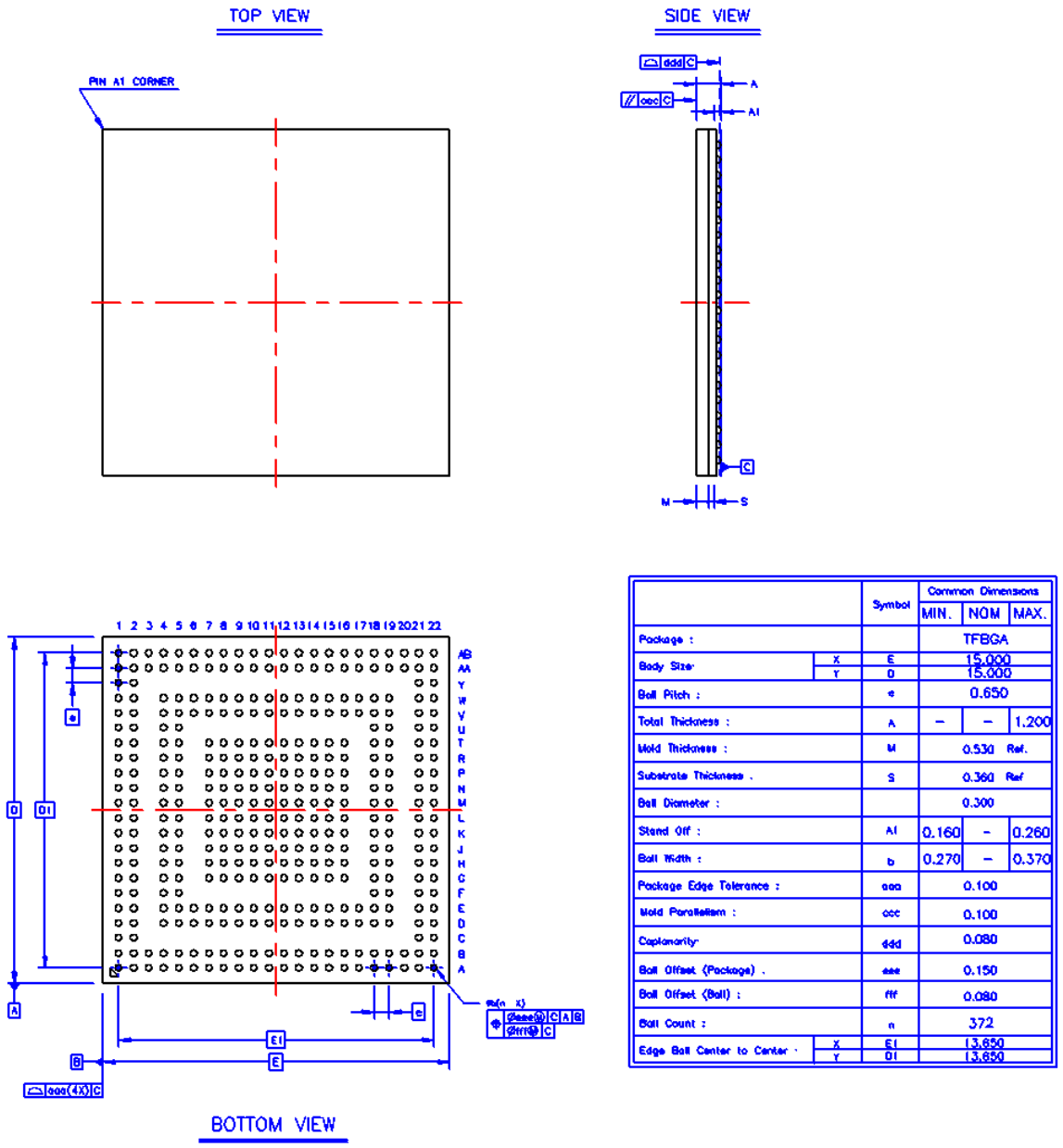
The SAMPA_V5 ASIC will be assembled in the TFBGA package that includes a large center ground slug for electrical grounding, mechanical strength, and thermal continuity. The package has a 15 mm x 15 mm body size, 1.2 mm thickness and a 0.65 mm ball pitch. The package provides 372 balls. Figure 15 the mechanical data and package dimensions. This is the same package used and validated for SAMPA_V4.

The SAMPA chip is a mixed signal chip, where extreme care should be taken to avoid interference and crosstalk between analog and digital domain. The package substrate keeps well-separated traces of different domains. The large center slug must be soldered to PCB ground for electrical ground, mechanical support, and thermal relief.

Figure 16 shows the ball layout of the package. White cells are signals (either *in* or *out*), blue cells are GND, while orange are VDD (each tone identifies a different power domain).

Figures 17 to 20 show the layouts of the 4-substrate layers. The second layer is a ground plane, with shielding purposes, while in others the separation in different domains are visible.

In order to improve overall performance, the package includes, on the substrate inside the package, a capacitor between ground and power for the two most sensitive domains: the power for the ADC (VDD_AD) and the voltage reference for the ADC (VREFP). In both cases a 100nF 0603 SMD capacitor is embedded in the package.



		Symbol	Common Dimensions		
			MIN.	NOM	MAX.
Package :			TFBGA		
Body Size	X	E		15.000	
	Y	D		15.000	
Ball Pitch :		e		0.650	
Total Thickness :		A	–	–	1.200
Mold Thickness :		M		0.530 Ref.	
Substrate Thickness :		S		0.360 Ref	
Ball Diameter :				0.300	
Stand Off :		A1	0.160	–	0.260
Ball Width :		b	0.270	–	0.370
Package Edge Tolerance :		aaa		0.100	
Mold Parallelism :		ccc		0.100	
Coplanarity:		ddd		0.080	
Ball Offset (Package) :		eee		0.150	
Ball Offset (Ball) :		fff		0.080	
Ball Count :		n		372	
Edge Ball Center to Center :	X	E1		13.650	
	Y	D1		13.650	

Figure 15: Mechanical data and package dimensions.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	IN[1]	IN[0]	N/C	V450	V600	V750	VREFP	VREFP	VREFP	clk_config[3]	clk_config[4]	clk_config[5]	VSS_DG	sclk	sen4	sen2	sen0	N/C	N/C	sdo4-	N/C	sdo2-	A
B	IN[2]	N/C	VDD_FE2	VDD_FE2	VDD_AD	VDD_AD	VDD_AD	VREFP	VREFP	clk_config[0]	clk_config[1]	clk_config[2]	VSS_DG	clk_config[6]	TME	sdi4	sdi2	sdi0	N/C	sdo4+	N/C	sdo2+	B
C	IN[3]	VSS_FE																			sdo0-	sdo0+	C
D	IN[4]	N/C		VSS	VSS_AD	VSS_AD	VDD_AD	VDD_AD	VDD_AD	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VSS_DG	VSS_DG		sda_o	scl	D
E	IN[5]	VSS_FE		VDD_FE	VSS	VSS_AD	VDD_AD	VDD_AD	VDD_AD	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DR	VDD_DR	VDD_DG	NBflowstop_in-	NBflowstop_in+		VSS_DG	VSS_DG	E
F	IN[6]	N/C		VDD_FE	VSS_FE2													VSS_DG	VSS_DG		dinN-	dinN+	F
G	IN[7]	VSS_FE		VDD_FE	VSS_FE2		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DR	VSS_DG	VDD_DG		NBflowstop_out_SO5-	NBflowstop_out_SO5+		VSS_DG	VSS_DG	G
H	IN[8]	IN[9]		VDD_FE	VSS_FE2		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS	VSS_DG	VSS	VSS	VSS	VDD_DG		VSS_DG	VSS_DG		serialOut-[3]	serialOut+[3]	H
J	IN[10]	IN[11]		VDD_FE	VSS_FE		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DR	VDD_DR		serialOut-[4]	serialOut+[4]		VSS_DG	VSS_DG	J
K	IN[12]	IN[13]		VDD_FE	VSS_FE		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS	VSS_DG	VSS	VSS_DR	VSS_DG	VDD_DG		VSS_DG	VSS_DG		serialOut-[2]	serialOut+[2]	K
L	IN[14]	IN[15]		VDD_FE	VSS_FE		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS	VSS	VDD_DG		serialOut-[0]	serialOut+[0]		VSS_DG	VSS_DG	L
M	IN[16]	IN[17]		VDD_FE	VSS_FE		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DR	VSS_DG	VDD_DG		VSS_DG	VSS_DG		serialOut-[1]	serialOut+[1]	M
N	IN[18]	IN[19]		VDD_FE	VSS_FE		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS	VSS_DG	VSS	VSS_DG	VSS_DR	VDD_DG		clkSOin-	clkSOin+		VSS_DG	VSS_DG	N
P	IN[20]	IN[21]		VDD_FE	VSS_FE		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VDD_DR		VSS_DG	VSS_DG		Hrstb-	Hrstb+	P
R	IN[22]	IN[23]		VDD_FE	VSS_FE		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS	VSS_DG	VSS	VSS	VSS	VDD_DG		clkBXin-	clkBXin+		VSS_DG	VSS_DG	R
T	IN[24]	VSS_FE		VDD_FE	VSS_FE2		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DR	VSS_DG	VDD_DG		VSS_DG	VSS_DG		trg-	trg+	T
U	IN[25]	N/C		VDD_FE	VSS_FE2													clkADCin-	clkADCin+		VSS_DG	VSS_DG	U
V	IN[26]	VSS_FE		VDD_FE	VSS	VSS_AD	VDD_AD	VDD_AD	VDD_AD	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DR	VDD_DR	VDD_DG	VSS_DG	VSS_DG		hb_trg-	hb_trg+	V
W	IN[27]	N/C		VSS	VSS_AD	VSS_AD	VDD_AD	VDD_AD	VDD_AD	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	bx_sync_trg-	bx_sync_trg+		VSS_DG	VSS_DG	W
Y	IN[28]	VSS_FE																			sdo1-	sdo1+	Y
AA	IN[29]	N/C	CTS	CG<0>	VDD_FE2	VDD_FE2	VDD_FE2	VREFP	VREFP	hadd[2]	hadd[0]	sme	sdi3	sen1	smo	TRST	TDI	TDO	N/C	sdo3-	N/C	VSS_DG	AA
AB	IN[30]	IN[31]	N/C	CG<1>	N/C	POL	VREFP	VREFP	VREFP	hadd[3]	hadd[1]	sen3	sdi1	PORin	PORout	TMS	TCLK	N/C	VSS_DG	sdo3+	N/C	N/C	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure 16: BGA ball layout (Top View)

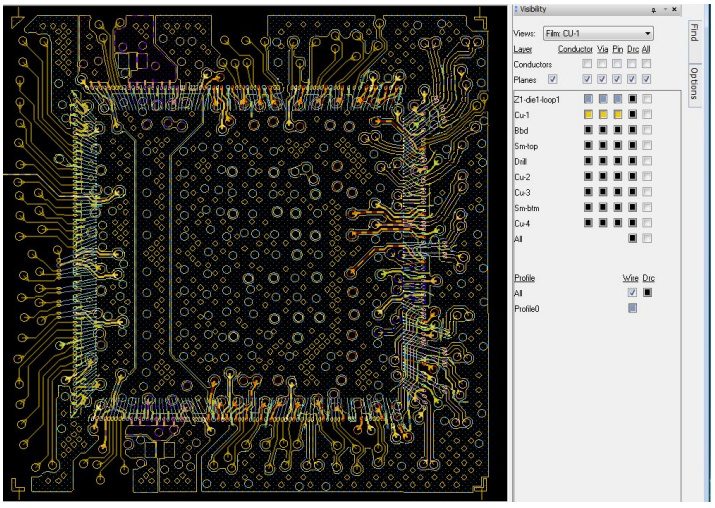


Figure 17: Layout of the first layer of the BGA substrate. Bond diagram is superimposed

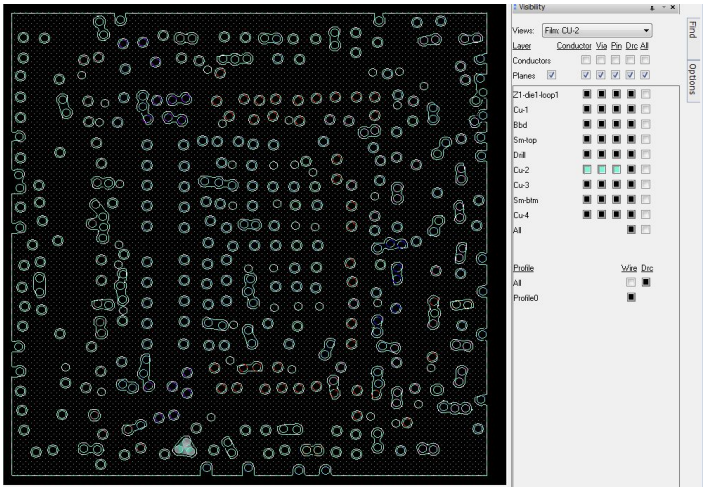


Figure 18: Layout of the 2nd layer of the BGA substrate, a pure GND plane

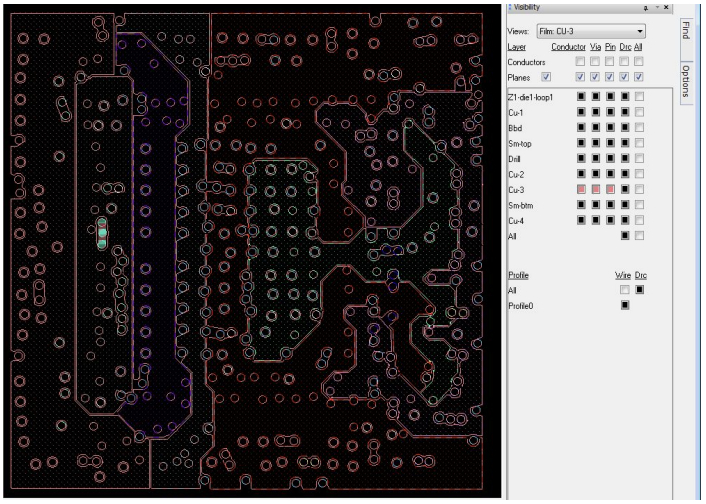


Figure 19: Layout of the 3rd layer of the BGA substrate. The presence of different domains is visible

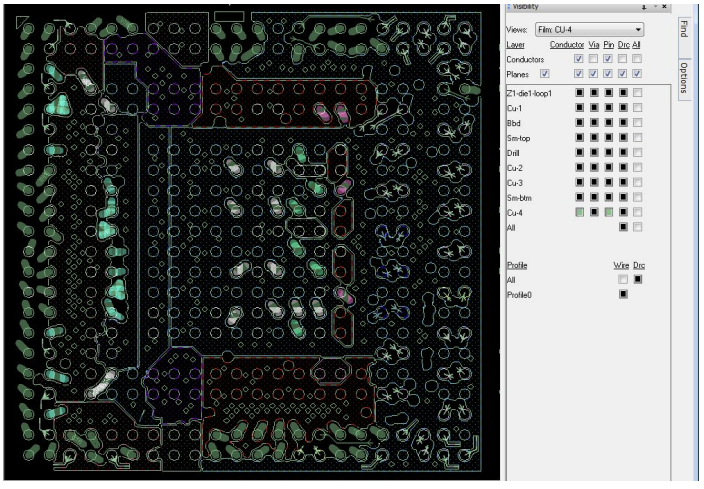


Figure 20: Layout of the 4th layer of the BGA substrate. Power domains separation is clearly visible (different colors).

4.2. Pinout

All input pins must be driven by a valid logic level: 0 < “logic zero” < 0.2 V or 1.1 < “logic one” < 1.3 V. Unused single-ended input pins should be tied high or low through a resistor (the same resistor can serve many pins). Differential inputs must be set to “0” or “1” by tying the non-inverting input low/high and the inverting input high/low respectively. The method to tie each input at low/high of a differential signal is the same as for the single-ended inputs. Output pins can be left floating. Pins marked N/C are unconnected in the package.

Table 23: Pinout part 1

Ball	Netname	Domain	IO type	Direction	Speed	Description
A1	IN[1]	Analog	Analog	in	0	Analog channel 1
A2	IN[0]	Analog	Analog	in	0	Analog channel 0
A3	N/C	-	-	-	-	Not connected
A4	V450	Analog	Power	in/out	0	Bandgap voltage reference (450mV)
A5	V600	Analog	Power	in/out	0	Bandgap voltage reference (600mV)
A6	V750	Analog	Power	in/out	0	Bandgap voltage reference (750mV)
A7	VREFP	Analog	Power	in	0	Voltage reference p
A8	VREFP	Analog	Power	in	0	Voltage reference p
A9	VREFP	Analog	Power	in	0	Voltage reference p
A10	clk_config[3]	Digital	Static	in	Static	Clock configuration
A11	clk_config[4]	Digital	Static	in	Static	Clock configuration
A12	clk_config[5]	Digital	Static	in	Static	Clock configuration
A13	VSS_DG	Digital	Power	in	0	Digital ground
A14	sclk	Digital	CMOS	in	20MHz	Scanchain test clock
A15	sen4	Digital	CMOS	in	20MHz	Scanchain test Scan Enable
A16	sen2	Digital	CMOS	in	20MHz	Scanchain test Scan Enable
A17	sen0	Digital	CMOS	in	20MHz	Scanchain test Scan Enable
A18	N/C	-	-	-	-	Not connected
A19	N/C	-	-	-	-	Not connected
A20	sdo4-	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
A21	N/C	-	-	-	-	Not connected
A22	sdo2-	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
B1	IN[2]	Analog	Analog	in	0	Analog channel 2
B2	N/C	-	-	-	-	Not connected
B3	VDD_FE2	Analog	Power	in	0	Analog core voltage SS and output buffer
B4	VDD_FE2	Analog	Power	in	0	Analog core voltage SS and output buffer
B5	VDD_AD	Analog	Power	in	0	ADC supply voltage
B6	VDD_AD	Analog	Power	in	0	ADC supply voltage
B7	VDD_AD	Analog	Power	in	0	ADC supply voltage
B8	VREFP	Analog	Power	in	0	Voltage reference p
B9	VREFP	Analog	Power	in	0	Voltage reference p
B10	clk_config[0]	Digital	Static	in	Static	Clock configuration
B11	clk_config[1]	Digital	Static	in	Static	Clock configuration
B12	clk_config[2]	Digital	Static	in	Static	Clock configuration
B13	VSS_DG	Digital	Power	in	0	Digital ground
B14	clk_config[6]	Digital	Static	in	Static	Clock configuration (Internal DSP Clock Gatting)
B15	TME	Digital	CMOS	in	Static	Scanchain test – TEST MODE EN
B16	sdi4	Digital	CMOS	in	20MHz	Scanchain test Scan In
B17	sdi2	Digital	CMOS	in	20MHz	Scanchain test Scan In
B18	sdi0	Digital	CMOS	in	20MHz	Scanchain test Scan In
B19	N/C	-	-	-	-	Not connected
B20	sdo4+	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
B21	N/C	-	-	-	-	Not connected
B22	sdo2+	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS

Table 24: Pinout part 2

Ball	Netname	Domain	IO type	Direction	Speed	Description
C1	IN[3]	Analog	Analog	in	0	Analog channel 3
C2	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
C21	sdo0-	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
C22	sdo0+	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
D1	IN[4]	Analog	Analog	in	0	Analog channel 4
D2	N/C	-	-	-	-	Not connected
D4	VSS	Analog/Digital	Power	in	0	PADRING ground
D5	VSS_AD	Analog	Power	in	0	ADC supply ground
D6	VSS_AD	Analog	Power	in	0	ADC supply ground
D7	VDD_AD	Analog	Power	in	0	ADC supply voltage
D8	VDD_AD	Analog	Power	in	0	ADC supply voltage
D9	VDD_AD	Analog	Power	in	0	ADC supply voltage
D10	VDD_DG	Digital	Power	in	0	Digital core voltage
D11	VDD_DG	Digital	Power	in	0	Digital core voltage
D12	VDD_DG	Digital	Power	in	0	Digital core voltage
D13	VDD_DG	Digital	Power	in	0	Digital core voltage
D14	VDD_DG	Digital	Power	in	0	Digital core voltage
D15	VDD_DG	Digital	Power	in	0	Digital core voltage
D16	VDD_DG	Digital	Power	in	0	Digital core voltage
D17	VDD_DG	Digital	Power	in	0	Digital core voltage
D18	VSS_DG	Digital	Power	in	0	Digital ground
D19	VSS_DG	Digital	Power	in	0	Digital ground
D21	sda_o	Digital	I2C	in/out	1MHz	I2C data
D22	scl	Digital	I2C	in	1MHz	I2C clock
E1	IN[5]	Analog	Analog	in	0	Analog channel 5
E2	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
E4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
E5	VSS	Analog/Digital	Power	in	0	PADRING ground
E6	VSS_AD	Analog	Power	in	0	ADC supply ground
E7	VDD_AD	Analog	Power	in	0	ADC supply voltage
E8	VDD_AD	Analog	Power	in	0	ADC supply voltage
E9	VDD_AD	Analog	Power	in	0	ADC supply voltage
E10	VDD_DG	Digital	Power	in	0	Digital core voltage
E11	VDD_DG	Digital	Power	in	0	Digital core voltage
E12	VDD_DG	Digital	Power	in	0	Digital core voltage
E13	VDD_DG	Digital	Power	in	0	Digital core voltage
E14	VDD_DG	Digital	Power	in	0	Digital core voltage
E15	VDD_DR	Digital	Power	in	0	Digital SLVS drivers voltage
E16	VDD_DR	Digital	Power	in	0	Digital SLVS drivers voltage
E17	VDD_DG	Digital	Power	in	0	Digital core voltage
E18	NBflowstop_in-	Digital	SLVS	in	160MHz	Stop neighbour data in n
E19	NBflowstop_in+	Digital	SLVS	in	160MHz	Stop neighbour data in p
E21	VSS_DG	Digital	Power	in	0	Digital ground
E22	VSS_DG	Digital	Power	in	0	Digital ground

Table 25: Pinout part 3

Ball	Netname	Domain	IO type	Direction	Speed	Description
F1	IN[6]	Analog	Analog	in	0	Analog channel 6
F2	N/C	-	-	-	-	Not connected
F4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
F5	VSS_FE2	Analog	Power	in	0	Analog ground SS and output buffer
F18	VSS_DG	Digital	Power	in	0	Digital ground
F19	VSS_DG	Digital	Power	in	0	Digital ground
F21	dinN-	Digital	SLVS	in	160MHz	Neigbour chip data n
F22	dinN+	Digital	SLVS	in	160MHz	Neigbour chip data p
G1	IN[7]	Analog	Analog	in	0	Analog channel 7
G2	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
G4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
G5	VSS_FE2	Analog	Power	in	0	Analog ground SS and output buffer
G7	VSS_AD	Analog	Power	in	0	ADC supply ground
G8	VSS_DG	Digital	Power	in	0	Digital ground
G9	VSS_DG	Digital	Power	in	0	Digital ground
G10	VSS_DG	Digital	Power	in	0	Digital ground
G11	VSS_DG	Digital	Power	in	0	Digital ground
G12	VSS_DG	Digital	Power	in	0	Digital ground
G13	VSS_DG	Digital	Power	in	0	Digital ground
G14	VSS_DR	Digital	Power	in	0	Digital SLVS drivers ground
G15	VSS_DG	Digital	Power	in	0	Digital ground
G16	VDD_DG	Digital	Power	in	0	Digital core voltage
G18	NBflowstop_out_SO5-	Digital	SLVS	out	160MHz	Stop neighbour data out or serial data link 5 n
G19	NBflowstop_out_SO5+	Digital	SLVS	out	160MHz	Stop neighbour data out or serial data link 5 p
G21	VSS_DG	Digital	Power	in	0	Digital ground
G22	VSS_DG	Digital	Power	in	0	Digital ground
H1	IN[8]	Analog	Analog	in	0	Analog channel 8
H2	IN[9]	Analog	Analog	in	0	Analog channel 9
H4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
H5	VSS_FE2	Analog	Power	in	0	Analog ground SS and output buffer
H7	VSS_AD	Analog	Power	in	0	ADC supply ground
H8	VSS_DG	Digital	Power	in	0	Digital ground
H9	VSS_DG	Digital	Power	in	0	Digital ground
H10	VSS_DG	Digital	Power	in	0	Digital ground
H11	VSS	Analog/Digital	Power	in	0	PADRING ground
H12	VSS_DG	Digital	Power	in	0	Digital ground
H13	VSS	Analog/Digital	Power	in	0	PADRING ground
H14	VSS	Analog/Digital	Power	in	0	PADRING ground
H15	VSS	Analog/Digital	Power	in	0	PADRING ground
H16	VDD_DG	Digital	Power	in	0	Digital core voltage
H18	VSS_DG	Digital	Power	in	0	Digital ground
H19	VSS_DG	Digital	Power	in	0	Digital ground
H21	serialOut-[3]	Digital	SLVS	out	160MHz	Serial data link 3 n
H22	serialOut+[3]	Digital	SLVS	out	160MHz	Serial data link 3 p

Table 26: Pinout part 4

Ball	Netname	Domain	IO type	Direction	Speed	Description
J1	IN[10]	Analog	Analog	in	0	Analog channel 10
J2	IN[11]	Analog	Analog	in	0	Analog channel 11
J4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
J5	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
J7	VSS_AD	Analog	Power	in	0	ADC supply ground
J8	VSS_DG	Digital	Power	in	0	Digital ground
J9	VSS_DG	Digital	Power	in	0	Digital ground
J10	VSS_DG	Digital	Power	in	0	Digital ground
J11	VSS_DG	Digital	Power	in	0	Digital ground
J12	VSS_DG	Digital	Power	in	0	Digital ground
J13	VSS_DG	Digital	Power	in	0	Digital ground
J14	VSS_DG	Digital	Power	in	0	Digital ground
J15	VSS_DR	Digital	Power	in	0	Digital SLVS drivers ground
J16	VDD_DR	Digital	Power	in	0	Digital SLVS drivers voltage
J18	serialOut-[4]	Digital	SLVS	out	160MHz	Serial data link 4 n
J19	serialOut+[4]	Digital	SLVS	out	160MHz	Serial data link 4 p
J21	VSS_DG	Digital	Power	in	0	Digital ground
J22	VSS_DG	Digital	Power	in	0	Digital ground
K1	IN[12]	Analog	Analog	in	0	Analog channel 12
K2	IN[13]	Analog	Analog	in	0	Analog channel 13
K4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
K5	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
K7	VSS_AD	Analog	Power	in	0	ADC supply ground
K8	VSS_DG	Digital	Power	in	0	Digital ground
K9	VSS_DG	Digital	Power	in	0	Digital ground
K10	VSS_DG	Digital	Power	in	0	Digital ground
K11	VSS	Analog/Digital	Power	in	0	PADRING ground
K12	VSS_DG	Digital	Power	in	0	Digital ground
K13	VSS	Analog/Digital	Power	in	0	PADRING ground
K14	VSS_DR	Digital	Power	in	0	Digital SLVS drivers ground
K15	VSS_DG	Digital	Power	in	0	Digital ground
K16	VDD_DG	Digital	Power	in	0	Digital core voltage
K18	VSS_DG	Digital	Power	in	0	Digital ground
K19	VSS_DG	Digital	Power	in	0	Digital ground
K21	serialOut-[2]	Digital	SLVS	out	160MHz	Serial data link 2 n
K22	serialOut+[2]	Digital	SLVS	out	160MHz	Serial data link 2 p
L1	IN[14]	Analog	Analog	in	0	Analog channel 14
L2	IN[15]	Analog	Analog	in	0	Analog channel 15
L4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
L5	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
L7	VSS_AD	Analog	Power	in	0	ADC supply ground
L8	VSS_DG	Digital	Power	in	0	Digital ground
L9	VSS_DG	Digital	Power	in	0	Digital ground
L10	VSS_DG	Digital	Power	in	0	Digital ground

Table 27: Pinout part 5

Ball	Netname	Domain	IO type	Direction	Speed	Description
M1	IN[16]	Analog	Analog	in	0	Analog channel 16
M2	IN[17]	Analog	Analog	in	0	Analog channel 17
M4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
M5	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
M7	VSS_AD	Analog	Power	in	0	ADC supply ground
M8	VSS_DG	Digital	Power	in	0	Digital ground
M9	VSS_DG	Digital	Power	in	0	Digital ground
M10	VSS_DG	Digital	Power	in	0	Digital ground
M11	VSS_DG	Digital	Power	in	0	Digital ground
M12	VSS_DG	Digital	Power	in	0	Digital ground
M13	VSS_DG	Digital	Power	in	0	Digital ground
M14	VSS_DR	Digital	Power	in	0	Digital SLVS drivers ground
M15	VSS_DG	Digital	Power	in	0	Digital ground
M16	VDD_DG	Digital	Power	in	0	Digital core voltage
M18	VSS_DG	Digital	Power	in	0	Digital ground
M19	VSS_DG	Digital	Power	in	0	Digital ground
M21	serialOut-[1]	Digital	SLVS	out	160MHz	Serial data link 1 n
M22	serialOut+[1]	Digital	SLVS	out	160MHz	Serial data link 1 p
N1	IN[18]	Analog	Analog	in	0	Analog channel 18
N2	IN[19]	Analog	Analog	in	0	Analog channel 19
N4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
N5	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
N7	VSS_AD	Analog	Power	in	0	ADC supply ground
N8	VSS_DG	Digital	Power	in	0	Digital ground
N9	VSS_DG	Digital	Power	in	0	Digital ground
N10	VSS_DG	Digital	Power	in	0	Digital ground
N11	VSS	Analog/Digital	Power	in	0	PADRING ground
N12	VSS_DG	Digital	Power	in	0	Digital ground
N13	VSS	Analog/Digital	Power	in	0	PADRING ground
N14	VSS_DG	Digital	Power	in	0	Digital ground
N15	VSS_DR	Digital	Power	in	0	Digital SLVS drivers ground
N16	VDD_DG	Digital	Power	in	0	Digital core voltage
N18	clkSOin-	Digital	SLVS	in	320MHz	Serial out clock n
N19	clkSOin+	Digital	SLVS	in	320MHz	Serial out clock p
N21	VSS_DG	Digital	Power	in	0	Digital ground
N22	VSS_DG	Digital	Power	in	0	Digital ground

Table 28: Pinout part 6

Ball	Netname	Domain	IO type	Direction	Speed	Description
P1	IN[20]	Analog	Analog	in	0	Analog channel 20
P2	IN[21]	Analog	Analog	in	0	Analog channel 21
P4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
P5	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
P7	VSS_AD	Analog	Power	in	0	ADC supply ground
P8	VSS_DG	Digital	Power	in	0	Digital ground
P9	VSS_DG	Digital	Power	in	0	Digital ground
P10	VSS_DG	Digital	Power	in	0	Digital ground
P11	VSS_DG	Digital	Power	in	0	Digital ground
P12	VSS_DG	Digital	Power	in	0	Digital ground
P13	VSS_DG	Digital	Power	in	0	Digital ground
P14	VSS_DG	Digital	Power	in	0	Digital ground
P15	VSS_DG	Digital	Power	in	0	Digital ground
P16	VDD_DR	Digital	Power	in	0	Digital SLVS drivers voltage
P18	VSS_DG	Digital	Power	in	0	Digital ground
P19	VSS_DG	Digital	Power	in	0	Digital ground
P21	Hrstb-	Digital	SLVS	in	160MHz	Reset n
P22	Hrstb+	Digital	SLVS	in	160MHz	Reset p
R1	IN[22]	Analog	Analog	in	0	Analog channel 22
R2	IN[23]	Analog	Analog	in	0	Analog channel 23
R4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
R5	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
R7	VSS_AD	Analog	Power	in	0	ADC supply ground
R8	VSS_DG	Digital	Power	in	0	Digital ground
R9	VSS_DG	Digital	Power	in	0	Digital ground
R10	VSS_DG	Digital	Power	in	0	Digital ground
R11	VSS	Analog/Digital	Power	in	0	PADRING ground
R12	VSS_DG	Digital	Power	in	0	Digital ground
R13	VSS	Analog/Digital	Power	in	0	PADRING ground
R14	VSS	Analog/Digital	Power	in	0	PADRING ground
R15	VSS	Analog/Digital	Power	in	0	PADRING ground
R16	VDD_DG	Digital	Power	in	0	Digital core voltage
R18	clkBXin-	Digital	SLVS	in	40MHz	Bunchcrossing clock n
R19	clkBXin+	Digital	SLVS	in	40MHz	Bunchcrossing clock p
R21	VSS_DG	Digital	Power	in	0	Digital ground
R22	VSS_DG	Digital	Power	in	0	Digital ground

Table 29: Pinout part 7

Ball	Netname	Domain	IO type	Direction	Speed	Description
T1	IN[24]	Analog	Analog	in	0	Analog channel 24
T2	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
T4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
T5	VSS_FE2	Analog	Power	in	0	Analog ground SS and output buffer
T7	VSS_AD	Analog	Power	in	0	ADC supply ground
T8	VSS_DG	Digital	Power	in	0	Digital ground
T9	VSS_DG	Digital	Power	in	0	Digital ground
T10	VSS_DG	Digital	Power	in	0	Digital ground
T11	VSS_DG	Digital	Power	in	0	Digital ground
T12	VSS_DG	Digital	Power	in	0	Digital ground
T13	VSS_DG	Digital	Power	in	0	Digital ground
T14	VSS_DR	Digital	Power	in	0	Digital SLVS drivers ground
T15	VSS_DG	Digital	Power	in	0	Digital ground
T16	VDD_DG	Digital	Power	in	0	Digital core voltage
T18	VSS_DG	Digital	Power	in	0	Digital ground
T19	VSS_DG	Digital	Power	in	0	Digital ground
T21	trg-	Digital	SLVS	in	160MHz	Event trigger n
T22	trg+	Digital	SLVS	in	160MHz	Event trigger p
U1	IN[25]	Analog	Analog	in	0	Analog channel 25
U2	N/C	-	-	-	-	Not connected
U4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
U5	VSS_FE2	Analog	Power	in	0	Analog ground SS and output buffer
U18	clkADCin-	Digital	SLVS	in	20MHz	ADC clock n
U19	clkADCin+	Digital	SLVS	in	20MHz	ADC clock p
U21	VSS_DG	Digital	Power	in	0	Digital ground
U22	VSS_DG	Digital	Power	in	0	Digital ground
V1	IN[26]	Analog	Analog	in	0	Analog channel 26
V2	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
V4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
V5	VSS	Analog/Digital	Power	in	0	PADRING ground
V6	VSS_AD	Analog	Power	in	0	ADC supply ground
V7	VDD_AD	Analog	Power	in	0	ADC supply voltage
V8	VDD_AD	Analog	Power	in	0	ADC supply voltage
V9	VDD_AD	Analog	Power	in	0	ADC supply voltage
V10	VDD_DG	Digital	Power	in	0	Digital core voltage
V11	VDD_DG	Digital	Power	in	0	Digital core voltage
V12	VDD_DG	Digital	Power	in	0	Digital core voltage
V13	VDD_DG	Digital	Power	in	0	Digital core voltage
V14	VDD_DG	Digital	Power	in	0	Digital core voltage
V15	VDD_DR	Digital	Power	in	0	Digital SLVS drivers voltage
V16	VDD_DR	Digital	Power	in	0	Digital SLVS drivers voltage
V17	VDD_DG	Digital	Power	in	0	Digital core voltage
V18	VSS_DG	Digital	Power	in	0	Digital ground
V19	VSS_DG	Digital	Power	in	0	Digital ground
V21	hb_trg-	Digital	SLVS	in	160MHz	Heartbeat trigger n
V22	hb_trg+	Digital	SLVS	in	160MHz	Heartbeat trigger p

Table 30: Pinout part 8

Ball	Netname	Domain	IO type	Direction	Speed	Description
W1	IN[27]	Analog	Analog	in	0	Analog channel 27
W2	N/C	-	-	-	-	Not connected
W4	VSS	Analog/Digital	Power	in	0	PADRING ground
W5	VSS_AD	Analog	Power	in	0	ADC supply ground
W6	VSS_AD	Analog	Power	in	0	ADC supply ground
W7	VDD_AD	Analog	Power	in	0	ADC supply voltage
W8	VDD_AD	Analog	Power	in	0	ADC supply voltage
W9	VDD_AD	Analog	Power	in	0	ADC supply voltage
W10	VDD_DG	Digital	Power	in	0	Digital core voltage
W11	VDD_DG	Digital	Power	in	0	Digital core voltage
W12	VDD_DG	Digital	Power	in	0	Digital core voltage
W13	VDD_DG	Digital	Power	in	0	Digital core voltage
W14	VDD_DG	Digital	Power	in	0	Digital core voltage
W15	VDD_DG	Digital	Power	in	0	Digital core voltage
W16	VDD_DG	Digital	Power	in	0	Digital core voltage
W17	VDD_DG	Digital	Power	in	0	Digital core voltage
W18	bx_sync_trg-	Digital	SLVS	in	160MHz	Bunchcrossing counter sync n
W19	bx_sync_trg+	Digital	SLVS	in	160MHz	Bunchcrossing counter sync p
W21	VSS_DG	Digital	Power	in	0	Digital ground
W22	VSS_DG	Digital	Power	in	0	Digital ground
Y1	IN[28]	Analog	Analog	in	0	Analog channel 28
Y2	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
Y21	sdo1-	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
Y22	sdo1+	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
AA1	IN[29]	Analog	Analog	in	0	Analog channel 29
AA2	N/C	-	-	-	-	Not connected
AA3	CTS	Analog	Static	in	Static	Shaping configuration
AA4	CG<0>	Analog	Static	in	Static	Gain configuration
AA5	VDD_FE2	Analog	Power	in	0	Analog core voltage SS and output buffer
AA6	VDD_FE2	Analog	Power	in	0	Analog core voltage SS and output buffer
AA7	VDD_FE2	Analog	Power	in	0	Analog core voltage SS and output buffer
AA8	VREFP	Analog	Power	in	0	Voltage reference p
AA9	VREFP	Analog	Power	in	0	Voltage reference p
AA10	hadd[2]	Digital	Static	in	Static	Chip address
AA11	hadd[0]	Digital	Static	in	Static	Chip address
AA12	sme	Digital	CMOS	in	Static	MEM Test En
AA13	sdi3	Digital	CMOS	in	20MHz	Scanchain test Scan In
AA14	sen1	Digital	CMOS	in	20MHz	Scanchain test Scan Enable
AA15	smo	Digital	CMOS	out	20MHz	MEM Test Out
AA16	TRST	Digital	CMOS	in	20MHz	JTAG
AA17	TDI	Digital	CMOS	in	20MHz	JTAG
AA18	TDO	Digital	CMOS	out	20MHz	JTAG
AA19	N/C	-	-	-	-	Not connected
AA20	sdo3-	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
AA21	N/C	-	-	-	-	Not connected
AA22	VSS_DG	Digital	Power	in	0	Digital ground

Table 31: Pinout part 9

Ball	Netname	Domain	IO type	Direction	Speed	Description
AB1	IN[30]	Analog	Analog	in	0	Analog channel 30
AB2	IN[31]	Analog	Analog	in	0	Analog channel 31
AB3	N/C	-	-	-	-	Not connected
AB4	CG<1>	Analog	Static	in	Static	Gain configuration
AB5	N/C	-	-	-	-	Not connected
AB6	POL	Analog	Static	in	Static	Polarity configuration
AB7	VREFP	Analog	Power	in	0	Voltage reference p
AB8	VREFP	Analog	Power	in	0	Voltage reference p
AB9	VREFP	Analog	Power	in	0	Voltage reference p
AB10	hadd[3]	Digital	Static	in	Static	Chip address
AB11	hadd[1]	Digital	Static	in	Static	Chip address
AB12	sen3	Digital	CMOS	in	20MHz	Scanchain test Scan Enable
AB13	sdi1	Digital	CMOS	in	20MHz	Scanchain test Scan In
AB14	PORin	Digital	CMOS	in	Static	Power on reset input
AB15	PORout	Digital	CMOS	out	Static	Power on reset output
AB16	TMS	Digital	CMOS	in	20MHz	JTAG
AB17	TCLK	Digital	CMOS	in	20MHz	JTAG
AB18	N/C	-	-	-	-	Not connected
AB19	VSS_DG	Digital	Power	in	0	Digital ground
AB20	sdo3+	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
AB21	N/C	-	-	-	-	Not connected
AB22	N/C	-	-	-	-	Not connected

Application Notes

A.1. Power-on Recommendations

The correct power-up procedure for SAMPA V5 chip is to first ramp up the power supply voltage, then wait approximately 50ms for the PoR (Power-on Reset) flag, and only after the PoR flag the system clock should be applied to the IC.

The Power-on Reset flag is available through the open-drain output pin AB15.

Should the user choose to use the internal PoR flag, package pins AB15 (PORout) and AB14 (PORin) should be externally connected. In case the user prefer to use an external PoR flag, it should be connected to pin AB14. Take note that pin AB14 is a CMOS active LOW level input signal with internal pull-up. Regarding the use of an external PoR flag, a time delay of at least 40ms must be waited after the power supply power-up.

If the system clock is fed into the SAMPA V5 ASIC before the Power on Reset, the system may start to operate in an irreversible incorrect state. In order to avoid such behavior, the system clock should only be enabled to the chip after the PoR flag.

The ideal power-on timing diagram is shown in figure A.1, it represents the power supply ramp up occurring first, the PoR flag occurring after around 50 ms, and only then the system clock may start.

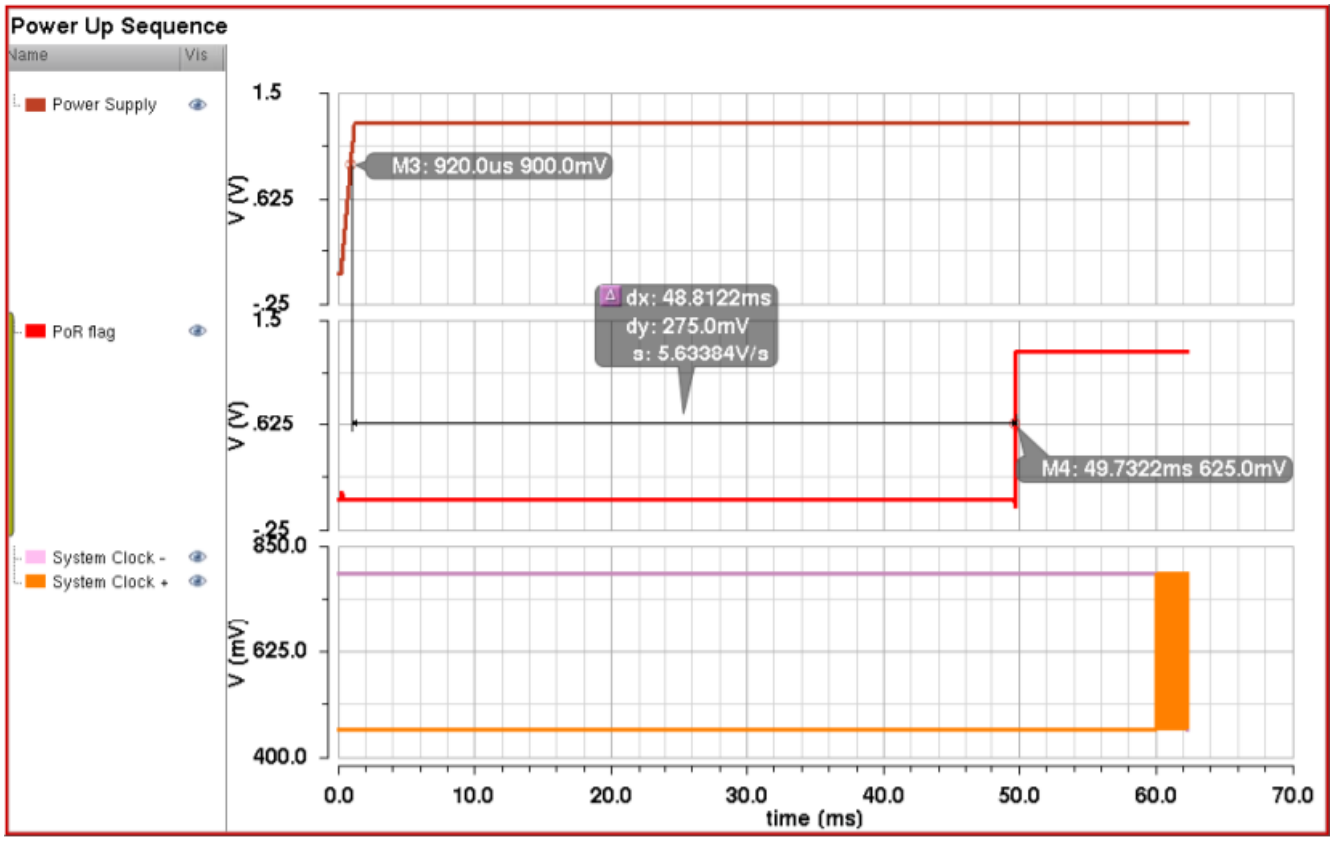


Figure A.1. Ideal SAMPA V5 ASIC Power Up Sequence.