PrPMC800/800ET Processor PMC Module

Programmer's Reference Guide

PRPMC800A/PG3

September 2003 Edition

Printed in the United States of America.

Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. If the equipment is supplied with a three-conductor AC power cable, the power cable must be plugged into an approved three-contact electrical outlet, with the grounding wire (green/yellow) reliably connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards and local electrical regulatory codes.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in any explosive atmosphere such as in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment could result in an explosion and cause injury or damage.

Keep Away From Live Circuits Inside the Equipment.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Service personnel should not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, such personnel should always disconnect power and discharge circuits before touching components.

Use Caution When Exposing or Handling a CRT.

Breakage of a Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, do not handle the CRT and avoid rough handling or jarring of the equipment. Handling of a CRT should be done only by qualified service personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that all safety features are maintained.

Observe Warnings in Manual.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

Warning

To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

Flammability

All Motorola PWBs (printed wiring boards) are manufactured with a flammability rating of 94V-0 by UL-recognized manufacturers.

EMI Caution

Caution

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used with adequate EMI protection.

Lithium Battery Caution

This product contains a lithium battery to power the clock and calendar circuitry.

Caution

Danger of explosion if battery is replaced incorrectly. Replace battery only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Attention

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabricant.

Vorsicht

Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch denselben oder einen vom Hersteller empfohlenen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.

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> EN55022 “Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment”; this product tested to Equipment Class A
>
> EN55024 “Information Technology Equipment-Immunity characteristics-Limits and methods of measurement”

Board products are tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a CE-marked system will maintain the required EMC/safety performance.

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About This Manual

The *PrPMC800/800ET Programmer's Reference Guide* provides specific programming instructions and memory map as well as selected information on hardware features. This document is intended for use in conjunction with the *Harrier ASIC Programmer's Reference Guide*, which provides a large portion of the programming capability for the PrPMC800/800ET.

Information in this manual applies to Motorola boards that are compatible with the PowerPC™ instruction set architecture and that use PPCBug as their resident debugger program. The majority of these boards, including most Processor PMC, VME, CompactPCI® and ATX form factors, are equipped with PPCBug.

This document is limited to the general programming and memory map information unique to this product.

The following table lists the various model numbers and configurations for the PrPMC800/800ET. Note that some of the models listed below qualify as Class B devices. If you require a Class B device, contact your Motorola Sales Representative for specific models and configurations that meet those requirements

PrPMC800/800ET Models/Configurations

Assembly Number 01-W3649	Model Number PrPMC800	Processor / Speed	L2 Cache	Memory	Ethernet	PCI Bus Speed
F05	-5251	MPC750 Class/ 450 MHz	1MB	128MB	Front	33 MHz
F06	-5261	MPC750 Class/ 450 MHz	1MB	256MB	Front	33 MHz
F07	-5271	MPC750 Class/ 450 MHz	1MB	512MB	Front	33 MHz
F14	-1241	MPC7410/ 450 MHz	2MB	64MB	Front	33 MHz
F15	-1251	MPC7410/ 450 MHz	2MB	128MB	Front	33 MHz
F16	-1261	MPC7410/ 450 MHz	2MB	256MB	Front	33 MHz
F17	-1271	MPC7410/ 450 MHz	2MB	512MB	Front	33 MHz
F25	-5259	MPC750 Class/ 450 MHz	1MB	128MB	Rear	33 MHz
F26	-5269	MPC750 Class/ 450 MHz	1MB	256MB	Rear	33 MHz
F27	-5279	MPC750 Class/ 450 MHz	1MB	512MB	Rear	33 MHz
F35	-1259	MPC7410/ 450 MHz	2MB	128MB	Rear	33 MHz
F36	-1269	MPC7410/ 450 MHz	2MB	256MB	Rear	33 MHz
* Industrial temperature						

PrPMC800/800ET Models/Configurations (Continued)

Assembly Number 01-W3649	Model Number PrPMC800	Processor / Speed	L2 Cache	Memory	Ethernet	PCI Bus Speed
F37	-1279	MPC7410/ 450 MHz	2MB	512MB	Rear	33 MHz
F45	-6251	MPC750 Class/ 450 MHz	1MB	128MB	None	66 MHz Capable
F46	-6261	MPC750 Class/ 450 MHz	1MB	256MB	None	66 MHz Capable
F47	-6271	MPC750 Class/ 450 MHz	1MB	512MB	None	66 MHz Capable
F55	-2251	MPC7410/ 450 MHz	2MB	128MB	None	66 MHz Capable
F56	-2261	MPC7410/ 450 MHz	2MB	256MB	None	66 MHz Capable
F57	-2271	MPC7410/ 450 MHz	2MB	512MB	None	66 MHz Capable
F65	-1159	MPC7410/ 400 MHz	1MB	128MB	Rear	33 MHz
F66	-1169	MPC7410/ 400 MHz	1MB	256MB	Rear	33 MHz
F87A	-1361*	MPC7410/500 MHz	2MB	256MB	Front	33MHz Capable
F88A	-1369*	MPC7410/500 MHz	2MB	256MB	Rear	33MHz Capable
F89A	-2361*	MPC7410/500 MHz	2MB	256MB	None	66MHz Capable
F95	-2151	MPC7410/ 400 MHz	1MB	128MB	None	66 MHz Capable
F96	-2161	MPC7410/ 400 MHz	1MB	256MB	None	66 MHz Capable

* Industrial temperature

Summary of Changes

The following changes have been made to this manual.

Date	Doc. Rev.	Changes
08/2003	PrPMC800A/PG3	Updated processor description of core frequencies. Updated Ethernet description to include 82551IT. Updated Appendix B, *Related Documentation*.
01/2002	PRPMC800A/PG2	In conjunction with the introduction of new model numbers to reflect the availability of low-power board configurations, selected items in Chapter 1, *Board Description and Memory Maps* and Appendix A, *PrPMC800/800ET VPD Reference Information* were updated as necessary.

Overview of Contents

Chapter 1, *Board Description and Memory Maps*, provides a general description of the PrPMC800/800ET including a summary of the basic features and architecture. It also includes a block diagram. The remainder of the chapter includes a description of the programming model unique to this product including memory maps, a discussion of the SDRAM interface, the flash interface, the PPC system bus functions, the PCI configuration space, the operating mode (monarch or non-monarch), and external registers.

Chapter 2, *Programming Details*, contains a section on PCI arbitration, reset sources, and Endian issues, including those with the processor/memory domain, MPIC's involvement and the PCI domain. It also includes error notification and handling information.

Appendix A, PrPMC800/800ET VPD Reference Information, provides a listing of all related Motorola and vendor documents, as well as related specifications.

Appendix B, *Appendix B, Related Documentation*, includes current Vital Product Data (VPD) and Serial Presence Detect (SPD) definitions.

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Conventions Used in This Manual

The following typographical conventions are used in this document:

bold

is used for user input that you type just as it appears. Bold is also used for commands, options and arguments to commands, and names of programs, directories and files.

italic

is used for names of variables to which you assign values. Italic is also used for comments in screen displays and examples, and to introduce new terms.

`courier`

is used for system output (for example, screen displays, reports), examples, and system prompts.

<**Enter**>, <**Return**> or <**CR**>

<**CR**> represents the carriage return or Enter key.

CTRL

represents the Control key. Execute control characters by pressing the Ctrl key and the letter simultaneously, for example, **Ctrl-d**.

|

separates two or more items from which to choose (one only)

[ ]

encloses an optional item that may not occur at all, or may occur once.

{ }

encloses an optional item that may not occur at all, or may occur one or more times.

A character precedes a data or address parameter to specify the numeric format, as follows (if not specified, the format is hexadecimal):

$	dollar	a hexadecimal character.
0x	Zero-x	
%	percent	a binary number.
&	ampersand	a decimal number.

Data and address sizes are defined as follows:

A *byte* is eight bits, numbered 0 through 7, with bit 0 being the least significant.

A *half-word* is 16 bits, numbered 0 through 15, with bit 0 being the least significant.

A *word* is 32 bits, numbered 0 through 31, with bit 0 being the least significant.

The MPU on the board is programmed to big-endian byte ordering. Any attempt to use little-endian byte ordering will immediately render the debugger unusable.

Note All references to processor bus support via the Harrier ASIC relate specifically to the MPC60x-class bus mode. They do not imply support of any other PowerPC-architecture bus mode.

Board Description and Memory Maps

1

Introduction

This chapter briefly describes the board-level hardware features of the PrPMC800/800ET processor modules. The chapter begins with a board-level overview and list of features. Next are memory maps, the major feature of this chapter.

Programmable registers in the PrPMC800/800ET series that reside in the Harrier ASIC are explained in the *Harrier ASIC Programmer's Reference Guide*. Appendix B, *Related Documentation* lists all related publications.

Overview

The PrPMC800/800ET Processor Module family, hereafter sometimes referred to simply as the PrPMC or the PrPMC800/800ET series, provides many standard features required by a computer system: MPC750-class, MPC7410, or MPC7410 (N) PowerPC-compatible processor, L2 cache, processor (MPC60x) bus to PCI Bridge, memory controller, asynchronous serial port, boot flash, and an Ethernet interface.

Feature Summary

There are several models based on the PrPMC800/800ET series architecture. For a description of the major board variants listed by model number, refer to the table in the *About this Manual* section of the *PrPMC800/800ET Processor PMC Installation and Use* guide. For a summary of the major features of these boards, refer to the following table.

Table 1-1. PrPMC800/800ET Features

Feature	Description
Processor	Single MPC750-class or MPC7410 processor Core frequencies of 450 MHz for MPC750-class, 450 MHz and 500 MHz for MPC7410, 400 MHz for MPC7410 (N) Bus clock frequency of 100 MHz Address and data bus parity
L2 Cache	Backside L2 Cache using pipeline burst-mode SRAMS: 1MB for MPC750-class and MPC7410 (N), 2MB for the MPC7410 Data bus parity
Flash Memory	Bank A: 32MB Soldered on-board flash using two 128 Mbit devices Bank B: Second bank of flash can be located on host board and accessed through the PMC P14 connector
SDRAM	Double-Bit-Error detect, Single-Bit-Error correct across 72 bits Single bank of 16-bit wide devices onboard provide 64MB, 128MB, or 256MB SDRAM
Memory Controller	Harrier's SMC (System Memory Controller)
PCI Host Bridge	Harrier's PHB (PCI Host Bridge)
Interrupt Controller	Harrier's MPIC (Multiprocessor Interrupt Controller)
PCI Interface	32/64-bit Data 33 MHz minimum, 66 MHz capable 3.3V/5V universal signaling interface P11, P12, P13 and P14 PMC connectors Address/data parity per PCI specification
Ethernet Interface	10BaseT/100BaseTX interface based on the Intel 82559ER/82551IT device AT93C46 SROM for 82559ER/82551IT configuration
SROM	Two 8Kb dual-address I^2C serial EEPROM devices for VPD, user configuration data One 256 byte standard I^2C serial EEPROM for memory SPD

Table 1-1. PrPMC800/800ET Features (Continued)

Feature	Description
Debug Support	Two 16550-compatible async serial ports with RS-232 interface Processor JTAG/COP interface RESET and ABORT signals Signals routed to 2mm header and PMC connector P14
Input Power Requirements	3.3V $\pm$ 5%

System Block Diagram

The general system block diagram for PrPMC800/800ET series appears in the following figure.

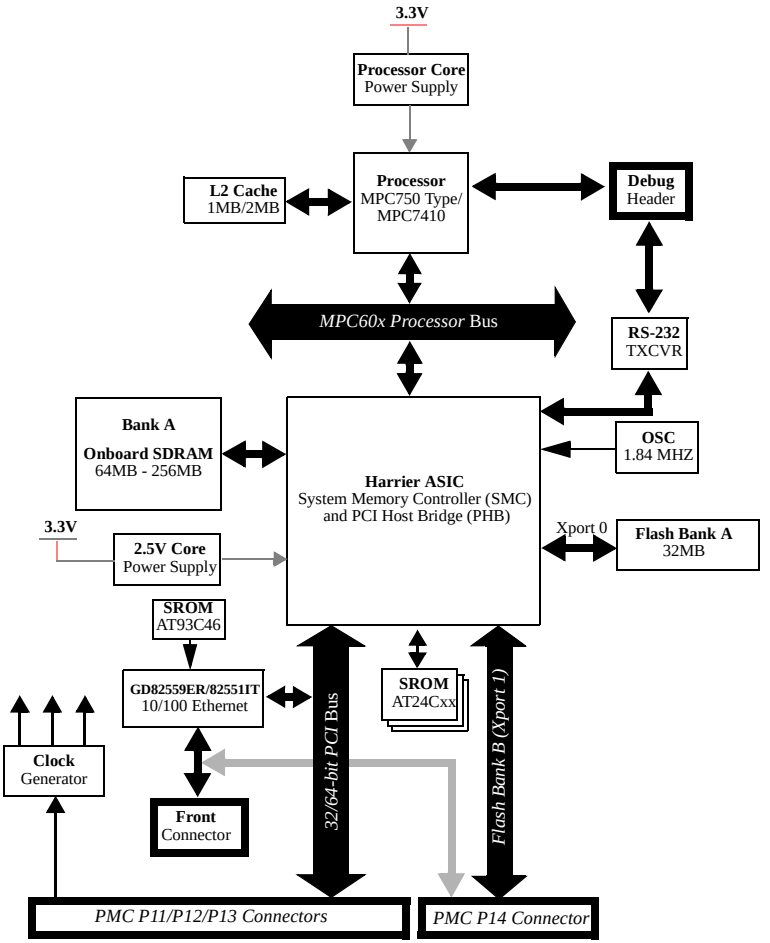

Figure 1-1. PrPMC800/800ET Series Block Diagram

Functional Description

The PrPMC800/800ET is a Motorola processor PMC module compatible with the PowerPlus III architecture. It consists of an MPC750-class, MPC7410, or MPC7410 (N) processor and L2 backside cache; a Harrier System Memory Controller (SMC)/PCI Host Bridge (PHB) ASIC; 32MB of flash memory; 64MB to 512MB of ECC-protected SDRAM on board with memory expansion capability; a 10BaseT/100BaseTX Ethernet controller; and a debug serial port.

The PrPMC800/800ET module interfaces to the host board PCI bus via the PMC P11, P12 and P13 connectors. These provide a 64-bit PCI interface (that is, 33 MHz/66 MHz capable) between the host board and the PrPMC800/800ET. The PrPMC800/800ET module draws +3.3V through the PMC connectors. The onboard Processor Core Power Supply derives the core voltage from the +3.3V power. The clock generator derives all of the required onboard clocks from the PCI clock input on P11.

The PrPMC800/800ET module has a 2mm header onboard to support module debug operations. This header provides the interface to the debug serial RS-232 port and an interface to the processor JTAG/COP port.

The PrPMC800/800ET module can function as a system controller (monarch mode) for the host board or as a slave processor (non-monarch) PMC, depending on the state of the MONARCH# signal from the PMC connector. When configured as the monarch, the PrPMC800/800ET enumerates the PCI bus as well as monitors and services the four PCI interrupts.

Programming Model

The following sections describe the memory maps for the PrPMC800/800ET series boards.

Processor Memory Maps

The processor memory map on the PrPMC800/800ET is controlled by the Harrier ASIC. The Harrier ASIC has flexible programming Map Decoder registers to customize the system to fit many different applications.

Default Processor Map

After a reset, the Harrier ASIC establishes the default processor memory map shown in the following table.

Table 1-2. Default Processor Memory Map

Processor Address		Size	Definition	Notes
Start	**End**			
0000 0000	7FFF FFFF	2G	Not mapped	
8000 0000	807F FFFF	8M	Harrier zero-based PCI/ISA I/O space	
8080 0000	80FF FFFF	8M	Reserved	
8100 0000	817F FFFF	8M	Reserved	
8180 0000	81FF FFFF	8M	Reserved	
8200 0000	FEEF FFFF	2G-49M 64K	Not mapped	
FEF0 0000	FEFE FFFF	1M-64K	Reserved	
FEFF 0000	FEFF 0FFF	4K	Harrier Control & Status (XCSR)	2
FEFF 1000	FEFF 1FFF	4K	Reserved	
FEFF 2000	FEFF 2FFF	4K	Reserved	
FEFF 3000	FEFF 3FFF	4K	Reserved	
FEFF 4000	FFEF FFFF	15M+48K	Not mapped	
FFF0 0000	FFFF FFFF	1M	Xport 0 (flash bank A), Xport 1 (flash bank B), or SDRAM alias.	1

Notes

1. The device that responds in this range is determined by the RVEN bits in the Xport attribute registers and the ENRV bit in the SDRAM control register. Depending on the bit settings, either SDRAM or flash may respond. The RVEN bits are set by the state of the BankB_SEL signal at power-up. The ENRV bit is set by software.
2. These address ranges are fixed within the Harrier ASIC. It is not possible to remap them within the physical memory map.

Suggested Processor Map

The following table describes a suggested memory map for the PrPMC800/800ET from the viewpoint of the processor. This memory map is neither CHRP nor PREP, although it has some CHRP similarities. The beginning of PCI memory space is determined by the end of DRAM rounded up to the nearest 256MB-boundary. For example, if memory was 128MB on the baseboard, the beginning of PCI memory would be rounded up to address 0x10000000 (256M). This is a suggested map only. Motorola-developed firmware and software will adhere to the mapping scheme shown, but end-user applications are free to select an alternate mapping.

Table 1-3. Memory Map Example

Processor Address		Size	Definition	Notes
Start	**End**			
0000 0000	top_dram-1	dram_size	System Memory (onboard SDRAM)	
top_dram	EFFF FFFF	3.75G – dram_size	PCI and/or VME memory space	4
F000 0000	FDFF FFFF	224M	Xport-0-based flash	5
FE00 0000	FEEF FFFF	15M	PCI/ISA I/O space	3
FEF0 0000	FEFE FFFF	1M-64K	Reserved	1
FEFF 0000	FEFF 0FFF	4K	Harrier XCSR registers	1
FEFF 1000	FEFF 1FFF	4K	Reserved	

Table 1-3. Memory Map Example (Continued)

Processor Address		Size	Definition	Notes
Start	**End**			
FEFF 2000	FEFF 2FFF	4K	Reserved	
FEFF 3000	FEFF 3FFF	4K	Reserved	
FEFF 4000	FEFF FFFF	48K	Reserved	
FF00 0000	FF03 FFFF	256K	Harrier MPIC registers	
FF04 0000	FF07 FFFF	256K	Reserved	
FF08 0000	FF0B FFFF	256K	Reserved	
FF0C 0000	FF0F FFFF	256K	Reserved	
FF10 0000	FF1F FFFF	1M	Reserved	
FF20 0000	FF2F FFFF	1M	Reserved	
FF30 0000	FF7F FFFF	6M	Reserved	
FF80 0000	FFEF FFFF	7M	Xport-1-based flash	5
FFF0 0000	FFFF FFFF	1M	Boot area (flash or SDRAM)	2

Notes

1. All address ranges except Harrier XCSR registers are configured by software.
2. The device responding here is determined by Xport RVEN bits and/or ENRV bit in SDRAM control register.
3. The only method to generate a PCI Interrupt Acknowledge cycle (8259 IACK) is to perform a read access to the Harrier's PIACK Register at 0xFEFF0210.
4. VME should be placed at top of PCI memory space.

5. Xport 0 is used for the “main” bank; Xport 1 is used for the boot flash (normally socketed parts). At least one flash bank must be implemented.

The following table shows the programmed values for the associated Harrier outbound translation registers for the suggested Processor Memory Map.

Table 1-4. Harrier XCSR Register Values for Suggested Memory Map

Address	Register Name	Register Value
FEFF 0220	OTAD0	X000 EFFF[X:1...8]
FEFF 0224	OTOF0 &OTAT0	0000 0782
FEFF 0228	OTAD1	0000 0000
FEFF 022C	OTOF1 & OTAT1	0000 0000
FEFF 0230	OTAD2	0000 0000
FEFF 0234	OTOF2 & OTAT2	0000 0000
FEFF 0238	OTAD3	FE00 FEEF
FEFF 023C	OTOF3 & OTAT3	0200 0780

Notes

1. Table assumes a single Harrier configuration.
2. OTAD0 must be dynamically determined based on size of SDRAM present.
3. PCI configuration address and data registers are accessed via OTAD3.
4. Write posting and other performance enhancements may be enabled via the OTAT∗ registers. The OTATX values shown above do not enable any of the available performance enhancements.

PCI Memory Map

Following a reset, the Harrier ASIC disables all PCI slave map decoders. Software must allocate PCI memory and I/O space as needed for the system configuration.

VME Memory Map

The PowerPlus III architecture is fully capable of supporting both the PREP and the CHRP VME Memory Map examples with RAM size limited to 2GB.

ISA Memory Map

The Harrier chip provides many of the I/O peripherals (such as UARTs) typically required in a computer. For that reason, a typical board compatible with the PowerPlus III architecture may not implement an ISA bus. If an ISA bus is required in a PowerPlus III board, it should be implemented consistent with the ISA bus implementation found on Genesis II boards.

SDRAM Interface

I^2C SROM devices are used to provide information to software regarding the size and speed of the SDRAM banks. Refer to Table 1-5 for the I^2C SROM address assignments.

SPD SRAMs are accessible via the I^2C bus interface provided by the Harrier chip.

Refer to the *Harrier ASIC Programmer's Reference Guide* for more information on the SDRAM-related registers.

SPD Format

The SPD format used on boards compatible with the PowerPlus III architecture, such as the PrPMC800/800ET, conforms to the JEDEC industry standard JESD21-C.

Flash Interface

A PowerPlus III board such as the PrPMC800/800ET may have up to two banks of flash memory, designated as flash bank A and flash bank B. Flash bank A is accessed through Xport 0, while flash bank B is accessed through Xport 1. The Xport programmable map decoders can support any flash size from 0 to 4GB with 64KB resolution. Due to memory map limitations, flash bank A can accommodate up to 224MB while flash bank B can accommodate up to 7MB.

The width of the flash data bus is 16 bits and is determined by hardware configuration resistors at power-up. The remainder of Xport configuration is initialized by software. VPD provides a flash information packet that software can use to determine the size, configuration, speed, etc. of flash devices on the board.

PPC System Bus Functions

The following sections describe the PPC system bus functions as implemented on the PrPMC800/800ET.

Processor

The PrPMC800/800ET has the BGA footprint that supports the MPC750-class and MPC7410 processor families. Parity checking is supported for the processor address and data buses.

Processor Type Identification

The type of the processor can be determined by reading the Processor Version register (PVR).

- The PVR value for MPC750-class processors is $08
- The PVR value for the MPC7410 and MPC7410 (N) is $800C

Processor PLL Configuration

The processor internal clock frequency (core frequency) is a multiple of the system bus frequency. The processor has four configuration pins, PLL_CFG[0:3], for hardware strapping of the processor core frequency

between 2x and 8x of the system bus frequency, in 0.5x steps. The processor core frequency is set by installing the appropriate resistors during assembly. The state of these bits may be read through the PC(0-3) bits in the processor HID1 register.

L2 Cache

The PrPMC800/800ET module implements the L2 cache using a two-way, set-associative tag memory located in the processor chip, with external direct-mapped synchronous SRAMs for data storage. The external SRAMs are accessed through a dedicated L2 cache port on the processor.

L2 Cache SRAM Size

The L2 cache port on MPC750-class processors supports SRAM configurations of 256K, 512K or 1M, while the MPC7410 supports up to 2MB. You define the L2 cache size by reading the L2 Cache configuration data in the VPD SROM and programming the L2SIZ bits in the processor L2 Cache Control register. The standard cache size on the PrPMC800/800ET is 1MB for MPC750-class processors, 2MB for the MPC7410, and 1MB for the MPC7410 (N). Refer to the individual processor specifications for details.

Cache Speed

The processor L2 cache port provides the clock for the synchronous SRAMs. This clock is generated by dividing the processor core frequency. Available core-to-cache ratios are 3:1, 5:2, 2:1, 3:2, or 1:1. The core-to-cache ratio is selected by reading the L2 Cache configuration data in the VPD SROM and programming the L2CLK bits of the processor L2 Cache Control register. Refer to the individual processor specification for details.

Flash Memory

The PrPMC800/800ET is configured with one bank of flash memory residing at flash bank A (Xport 0). The bank consists of two Intel StrataFlash devices configured as 8-bit devices making this flash bank 16-bits wide. All writes to this flash bank must be 8-bit or 16-bit writes on an aligned boundary. The Intel StrataFlash devices support page read operations with a page size of eight bytes for each device. The Harrier

Xport 0 may be set for a burst size of 16 bytes in order to take advantage of the page mode feature. Refer to the *Intel 28F128J3A Data Sheet* for page mode timing.

The bank width is automatically determined by the Harrier ASIC during power-up configuration. Note that the flash type, size, configuration and speed information may be determined by analyzing the flash Memory Configuration information in the VPD SROM and by reading the flash device Common Flash Interface (CFI) information. The flash type information is used to determine the correct programming algorithm for the actual flash devices.

An optional bank of flash, bank B, may be located on the host board and accessed through the PMC P14 connector via Xport 1. This flash bank is configured by default to be 16-bits wide using the Hawk 16-bit compatibility mode with Hawk data ordering. This makes the P14 flash interface compatible with the PrPMC750. This Xport may be configured, using on board jumpers, to operate in the normal data ordering mode in which the data alternates every byte instead of every four bytes as in the Hawk data ordering mode.

The reset vector may be sourced by either bank A or bank B depending on the state of the Harrier Xport reset vector control bits (***RVEN0/RVEN1***). When the ***RVEN0*** bit is set, address range $FFF00000-$FFFFFFFF maps to bank A. When ***RVEN0*** bit is cleared and the ***RVEN1*** bit is set, the address range $FFF00000-$FFFFFFFF maps to bank B. The default state uses bank A for the reset vector. Bank B may be selected by connecting the BANKB_SEL pin on P14 to 3.3V. Xport 1 may be configured to operate in the normal data byte ordering mode where the data alternates every byte instead of every forth byte (Hawk data mode). The data ordering mode is controlled by one of the on board jumpers.

System Memory

PrPMC800/800ET system memory consists of one bank of on-board SDRAM (Harrier bank A). The bank consists of 64 data bits and 8 check bits. The size and configuration of the on-board memory bank can be determined by reading the on-board SPD SROM data.

Harrier ASIC

The characteristics of the Harrier ASIC's interface to flash and RAM memory are described in the *Harrier ASIC Programmer's Reference Guide*.

PPC Bus Arbitration

The Harrier PPC arbiter provides the arbitration for the processor 60*x* bus. There are only two PPC bus masters: the PowerPC-compatible processor and the Harrier ASIC. The processor is connected to the Harrier arbiter CPU0_REQ/CPU0_GNT signal pair (XARB3/XARB0). The Harrier PPC arbiter supports both fixed and rotating priority schemes. Refer to the *Harrier ASIC Programmer's Reference Guide* for programming details.

PCI Bus Arbitration

PCI bus arbitration must be provided by the baseboard in the standard PrPMC800/800ET configuration.

PPC-to-PCI Bus Clock Ratio

The Harrier ASIC determines the PPC-to-PCI bus clock ratio by reading the state of the XAD (14:12) pins at power-up. The state of these pins is a function of configuration resistors and the signal on the PMC M66EN pin. Software can find the PPC-to-PCI bus clock ratio by reading the Global Control and Status register at address $FEFF 0010. For details, refer to the *Harrier ASIC Programmer's Reference Guide*.

Harrier I^2C Interface

The Harrier ASIC has two independent I^2C (Inter-Integrated Circuit) two-wire serial interface buses with a serial clock line (SCL) and a serial data line (SDA). Each interface has *master-only* capability. I^2C Channel 0 is used to obtain configuration information from the slave I^2C serial EEPROM devices. Three on-board EEPROM devices maintain the configuration data related to the board's Vital Product Data (VPD), user-specified configuration data (User Product Data, UPD), and the on-board memory subsystem data (Serial Presence Detect, SPD). Additionally, a 256x8 EEPROM may be located on the baseboard. You can use this device to provide information on the configuration of the baseboard when the

PrPMC800/800ET is operating as System Controller (in monarch mode). The I^2C channel 1 bus may be used to host additional EEPROM devices or other I^2C devices, depending on the specific requirements of the board.

Each slave EEPROM device connected to the I^2C bus is software addressable by a unique address. The following table defines the addresses for each of these devices.

Table 1-5. I^2C Device Addressing

Device Function	Size	Device Address (A2A1A0)	Software Address	Note
Onboard Configuration VPD	8Kx8	000b	$A0	1
Onboard User Configuration Data	8Kx8	001b	$A2	1
Optional Baseboard Configuration	256x8	011b	$A6	
Onboard Memory SPD (Bank A)	256x8	100b	$A8	

Note This is a dual-address serial EEPROM device. Refer to the *Atmel AT24C64 Data Sheet* for programming details.

PCI Configuration Space

The Harrier ASIC's PCI Configuration Space registers are normally initialized by the host processor when the PrPMC800/800ET is operating as a slave module. The Harrier IDSEL-to-AD bit mapping is determined by signal routing on the baseboard.

When operating as a monarch (system controller), PCI Configuration Space accesses are accomplished via the Harrier using the CONADD and CONDAT registers. The CONADD register and the CONDAT register are located at offsets CF8h and CFCh, respectively, from the PCI I/O base address. Refer to the PCI specification and/or the Harrier *Programmer's Reference Guide* for more information on the use of these registers. After

a reset, the PCI I/O base address is defaulted to 80000000h. The Harrier IDSEL to AD bit mapping is determined by signal routing on the baseboard.

Operating Mode

The operating mode of the PrPMC800/800ET is determined by the state of the Processor PMC MONARCH# pin. If MONARCH# is high, the PrPMC800/800ET operates as a NON-MONARCH# or slave processor. If MONARCH# is low, the PrPMC800/800ET operates as a system controller module (monarch mode) and provides PCI bus configuration and PCI interrupt handling functions. The PCI interrupt handling feature must be enabled in software by programming the MPIC accordingly. Software can determine the state of the MONARCH# signal by reading the Harrier Miscellaneous Control and Status register.

External Registers

The PrPMC800/800ET module does not implement any external hardware registers. All required control and status functions implemented in the previous processor, the PrPMC750 design, are implemented using the Harrier register set and programming model. These functions include the serial debug port (Harrier, UART0), BAUOUT status, ABORT status, board fail LED control, module reset control, PCI interrupt routing registers, and processor timebase enable. Refer to the *Harrier ASIC Programmer's Reference Guide* for additional information.

Programming Details 2

Introduction

This chapter contains details of several programming functions that are not tied to any specific ASIC chip.

Harrier MPIC

The Harrier ASIC has a built-in interrupt controller that meets the Multi-Processor Interrupt Controller (MPIC) specification. This MPIC supports up to two processors and 16 external interrupt sources. There are also 10 other interrupt sources inside the MPIC; four interprocessor sources, four timer interrupts, an internal functional interrupt, and an error exceptions interrupt. The internal functions interrupt includes the DMA controller, the message unit, the abort switch and the internal UARTs. PowerPlus III designs can combine interrupts or use interrupt expansion devices prior to connection to the Harrier MPIC. For example, if an ISA bus is present on the baseboard, interrupts can be routed to the 8259 pair in the ISA bridge and the output of the ISA bridge then goes through the MPIC in the Harrier. A module using an ISA bridge as an interrupt expansion device shall specify the interrupt assignment within its programming model. Refer to the *Harrier ASIC Programmer's Reference Guide* for details on the Harrier MPIC.

The following table shows the interrupt assignments for the Harrier MPIC on a board using PowerPlus III architecture.

Table 2-1. Harrier Interrupt Assignments

MPIC IRQ	Edge/ Level	Polarity	Interrupt Source	Notes
IRQ0	-	-	HOSTINT0	2
IRQ1	N/A	N/A	Not used	
IRQ2	Level	Low	DEBUGINT_L	4

Table 2-1. Harrier Interrupt Assignments (Continued)

MPIC IRQ	Edge/ Level	Polarity	Interrupt Source	Notes
IRQ3	Level	Low	Harrier WDT0O_L	
IRQ4	N/A	N/A	Not used	
IRQ5	N/A	N/A	Not used	
IRQ6	-	-	HOSTINT1	3
IRQ7	-	-	HOSTINT2	3
IRQ8	-	-	HOSTINT3	3
IRQ9	Level	Low	PMC INTA#	1
IRQ10	Level	Low	PMC INTB# || GD82559ER/82551IT INTA#	1
IRQ11	Level	Low	PMC INTC#	1
IRQ12	Level	Low	PMC INTD#	1
IRQ13	N/A	N/A	Not used	
IRQ14	N/A	N/A	Not used	
IRQ15	N/A	N/A	Not used	

Notes

1. Unmask these interrupt modes in monarch mode only.
2. This is a general-purpose interrupt from the host board routed through the P14 connector. Edge/level and polarity settings are programmable, depending on the requirements of the host board. This interrupt should be used for 8259-type interrupt controllers if implemented on the baseboard.
3. These are general-purpose interrupts from the host board routed through the P14 connector. These interrupts are active low; edge/level settings are programmable depending on the requirements of the host board.
4. Interrupt routed from debugger header.

Sources of Reset

There are five potential sources of reset on PrPMC800/800ET series boards. They are:

1. Power-on reset
2. PMC PCI RST# signal
3. Watchdog timer reset via the Harrier Watchdog 1 Timer output
4. Software-generated reset from the Harrier RSTOUT bit
5. RESET_L signal from the debug header

Only the Power-On and PCI reset sources reset the processor, the Harrier ASIC and all other onboard logic. The PMC RESETOUT_L pin is also activated for each reset source, except the PMC PCI RST# input.

Soft Reset

Software can assert the SRESET# pin of the processor by appropriately programming the P0 bit in the Processor Init register in the Harrier MPIC.

CPU Reset

The Harrier HRST0_L output is connected to the CPU reset logic. Setting the Processor 0 Holdoff bit in the Harrier Bridge PowerPC Control and Status register will result in the local processor being held in reset. Clearing the bit will release the reset. This feature can be used by a processor on the baseboard to disable the local processor while the host processor programs the onboard bank A flash.

2

Endian Issues

The PrPMC800 endian issues are fully described within the *Harrier ASIC Programmer's Reference Guide*.

Error Notification and Handling

The Harrier ASIC can detect certain hardware errors and can be programmed to report these errors via the MPIC interrupts or the Machine Check interrupt. The following table summarizes how hardware errors are handled by PrPMC800 series boards.

Table 2-2. Exception Summary - Error Category

Exception	Description	Primary Status	Additional Status	Clear	Edge/ Level
Processor Address Bus Time-out	Any unclaimed processor address tenure originating from any processor bus master.	EEST.XBT	EXAD/ EXAT	**EECL**.XBT (*XCSR*)	Edge
Processor Address Parity Error	Detection of an address parity error during any address tenure involving any processor bus master.	EEST.XAP	EXAD/ EXAT	**EECL**.XAP (*XCSR*)	Edge
Processor Data Parity Error	Detection of a data parity error during any data tenure involving any processor bus master and any processor bus slave.	EEST.XDP	EXAD/ EXAT	**EECL**.XDP (*XCSR*)	Edge
Processor Delayed Transaction Time-out	Any unclaimed processor delayed transaction originating from any processor bus master.	**EEST.**XDT	EXAD/ EXAT	**EECL**.XDT (*XCSR*)	Edge
SDRAM Memory Interface Single BIt Error	Detection and correction of a single bit error.	**EEST**.SSE	SDSES/ SDSEA	**EECL**.SSE (*XCSR*)	Edge

Table 2-2. Exception Summary - Error Category (Continued)

Exception	Description	Primary Status	Additional Status	Clear	Edge/ Level
SDRAM Memory Interface Single Bit Error Overflow	Detection of a single bit error count overflow	**EEST**.SSC	SDSES	**EECL**.SSC (*XCSR*)	Edge
SDRAM Memory Interface Multi Bit Error on Processor Access	Detection of a multi bit error during any processor access.	**EEST**.SMX	SDMES/ SDMEA	**EECL**.SMX (*XCSR*)	Edge
SDRAM Memory Interface Multi Bit Error on Scrub	Detection of a multi bit error on a scrub.	**EEST**.SMS	SDMES/ SDMEA	**EECL**.SMS (*XCSR*)	Edge
PCI Master Abort	Detection of a Master Abort with the Harrier as a PCI Bus Master. Can be either a bridge or a DMA transaction.	EEST.PMA	EPAD/ EPAT	EECL.PMA (*XCSR*)	Edge
PCI Target Abort	Detection of a Target Abort with the Harrier as a PCI Bus Master. Can be either a bridge or a DMA transaction.	EEST.PTA	EPAD/ EPAT	EECL.PTA (*XCSR*)	Edge
PCI Address Parity Error	Detection of a parity error during the address phase of any PCI transfer involving any PCI bus master and target.	EEST.PAP	EPAD/ EPAT	EECL.PAP (*XCSR*)	Edge

Table 2-2. Exception Summary - Error Category (Continued)

Exception	Description	Primary Status	Additional Status	Clear	Edge/ Level
PCI Data Parity Error	Detection of a parity error during the data phase of any PCI transfer involving any PCI bus master and target.	EEST.PDP	EPAD/ EPAT	EECL.PDP (*XCSR*)	Edge
PCI SERR	Assertion of SERR. Note that this may or may not be as a result of the Harrier detecting an address parity error.	EEST.PSE	None	**EECL**.PSE (*XCSR*)	Edge
PCI PERR	Assertion of PERR. Note that this may or may not be as a result of the Harrier detecting a data parity error.	EEST.PPE	None	**EECL**.PPE (*XCSR*)	Edge
PCI Delayed Transaction Time-out	Any unclaimed PCI delayed transaction originating from any PCI bus master.	**EEST.**PDT	EXAD/ EXAT	**EECL**.PDT (*XCSR*)	Edge
PCI Master Retry Error	Bridge or DMA as a PCI master has exceeded the maximum number of sequential retries.	EEST.PMR	EPAD/ EPAT	EECL.PMR (*XCSR*)	Edge

Table 2-3. Exception Summary - Functional Category

Exception	Description	Primary Status	Additional Status	Clear	Edge/ Level
DMA Controller	Completion of a Direct Mode transfer or a Linked-List Mode transaction. May be accompanied by an error condition.	**FEST**.DMA	DSTA	**FECL**.DMA (*XCSR*)	Edge
MP Generic Doorbell	Assertion of any Inbound Doorbell bit.	**FEST**.MDB	MGID	MGID.DBIx (*XCSR*)	Edge

Table 2-3. Exception Summary - Functional Category (Continued)

Exception	Description	Primary Status	Additional Status	Clear	Edge/ Level
MP Generic Message #0	New message written to Message Passing Register 0.	**FEST**.MM0	MGIM0	**FECL**.MM0 (*XCSR*)	Edge
MP Generic Message #1	New message written to Message Passing Register 1.	**FEST**.MM1	MGIM1	**FECL**.MM1 (*XCSR*)	Edge
MP I2O Inbound post_list	New entry written into Inbound Post_List queue. (**MIIPH** != **MIIPT**)	**FEST**.MIP	MIIPH/ MIIPT	MIIPH = MIIPT	Level
UART #0	UART0 Received data available interrupt, time-out interrupt in the FIFO mode, Transmitter holding register empty interrupt, Receiver line status interrupt or MODEM status interrupt.	**FEST**.UA0	IDFC0	UART0 service routine	Level
UART #1	UART1 Received data available interrupt, time-out interrupt in the FIFO mode, Transmitter holding register empty interrupt, Receiver line status interrupt or MODEM status interrupt.	**FEST**.UA1	IDFC1	UART1 service routine	Level
Abort	Assertion of ABTSW_ pin for a short period.	**FEST**.ABT	None	**FECL**.ABT (*XCSR*)	Edge

PrPMC800/800ET VPD Reference Information

A

The data listed in the following tables are for general reference information. The VPD identifies board information that may be useful during board initialization, configuration, and verification.

Information that is contained in the VPD includes:

- Marketing Product Number (for example, PrPMC815-1251)
- Factory Assembly Number (for example, 01-W3506F01)
- Serial number of the specific PrPMC815
- Processor family number (for example, 8245, etc.)
- Hardware clock frequencies (internal, external, fixed, PCI bus)
- Component configuration information (connectors, Ethernet addresses, Flash Bank ID)
- Security information (VPD type, version and revision data, 32-bit CRC protection)
- Base address information for various components
- Direct Memory Addresses
- Interrupt resources

How to Read the VPD Information

There are several ways to read VPD information:

- Version command - **ver**
- Displays most of the identification strings and hardware clock frequencies
- Serial EEPROM command - **srom;i**

- Can be used as a byte viewer
- Indirect block move command - **ibm<addr>;i**
- Reads the entire SROM block to memory
- Memory display command - **md<addr>**
- Can be used to display a VPD block which has been copied to memory
- Network I/O physical command - **niop**
- Can be used to upload a VPD block from memory to a network file

How to Modify the VPD Information

The following commands can be used to modify the VPD information in various ways:

- Serial EEPROM command - **srom;i**

Can be used as a byte editor

- Network I/O physical command - **niop**
- Can be used to download a VPD block from a network file to memory
- Indirect block move command - **ibm<addr>;iw**
- Writes a block of memory into the SROM
- SROM update command - **update**
- Updates each SROM on the board to the current revision using network files

What Happens if the VPD Information is Corrupted?

If for some reason the VPD information becomes corrupted, the following occurs:

- A warning is displayed in the startup banner
- The firmware ignores the VPD contents and attempts to acquire information from other sources
- Some device drivers will not work
- Some diagnostic tests fail
- The board runs much slower than usual

How to Fix Corrupted VPD Information

- The firmware is designed to reach the prompt with bad VPD
- Use the **srom**, **ibm**, or **update** command to fix the VPD

How to Fix Wrong VPD Problems

If you suspect that your board has problems as a result of wrong VPD information, perform the following:

- Press the abort switch during startup (double-button reset - reset/abort) to enter the safe mode (at this point, the firmware will ignore all SROM contents and reset)
- Use the **srom**, **ibm**, or **update** command to change the VPD to the correct parameters

The data listed in the following tables are for general reference information. It is divided into two major sections: *VPD Packet Types* which define VPD packet formats, and *VPD Data Definitions* which includes information on what is actually contained in the VPD.

What if Your Board Has the Wrong VPD?

If for some reason your board has the wrong VPD information, the following occurs:

- No warning is displayed
- The firmware believes the incorrect VPD information
- The board may hang during startup (no-start condition)
- The board may be very unstable if it reaches the prompt
- Device drivers, diagnostic tests, and firmware commands may hang or fail in unexpected ways

VPD Data Definitions

The following table describes and lists the currently assigned packet identifiers. **Note: Additional packet identifiers may be added to this list as future versions of the VPD are released.**

Table A-1. VPD Packet Types

ID#	Size	Description	Data Type	Notes
00	N/A	Guaranteed Illegal	N/A	
01	Variable	Product Identifier (e.g., “MBX”, “MTX”, “PrPMC800”, “MCP750”, “MVME2400”, etc.)	ASCII	1
02	Variable	Factory Assembly Number (e.g., “01-W3649F04C”, etc.)	ASCII	1
03	Variable	Serial Number (e.g., “3383185”, etc.)	ASCII	1
04	10	Product Configuration Options Data The data in this packet further describes the board configuration (e.g., header population, I/O routing, etc.). Its exact contents is dependent upon the product configuration/type. A following table describes this packet.	Binary	
05	04	MPU Internal Clock Frequency in Hertz (e.g., 350,000,000 decimal, etc.)	Integer (4-byte)	2

Table A-1. VPD Packet Types (Continued)

ID#	Size	Description	Data Type	Notes
06	04	MPU External Clock Frequency in Hertz (e.g., 100,000,000 decimal, etc.). This is also called the local processor bus frequency.	Integer (4-byte)	2
07	04	Reference Clock Frequency in Hertz (e.g., 32,768 decimal, etc.). This value is the frequency of the crystal driving the OSCM.	Integer (4-byte)	2
08	06	Ethernet Address (e.g., 08003E26A475, etc.)	Binary	3, 4
09	Variable	MPU Type (e.g., 601, 602, 603, 604, 750, 801, 821, 823, 860, 860DC, 860DE, 860DH, 860EN, 860MH, etc.)	ASCII	1
0A	04	EEPROM CRC This packet is optional. This packet would be utilized in environments where CRC protection is required. When computing the CRC this field (i.e., 4 bytes) is set to zero. This CRC only covers the range as specified the size field.	Integer (4-byte)	2
0B	0C	Flash Memory Configuration A table found later in this document further describes this packet.	Binary	
0C	TBD	VLSI Device Revisions/Versions	Binary	
0D	04	Host PCI-Bus Clock Frequency in Hertz (e.g., 33,333,333 decimal, etc.)	Integer (4-byte)	2
0E	0F	L2 Cache Configuration A table found later in this document further describes this packet.	Binary	
0F	04	VPD Revision. A table found later in this section further describes this packet.	Binary	
10-BF		Reserved		

Table A-1. VPD Packet Types (Continued)

ID#	Size	Description	Data Type	Notes
C0-FE		User Defined An example of a user defined packet could be the type of LCD panel connected in an MPC821 based application.		
FF	N/A	Termination Packet (follows the last initialized data packet)	N/A	

Notes

1. The data size is variable. Its actual size is dependent upon the product configuration/type.
2. Integer values are formatted/stored in big-endian byte ordering.
3. This packet may be omitted if the Ethernet interface is nonexistent, or the Ethernet interface has an associative SROM (e.g., DEC21x4x).
4. This packet may contain an additional byte following the address data. This additional byte indicates the Ethernet interface number. This additional byte would be specified in applications where the host product supports multiple Ethernet interfaces. For each Ethernet interface present, the instance number would be incremented by one starting with zero.

Product Configuration Options Data

The product configuration options data packet consists of a binary bit field. The first bit of the first byte is bit 0 (for example, bit numbering is compatible with PowerPC architecture). An option is present when the assigned bit is a 1. The following table describes the VPD product configuration options that are present in the PrPMC800:

Table A-2. MCG Product Configuration Options Data

Bit Number	Bit Mnemonic	Bit Description
0	PCO_PCI0_CONN1	PCI/PMC bus 0 connector 1 present
16	PCO_ENET1_CONN	Ethernet device 1 connector present
24	PCO_SERIAL1_CONN	Serial device 1 connector present
32	PCO_PMC1_IO_CONN	PMC slot 1 I/O connector present
42	PCO_ABORT_SWITCH	Abort switch present
43	PCO_BDFAIL_LIGHT	Board Fail light present

Flash Memory Configuration Data

The Flash memory configuration data packet consists of byte fields which indicate the size/organization/type of the Flash memory array. The following table(s) further describe the Bank A Flash memory configuration VPD data packet.

Table A-3. Bank A Flash Memory Configuration Data

Field Mnemonic	Field Description	Field Values	Value Description
FMC_MID	Manufacturer's Identifier (FFFF = Undefined/Not applicable)	$0089	Intel
FMC_DID	Manufacturer's Device Identifier (FFFF = Undefined/Not applicable)	$0018	28F128J3A (128 Mbit)
FMC_DDW	Device Data Width (e.g., 8-bits, 16-bits)	$08	8-bits

Table A-3. Bank A Flash Memory Configuration Data

Field Mnemonic	Field Description	Field Values	Value Description
FMC_NOD	Number of Devices/Sockets Present	$02	Two devices
FMC_NOC	Number of Columns (Interleaves)	$01	One device
FMC_CW	Column Width in Bits This will always be a multiple of the device's data width.	$10	16-bits
FMC_WEDW	Write/Erase Data Width The Flash memory devices must be programmed in parallel when the write/erase data width exceeds the device's data width.	$10	16-bits
FMC_BANK	Bank Number of Flash Memory Array: 0 = A, 1 = B	$00	Bank A
FMC_SPEED	Flash Access Speed in Nanoseconds	$96	150nS (28F128J3A)
FMC_SIZE	Total Bank Size (Should agree with the physical organization above): 00=256K, 01=512K, 02=1M, 03=2M, 04=4M, 05=8M	$07	32 Mbytes (28F128J3A)

A product may contain multiple flash memory configuration packets.

L2 Cache Configuration Data

The L2 cache configuration data packet consists of byte fields that show the size, organization, and type of the L2 cache memory array. The following table(s) further describe the L2 cache memory configuration VPD data packet.

Table A-4. L2 Cache Configuration Data

Field Mnemonic	Field Description	Field Values	Value Description
L2C_MID	Manufacturer's Identifier (FFFF = Undefined/Not applicable)	$FFFF	Undefined/Not applicable
L2C_DID	Manufacturer's Device Identifier (FFFF = Undefined/Not applicable)	$FFFF	Undefined/Not applicable
L2C_DDW	Device Data Width (e.g., 8-bits, 16-bits, 32-bits, 64-bits, 128-bits)	$20	32-bits
L2C_NOD	Number of Devices Present	$02	2 devices
L2C_NOC	Number of Columns (Interleaves)	$02	2 columns
L2C_CW	Column Width in Bits This will always be a multiple of the device's data width.	$20	32-bits
L2C_TYPE	L2 Cache Type: 00 - Arthur Backside 01 - External 02 - In-Line	$00	Either write-through or write-back (software configurable)
L2C_ASSOCIATE	Associative Microprocessor Number (If Applicable)	$00	Not applicable

Table A-4. L2 Cache Configuration Data (Continued)

Field Mnemonic	Field Description	Field Values	Value Description
L2C_OPERATION MODE	Operation Mode: 00 - Either Write-Through or Write-Back (S/W Configurable) 01 - Either Write-Through or Write-Back (H/W Configurable) 02 - Write-Through Only 03 - Write-Back Only	$00	Either write-through or write-back (software configurable)
L2C_ERROR_DETECT	Error Detection Type: 00 - None 01 - Parity 02 - ECC	$01	Parity
L2C_SIZE	L2 Cache Size (Should agree with the physical organization above): 00 - 256K 01 - 512K 02 - 1M 03 - 2M 04 - 4M	$02 $03	1MB (4Mbit cache SRAM) 2MB (8Mbit cache SRAM)

Table A-4. L2 Cache Configuration Data (Continued)

Field Mnemonic	Field Description	Field Values	Value Description
L2C_TYPE_BACK SIDE	L2 Cache Type (Backside Configurations): 00 - Late Write Sync, 1nS Hold, Differential Clock, Parity 01 - Pipelined Sync Burst, 0.5nS Hold, No Differential Clock, Parity 02 - Late Write Sync, 1nS Hold, Differential Clock, No Parity 03 - Pipelined Sync Burst, 0.5nS Hold, No Differential Clock, No Parity	$01	Piplines sync burst, 0.5ns hold, no differential clock, parity.
L2C_RATIO_BACK SIDE	Processor Core to L2 Cache Ratio (Backside Configurations): 00 - Disabled 01 - 1:1 (1) 02 - 3:2 (1.5) 03 - 2:1 (2) 04 - 5:2 (2.5) 05 - 3:1 (3)	$03 $04	2:1 (for MPC750-class or MPC7410 (N) processor) 5:2 (for MPC7410 processor)

A product may contain multiple L2 cache configuration packets.

VPD Revision Data

The VPD revision data packet consists of byte fields that indicate the type, version, and revision of the vital product data. The following table(s) further describe the VPD revision data packet.

Table A-5. VPD Revision Data

Byte Offset	Field Size (Bytes)	Field Mnemonic	Field Description
00	1	VR_TYPE	Vital Product Data Type: 00 - Processor board VPD 01 - Baseboard (non-processor) VPD 02 - Transition module VPD
01	1	VR_ARCH	Vital Product Data Architecture Revision (currently at 2)
02	1	VR_BUILD	Vital Product Data Board Build Revision (starts at 0)
03	1	VR_REASON	Vital Product Data Revision Flags: 00 - Initial release

A product must have exactly one VPD revision packet.

Local Memory Configuration

The format for the local memory configuration data follows the industry standard format for the SDRAM module Serial Presence Detect (SPD) definitions. The following tables list the variable and static contents of the SPD serial EEPROM for the various memory configuration options.

Table A-6. Variable SPD SROM Configuration Data

SPD Offset	SDRAM Configuration		
	64Mbytes Nine 8Mx8 devices	128Mbytes Nine 16Mx8 devices	256Mbytes Nine 32Mx8 devices
03 (0x03)	0C	0C	0D
04 (0x04)	09	0A	0A
09 (0x09)	80	A0	A0
13 (0x0D)	08	08	08
14 (0x0E)	08	08	08
23 (0x17)	A0	C0	C0
24 (0x18)	60	70	70
28 (0x1C)	10	14	14
30 (0x1E)	30	32	32
31 (0x1F)	10	20	40
63 (0x3F)	57	BE	DF

Table A-7. Static SPD SROM Configuration Data

Offset	Value	Description
00 (0x00)	80	Number of Serial PD Bytes written during module production. Refer to Note 1.
01 (0x01)	08	Total Number of Bytes in Serial PD Device. Refer to Note 2.
02 (0x02)	04	Fundamental Memory Type (FPM, EDO, SDRAM)
03 (0x03)	xx	Number of Row Addresses on this assembly Refer to Note 3. Refer to Table A-6 for “xx” values.
04 (0x04)	xx	Number of Column Addresses on this assembly. Refer to Table A-6 for “xx” values.
05 (0x05)	01	Number of DIMM Banks.
06 (0x06)	48	Data Width of this assembly
07 (0x07)	00	---as above---
08 (0x08)	01	Voltage Interface Level of this assembly
09 (0x09)	xx	SDRAM Cycle time at Maximum Supported CAS Latency (CL), CL=X. Refer to Note 4. Refer to Table A-6 for “xx” values.
10 (0x0a)	60	SDRAM Access from Clock.
11 (0x0b)	02	DIMM configuration type (Non-parity, Parity or ECC)
12 (0x0c)	00	Refresh Rate/Type Refer to Notes 4, 5
13 (0x0d)	xx	Primary SDRAM Width. Refer to Table A-6 for “xx” values.
14 (0x0e)	xx	Error Checking SDRAM Width. Refer to Table A-6 for “xx” values.
15 (0x0f)	01	SDRAM Device Attributes: Minimum Clock Delay, Back-to-Back Random Column Access
16 (0x10)	8F	SDRAM Device Attributes: Burst Lengths Supported
17 (0x11)	04	SDRAM Device Attributes: Number of Banks on SDRAM Device. Refer to Note: 4
18 (0x12)	06	SDRAM Device Attributes: CAS Latency. Refer to Note 4.
19 (0x13)	01	SDRAM Device Attributes: CS Latency. Refer to Note 4.

Table A-7. Static SPD SROM Configuration Data (Continued)

Offset	Value	Description
20 (0x14)	01	SDRAM Device Attributes: Write Latency. Refer to Note 4.
21 (0x15)	00	SDRAM Module Attributes
22 (0x16)	0E	SDRAM Device Attributes: General. Refer to Note: 4.
23 (0x17)	xx	Minimum Clock Cycle at CLX-1. Refer to Note 4. Refer to Table A-6 for “xx” values.
24 (0x18)	xx	Maximum Data Access Time (t AC) from Clock at CLX-1. Refer to Note 4. Refer to Table A-6 for “xx” values.
25 (0x19)	00	Minimum Clock Cycle at CLX-2. Refer to Note 4.
26 (0x1a)	00	Maximum Data Access Time (t AC) from Clock at CLX-2. Refer to Note 4.
27 (0x1b)	14	Minimum Row Precharge Time (t RP). Refer to Note 4.
28 (0x1c)	xx	Minimum Row Active to Row Active delay (t RRD). Refer to Note 4. Refer to Table A-6 for “xx” values.
29 (0x1d)	14	Minimum RAS to CAS delay (t RCD). Refer to Note 4.
30 (0x1e)	xx	Minimum RAS Pulse width (t RAS). Refer to Note 4. Refer to Table A-6 for “xx” values.
31 (0x1f)	xx	Module Bank Density. Refer to Table A-6 for “xx” values.
32 (0x20)	20	Address and Command Setup Time Before Clock. Refer to Note: 6.
33 (0x21)	10	Address and Command Hold Time After Clock. Refer to Note: 6.
34 (0x22)	20	Data Input Setup Time Before Clock. Refer to Note: 6.
35 (0x23)	10	Data Input Hold Time After Clock. Refer to Note: 6.
36 (0x24)	FF	Reserved for future expansion
:	:	:
61 (0x3D)	FF	
62 (0x3E)	12	SPD Revision
63 (0x3F)	xx	Checksum for bytes 0-62. Refer to Table A-6 for “xx” values.
64 (0x40)	FF	Reserved for future expansion

Table A-7. Static SPD SROM Configuration Data (Continued)

Offset	Value	Description
:	:	
255 (0xFF)	FF	

Notes

1. This is normally programmed as 128 Bytes.
2. This is normally programmed as 256 Bytes.
3. The high order bit defines this value if the assembly requires “redundant” addressing (if it is set to “1”, redundant addressing is required).
4. From SDRAM datasheet.
5. The high order bit is the Self Refresh “flag”. If it is set to “1”, the assembly supports self refresh.
6. The JEDEC spec specifies that these bytes are optional for 66 MHz applications. If they are not included, then the SPD revision level (byte 62) is set at revision 1 (01h).

SROM Data Definitions

The following table defines the contents of the AT93C46 serial EEPROM device used to store configuration data for the 82559ER/82551IT device.

Table A-8. 82559ER/82551IT SROM Contents

Word Address	Fixed/ Variable	High Byte	Low Byte	Default Value (Hex)
0	Variable	IA Byte 2	IA Byte 1	Ethernet Adr, Word 1 **[xxxx]**
1	Variable	IA Byte 4	IA Byte 3	Ethernet Adr, Word 2 **[xxxx]**
2	Variable	IA Byte 6	IA Byte 5	Ethernet Adr, Word 3 **[xxxx]**
3	Fixed	Compatibility Byte 1	Compatibility Byte 0	0000
4	Fixed	Reserved	Reserved	0000
5	Fixed	Controller Type	Connectors	0000
6	Fixed	PHY Device Record	PHY Device Record	0000
7	Fixed	Reserved	Reserved	0000
8	Fixed	PWB Byte 1	PWB Byte 2	0000
9	Fixed	PWB Byte 3 (Revision Byte 2)	PWB Byte 4 (Revision Byte 1)	0000
A	Fixed	EEPROM ID	EEPROM ID	4980
EEPROM ID Upper Byte Bit Definitions		Bits [7:6]		01 = EEPROM present
		Bit [5]		0 = Rev ID bits controlled by silicon stepping
		Bit [4]		Reserved
		Bit [3]		1 = Boot ROM Base Address register disabled
		Bits [2:0]		Rev ID bits

Table A-8. 82559ER/82551IT SROM Contents (Continued)

Word Address	Fixed/ Variable	High Byte	Low Byte	Default Value (Hex)
EEPROM ID Lower Byte Bit Definitions			Bit [7]	Power Management enabled (Always set)
			Bit [6]	0 = Deep power down enabled
			Bit [5]	Reserved
			Bit [4]	0 = During WOL mode, the ACT LED is activated by a transmission and reception of broadcast and Individual Address match packets only
			Bits [3:2]	Reserved
			Bit [1]	0 = Standby Mode disabled
			Bit [0]	Reserved
B	Fixed	Subsystem ID	Subsystem ID	0000
C	Fixed	Subsystem Vendor ID	Subsystem Vendor ID	0000
D	Fixed	HB Packet Pointer	SMB Address / EEPROM CIS Pointer	0000
E-2F	Fixed	Reserved	Reserved	0000
30	Fixed	RPL Configuration	RPL Configuration	0000
32-3E	Fixed	Reserved	Reserved	0000
3F	Variable	Checksum High Byte	Checksum Low Byte	Checksum of words 0-3E (16-bit sum of 0-3F = BABAh) **[cccc]**

SROM_CRC.C Routine

```
/*
 * srom_crc - generate CRC data for the passed buffer
 * description:
 * This function's purpose is to generate the CRC for the
 * passed buffer.
 * call:
 *    argument #1 = buffer pointer
 *    argument #2 = number of elements
 * return:
 *    CRC data
 */
unsigned int
srom_crc(elements_p, elements_n)
register unsigned char *elements_p; /* buffer pointer */
register unsigned int elements_n;   /* number of elements */
{
   register unsigned int crc;
   register unsigned int crc_flipped;
   register unsigned char cbyte;
   register unsigned int index, dbit, msb;

   crc = 0xffffffff;
   for (index = 0; index < elements_n; index++) {
      cbyte = *elements_p++;
      for (dbit = 0; dbit < 8; dbit++) {
         msb = (crc >> 31) & 1;
         crc <<= 1;
         if (msb ^ (cbyte & 1)) {
            crc ^= 0x04c11db6;
            crc |= 1;
         }
         cbyte >>= 1;
      }
   }

   crc_flipped = 0;
   for (index = 0; index < 32; index++) {
      crc_flipped <<= 1;
      dbit = crc & 1;
      crc >>= 1;
      crc_flipped += dbit;
   }
   crc = crc_flipped ^ 0xffffffff;
   return (crc);
```

Example VPD SROM

An example of a PrPMC800/800ET board build configuration is provided below.

Table A-9. VPD SROM Configuration Specification for 01-W3649F15*

Offset	Value	Field Type	Description
00 (0x00)	4D	ASCII	Eye-Catcher (“MOTOROLA”) **Note: Starting byte for the calculation of CRC**
01 (0x01)	4F		
02 (0x02)	54		
03 (0x03)	4F		
04 (0x04)	52		
05 (0x05)	4F		
06 (0x06)	4C		
07 (0x07)	41		
08 (0x08)	01	Binary	Size of VPD in area in bytes. The size is viewed as logical, it is not the size of the EEPROM.
09 (0x09)	00		
10 (0x0a)	0F	Packet Binary	VPD Revision
11 (0x0b)	04		
12 (0x0c)	00		
13 (0x0d)	02		
14 (0x0e)	00		
15 (0x0f)	00		
16 (0x10)	01	Packet ASCII	Product Identifier [PrPMC800-xxxx].
17 (0x11)	0D		
18 (0x12)	50		
19 (0x13)	72		
20 (0x14)	50		
21 (0x15)	4D		
22 (0x16)	43		

Table A-9. VPD SROM Configuration Specification for 01-W3649F15*

Offset	Value	Field Type	Description
23 (0x17)	38		
24 (0x18)	30		
25 (0x19)	30		
26 (0x1a)	2D		
27 (0x1b)	31		
28 (0x1c)	32		
29 (0x1d)	35		
30 (0x1e)	31	Packet ASCII	Factory Assembly number [01-W3649Fxx*]
31 (0x1f)	02		
32 (0x20)	0C		
33 (0x21)	30		
34 (0x22)	31		
35 (0x23)	2D		
36 (0x24)	57		
37 (0x25)	33		
38 (0x26)	36		
39 (0x27)	34		
40 (0x28)	39		
41 (0x29)	46		
42 (0x2a)	31		
43 (0x2b)	35		
44 (0x2c)	xx		Serial number
45 (0x2d)	03		
46 (0x2e)	07		
47 (0x2f)	xx		
48 (0x30)	xx		
49 (0x31)	xx		
50 (0x32)	xx		
51 (0x33)	xx		

Table A-9. VPD SROM Configuration Specification for 01-W3649F15*

Offset	Value	Field Type	Description
52 (0x34)	xx		
53 (0x35)	xx		
54 (0x36)	10	Packet Binary	Product Configuration Options data
55 (0x37)	10		
56 (0x38)	80		
57 (0x39)	00		
58 (0x3A)	80		
59 (0x3B)	80		
60 (0x3C)	80		
61 (0x3D)	30		
62 (0x3E)	00		
63 (0x3F)	00		
64 (0x40)	00		
65 (0x41)	00		
66 (0x42)	00		
67 (0x43)	00		
68 (0x44)	00		
69 (0x45)	00		
70 (0x46)	00		
71 (0x47)	00		
72 (0x48)	0B	Packet Binary	Flash Memory configuration (Bank A)
73 (0x49)	0C		
74 (0x4A)	00		
75 (0x4B)	89		
76 (0x4C)	00		
77 (0x4D)	18		
78 (0x4E)	08		
79 (0x4F)	02		
80 (0x50)	01		

Table A-9. VPD SROM Configuration Specification for 01-W3649F15*

Offset	Value	Field Type	Description
81 (0x51)	10		
82 (0x52)	08		
83 (0x53)	00		
84 (0x54)	96		
85 (0x55)	07		
86 (0x56)	OE	Packet Binary	L2 Cache configuration [for 01-3649F15∗ and 02∗ pipeline w/parity, 2M, 5:2]
87 (0x57)	OF		
88 (0x58)	FF		
89 (0x59)	FF		
90 (0x5A)	FF		
91 (0x5B)	FF		
92 (0x5C)	20		
93 (0x5D)	02		
94 (0x5E)	02		
95 (0x5F)	20		
96 (0x60)	00		
97 (0x61)	00		
98 (0x62)	00		
99 (0x63)	01		
100 (0x64)	03		
101 (0x65)	01		
102 (0x66)	04		
103 (0x67)	0A	Packet Integer	EPROM CRC When computing the CRC, this field (four bytes) is set to zero. This CRC only covers the range as Integer (four bytes). Note: Starting byte for the calculation of CRC = 00. End byte for the calculation of CRC = 255.
104 (0x68)	04		

Table A-9. VPD SROM Configuration Specification for 01-W3649F15*

Offset	Value	Field Type	Description
105 (0x69)	xx		**CRC to be filled in at ATE
106 (0x6A)	xx		
107 (0x6B)	xx		
108 (0x6C)	xx		
109 (0x6D)	09	Packet ASCII	MPU Type
110 (0x6E)	04		
111 (0x6F)	37		
112 (0x70)	34		
113 (0x71)	31	Binary	Reserved for future expansion
114 (0x72)	30		
115 (0x73)	FF	Binary	Reserved for future expansion.
:	:		
255 (0xFF)	FF		Reserved for future expansion **Note:** End byte for the calculation of CRC

Note *This data will change to reflect the specific configuration of the corresponding board assembly number to which it applies.

Related Documentation B

Motorola Computer Group Documents

The Motorola publications listed below are referenced in this manual. You can obtain paper or electronic copies of Motorola Computer Group publications by:

- Contacting your local Motorola sales office
- Visiting Motorola Computer Group's World Wide Web literature site, http://www.motorola.com/computer/literature

Table B-1. Motorola Computer Group Documents

Document Title	Publication Number
PrPMC800/800ET Processor PMC Module Installation and Use	PRPMC800A/IH
Harrier ASIC Programmer's Reference Guide	ASICHRA/PG
PPCBug Firmware Package User's Manual (Parts 1 and 2)	PPCBUGA1/UM
	PPCBUGA2/UM
PPCBug Diagnostics Manual	PPCDIAA/UM

To locate and view the most up-to-date product information in PDF or HTML format, visit http://www.motorola.com/computer/literature.

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Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As a further help, sources for the listed documents are also provided. Please note that while these sources have been verified, the information is subject to change without notice.

Table B-2. Manufacturers' Documents

Document Title and Source	Publication Number or Search Term
MPC750 RISC Microprocessor Technical Summary Literature Distribution Center for Motorola Telephone: 1-800- 441-2447 FAX: (602) 994-6430 or (303) 675-2150 WebSite: http://e-www.motorola.com/webapp/DocLibServlet E-mail: ldcformotorola@hibbertco.com	MPC750/D
MPC750 RISC Microprocessor User's Manual *MPC7410 RISC Microprocessor User's Manual* Literature Distribution Center for Motorola Telephone: 1-800- 441-2447 FAX: (602) 994-6430 or (303) 675-2150 WebSite: http://e-www.motorola.com/webapp/DocLibServlet E-mail: ldcformotorola@hibbertco.com OR IBM Microelectronics http://www-3.ibm.com/chips/techlib/	MPC750UMAD/D MPC7410UM/AD MPR750UMU-01
Programming Environments Manual for the Family of 64-Bit Microprocessors that Implement the PowerPC Architecture Literature Distribution Center for Motorola Telephone: 1-800- 441-2447 FAX: (602) 994-6430 or (303) 675-2150 WebSite: http://e-www.motorola.com/webapp/DocLibServlet E-mail: ldcformotorola@hibbertco.com OR	MPCFPE/AD

Table B-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number or Search Term
PowerPC Microprocessor Family: The Programming Environments for 32-Bit Microprocessors IBM Microelectronics Web Site: http://www-3.ibm.com/chips/techlib/	G522-0290-01
Intel 82559ER/82551IT Fast Ethernet PCI Bus Controller with Integrated PHY — External Design Specification; Intel Corporation; http://developer.intel.com/design/network/	
3 Volt Intel StrataFlash® Memory, 28F128J3A Intel Corporation Web: http://developer.intel.com/design/flash/	29066709.pdf
ATMEL 2-Wire Serial EEPROM Data Sheet, AT24C02 *ATMEL 2-Wire Serial EEPROM Data Sheet, AT24C64* ATMEL Nonvolatile Memory Data Book Must request documentation at: http://www.atmel.com/atmel/support/	doc0180.pdf doc0336.pdf
TL16C550C Single UART with 16-Byte FIFO and Auto Flow Control Texas Instruments Web: http://www.ti.com/	TL16C550C

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Related Specifications

The following table lists the product's related specifications. The appropriate source for the listed document is also provided. Please note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Table B-3. Related Specifications

Document Title and Source	Publication Number
VITA http://www.vita.com/	
VITA 32-199x Processor PMC Standard for Processor PMC Mezzanine Cards VITA (VMEbus International Trade Association)	ANSI/VITA32-199x
IEEE http://standards.ieee.org/catalog/	
IEEE - Common Mezzanine Card Specification (CMC) Institute of Electrical and Electronics Engineers, Inc.	P1386 Draft 2.1
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc.	P1386.1 Draft 2.1
PCI Special Interest Group (PCI SIG) http://www.pcisig.com/	
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.0, 2.1, 2.2 PCI Special Interest Group	PCI Local Bus Specification
IBM for Specifications http://www.ibm.com	
PowerPC Reference Platform (PRP) Specification, Third Edition, Version 1.0, Volumes I and II International Business Machines Corporation	MPR-PPC-RPU-02
PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture (CHRP), Version 1.0 Literature Distribution Center for Motorola Telephone: 1-800- 441-2447 FAX: (602) 994-6430 or (303) 675-2150 http://e-www.motorola.com/webapp/sps/library/ E-mail: ldcformotorola@hibbertco.com OR	

Table B-3. Related Specifications (Continued)

Document Title and Source	Publication Number
Morgan Kaufmann Publishers, Inc. Telephone: (415) 392-2665 Telephone: 1-800-745-7323 http://www.mkp.com/books_catalog/	
Electronic Industries Alliance http://www.eia.org/	
Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange; Electronic Industries Alliance; http://global.ihs.com/index.cfm (for publications)	TIA/EIA-232 Standard
PCI Industrial Manufacturers Group (PICMG) http://www.picmg.com/	
Compact PCI Specification	CPCI Rev. 2.1 Dated 9/2/97

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