

VxWorks 5.5/Tornado[™] 2.2

Rel 3.3

for PMC280

Release Notes

P/N 223487 Revision AC

July, 2004

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Contents of the BSP Package

The package contains the below mentioned deliverables

- 1. frcPMC280_VxWorks_src_REL_3_3.tar
 - a. PMC280 Source code for the BSP

2.frcPMC280_VxWorks_bin_REL_3_3.tar

Contains the images for vxWorks5.5/Tornado2.2

a. vxWorksDual.st_rom.bin	 stand alone image in binary format for the Dual CPU Variants.
b. bootromDual.bin	- minimum boot rom image in
	binary format for the Dual CPU
	Variants.
c. vxWorksDual.st	- complete vxWorks netload image with symbol table for the Dual
	CPU Variants.

3.vxWorks Installation Guide

a. 221087 410 000	- This documentation for the BSP	
	describes the installation of the BSP	

4.vxWorks Programmer's Guide

a. 221088 410 000	- This documentation describes all	
	the routines exported by the BSP.	

Features Supported in This Release

The features supported in vxWorks BSP Release 2.2/3.3 for PMC280:

- 1. Board Initialization
 - a. Initialize all the CPU registers (like IBAT, DBAT, LR, MSR, etc)
 - b. Initialize CPU interface registers of MV64360.
 - c. Configure Memory Controller registers of MV64360.

- d. Set up initial stack pointer
- e. Sets up the board's memory map by configuring MV64360 decode registers.
- f. Configure PCI interface registers of MV64360.
- g. Detect PCI devices and assign memory and I/O resources as well as interrupt numbers (depending upon whether the board operates as a monarch or a non-monarch)
- h. Initialize and configure MV64360's Interrupt controller to route PCI and other device interrupts.
- i. Initialize all on-board devices by calling the driver initialization functions. This would include (but not limited to) initialization of MPSC ports, Gigabit Ethernet, PCI Ethernet Adapters (if present) etc.
- j. Initialize and enable L1/L2 cache
- k. Enable Interrupts.
- 2. On-board devices support
 - a. Boot Flash
 - b. User Flash
 - c. I2C
 - d. Serial E2PROM
 - e. RTC
 - f. VPD
 - g. PCI subsystem id and subsystem vendor id as part of PCI configuration
 - h. MPSC serial driver
 - i. 10/100/1000 Mbps Ethernet 2 numbers
- 3. Boot from PCI (for Variant B, F only)
- 4. Serial Console for both CPUs
- 5. Monarch and Non-Monarch operation
- 6. Memory Partitioning
- 7. Loosely coupled SMP operation
- 8. PCI Network Drivers
 - a. Intel eepro100/82559 Ethernet Adapter
 - b. FORCE Athena (82543 based) Gigabit Adapter
- 9. Interrupt routing
- 10. Interrupts in non-monarch mode
- 11. Board Information Block
- 12. Boot Flash utility
- 13. MAC address programming to EEPROM.
- 14. 30 MB ram disk
- 15. FTP server support
- 16. Watchdog support
- 17. Board + assembly revision detection.

Revision History

P/N	Revision	Date	Description
223487 410 000	AA	June, 2004	Release 3.3
223487 410 000	AB	July, 2004	Release 3.3 Added details of known problems
223487 410 000	AC	July, 2004	Release 3.3 Memory Test Added

Changes from Release 3.2 to 3.3

• Added support for Dual CPU with 1 GB of memory.

Changes from Release 3.1 to 3.2

- Fixed the cacheDmaMalloc issue in Dual CPU BSP.
- Code cleanup.
- New variant detection for I and J.

Changes from Release 3.0 to 3.1

- Cache fix for cacheDmaMalloc().
- Memory autosizing.
- Flash autosizing
- ALtivec support.
- Watchdog support.
- Variant identification for all 8 variants.
- Subsystem ID for all variants.
- sysInByte and sysOutByte corrections.
- Netload support.
- user flash driver modification to support PMC280 Rev B.

Known Problems

• Other than PMC280, any other external host will not be able to read the VPD of PMC280.

Restrictions

The restrictions in this release are detailed below:

- 1. Warm boot is not supported. The Ctrl-X or reboot commands will issue a hard reset to the board instead of providing a warm boot.
- 2. For the integrated 82559 driver to work, the cable has to be inserted into the card before the driver gets loaded on the BSP.
- 3. IDE Build is not supported as a part of this release.

Product Error Report

Product:	Serial No.:			
Date Of Purchase:	Originator:			
Company:	Point Of Contact:			
Tel.:	Ext.:			
Address:				
	r			
	Sec. 1			
Present Date:				
Affected Product:	Affected Documentation:			
🗅 Hardware 🗅 Software 🗅 Systems	🗅 Hardware 🗅 Software 🕒 Systems			
Error Description:				
This Area to Be Completed by Force Computers:				
Date:				
PR#:				
Responsible Dept.: Marketing Production				
Engineering 🛥 🖬 Board 🖬 Systems				

Send this report to the nearest Force Computers headquarter listed on the back of the title page.