PPMC-280

Installation Guide

P/N 221086 Revision AA
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Using This Guide

This Installation Guide explains how to install, use, and troubleshoot problems associated with PPMC-280.
This Installation Guide is intended for users qualified in electronics or electrical engineering. It is presumed that you have the pre-requisite knowledge and working experience with:

- Peripheral Component Interconnect (PCI) bus
- PCI Mezzanine Cards (PMCs)
- Processor PCI Mezzanine Cards (PPMCs)
- PowerPC

Conventions

Notation	Description
57	All numbers are decimal numbers except when used with the notations described below
00000000_{16}	Typical notation for hexadecimal numbers (digits are 0 through F), e.g. used for addresses and offsets
0000_2	Same for binary numbers (digits are 0 and 1)
x	Generic use of a letter
n	Generic use of numbers
n.nn	Decimal point indicator is signaled
Bold	Character format used to emphasize a word
`Courier`	Character format used for on-screen output
Courier+Bold	Character format used to characterize user input
Italics	Character format for references, table, and figure descriptions
<text>	Typical notation used for variables and keys
[text]	Typical notation for buttons
...	Repeated item
. . .	Omission of information from example/command that is not necessary at the time being
..	Ranges

Notation	Description
:	Extents
|	Logical OR
Note:	No danger encountered. Pay attention to important information marked using this layout.
Caution 	Possibly dangerous situation: slight injuries to people or damage to objects possible
Danger 	Dangerous situation: injuries to people or severe damage to objects possible

Abbreviations

BIB	Board Information Block
BSP	Board Support Package
CL	CAS Latency for SDRAM
CMC	Common Mezzanine Card
CPCI	Compact Peripheral Component Interconnect
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
DDR	Dual Data Rate
ECC	Error Correcting Code
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIA	Electronic Industries Association
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
ESD	Electrostatic discharge
FAE	Field Applications Engineer
FCC	Federal Communications Commission

GPP	General Purpose Port
IC	Integrated Circuit
I^2C	Inter-Integrated Circuit
IDMA	Internal Direct Memory Access
IEEE	International Electrical and Electronics Engineers
I^2C	Inter Integrated Circuit
I/O	Input/Output
ISP	In System Programmability
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LFM	Linear Feet per Minute
LSP	Linux Support Package
MAC	Message Authentication Code/Media Access Control
MTBF	Mean Time Between Failures
NMI	Non-Maskable Interrupt
NVRAM	Non-Volatile Random Access Memory
PCB	Printed Circuit Board
PBGA	Plastic Ball Grid Array
PCI	Peripheral Component Interconnect
PMC	PCI Mezzanine Card
PPMC	Processor PCI Mezzanine Card
RefDes	Reference Designator
RTC	Real Time Clock
R/W	Read/Write
SDMA	Serial DMA
SDRAM	Synchronous Dynamic Random Access Memory
SMI	Serial Management Interface
SMP	Symmetric Multi-Processing
SRAM	Static Random Access Memory
TFTP	Trivial File Transfer Protocol

TSOP	Thin Small Outline Package
UART	Universal Asynchronous Receiver Transmitter
UL	Underwriters Laboratories Inc.®
VITA	VMEBus International Trade Association
Y2K	Year 2000

Revision History

Order Number	Revision	Date	Description
221086 420 000	AA	October 2003	Initial Release

Other Sources of Information

For further information refer to the following documents:

Company	Web Address	Document
Motorola	www.motorola.com	PowerPC MPC7450 RISC Microprocessor Familiy user manual , 10/2002, Revision 2.2
		RISCWatch Debugger for PowerPC Processors
		PowerPC MPC7457 RISC Microprocessor Hardware specification, 7/2003, Revision 2
Philips Semiconductors	www.philips.com	I^2C bus specification, Version 2.1, January 2000
Marvell Technology		MV64360/1/2 system controller for PowerPC Processors-datasheet, Revision B, January 13, 2003
Broadcom©Corporation	www.broadcom.com	BCM5421 Datasheet
JEDEC Solid State Technology Association		Double Data Rate (DDR) SDRAM specification, JESD79, June 2000

In addition, refer the following documents:

- Processor PMC Standard, VITA32-2003, Revision 1.0a, April 2003: VITA Standards Organization
- Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC, P1386.1/Draft2.4, January 12, 2001: IEEE
- Draft Standard Physical and Environmental Layers for a Common Mezzanine Card: CMC, P1386/Draft2.4a, March 21, 2001: IEEE
- PCI Local Bus Specification, Revision 2.2, June 8, 1998: PCI Special Interest Group

Safety Notes

This section provides safety precautions to follow when installing, operating, and maintaining PPMC-280.

We intend to provide all necessary information to install and handle PPMC-280 in this Installation Guide. However, as the product is complex and its usage manifold, we do not guarantee that the given information is complete. If you need additional information, ask your Force Computers representative.

PPMC-280 has been designed to meet the standard industrial safety requirements. It must only be used in its specific area of office telecommunication industry and industrial control.

PPMC-280 is intended for use with a UL listed chassis that has adequate instructions on installation of PMC accessories.

Only personnel trained by Force Computers or persons qualified in electronics or electrical engineering are authorized to install, maintain, and operate PPMC-280. The information given in this manual is meant to complete the knowledge of a specialist and must not be taken as replacement for qualified personnel.

EMI

The EMI limits are designed to provide reasonable protection against harmful interference when the board is operated in a commercial, business, or industrial environment.
The board generates and uses radio frequency energy. If not installed properly and used in accordance with this Installation Guide, the board may cause harmful interference to radio communications. Operating the board in a residential area is likely to cause harmful interference, in which case, users will be required to correct the interference at their own expense.

ESD

PPMC-280 contains very delicate Integrated Circuit (IC) chips. To protect them against damage from Electrostatic Discharge (ESD), follow the described precautions:

- **Ground yourself properly before removing the board from the antistatic bag**

- **Use a grounded wrist strap before handling system components. If you do not have one, touch both hands to a safely grounded object or to a metal object such as the system case**
- **Hold the board by its edges and do not touch the components, IC chips, connectors and leads**

Whenever components are separated from the system, place components on a grounded antistatic pad or the original packaging bag

Installation

Electrostatic discharge and incorrect board installation and removal can damage circuits or shorten their life. Therefore:

- **Before installing or removing the board, read “Action Plan” page 2-3**
- **Before touching boards or electronic components, make sure that you are working in an ESD-safe environment.**
- **Before installing or removing an additional device or module, read the respective documents.**

Operation

While operating the board, ensure that the environmental and power requirements are met.

Do not operate the product outside the specified environmental limits. High humidity and condensation may cause short circuits. Make sure the product is completely dry and there is no moisture on any surface before applying power. Do not operate the product below 0°C.

When operating the board in areas of electromagnetic radiation, ensure that the board is bolted on the carrier card and the system is shielded by enclosure.

Make sure that contacts and cables of the board cannot be touched while the board is operating.

Replacement/Expansion

Only replace or expand components or system parts with those recommended by Force Computers. Otherwise, you are fully responsible for the impact on EMC and the possibly changed functionality of the product.

Check the total power consumption of all components installed (see the technical specification of the respective components). Ensure that any individual

output current of any source stays within its acceptable limits (see the technical specification of the respective source).

Environment

Always dispose off old boards according to your country's legislation, if possible, in an environmentally acceptable way.

1

Introduction

Product Overview

PPMC-280 is a Processor PMC (PPMC) dual-processing card based on the MPC7447 PowerPC and MV64360 system controller.

The standard variant of PPMC-280 (120092) supports the following features. For features supported by other variants, refer to Table 1 “Variants of PPMC-280” page 1-4.

- Dual Motorola PowerPC® MPC7447 processors
  - 1GHz core CPU frequency
  - 133 MHz front-side bus
- Marvell Atlantis MV64360 System Controller
- 512 MB Dual Data Rate (DDR) Synchronous Dynamic Random Access Memory (SDRAM)
  - 133 MHz bus frequency (266 MHz data rate)
- Flash
  - 64 MB user-programmable flash
- PCI2.2 interface
  - Universal signaling
  - 64-bit, 66 MHz
- Two Gigabit Ethernet ports accessible through the PMC I/O P4 Connector
- Two RS-232 Serial Ports accessible through the PMC I/O P4 Connector

In addition, PPMC-280 also provides a Y2K-compliant Real Time Clock (RTC) and serial EEPROMs for board configuration and identification.

PPMC-280 Variants

The PPMC-280 variant information is detailed in the table given in the following page.

Table 1: *Variants of PPMC-280*

Features	Description	Variant 120092	Variant 120048	Variant 120047	Variant 120049	Variant 120093	Variant 120094	Variant 120791	Variant 120673
CPU(s)	MPC7447 PowerPC	Dual	Dual	Single	Single	Single	Single	Single	Dual
Core speed	CPU core frequency	1 GHz	1 GHz	733 MHz	1 GHz	1 GHz	733 MHz	1 GHz	1GHz
System Controller	Marvell Discovery -II MV6436X	MV64360	MV64362	MV64360	MV64360	MV64360	MV64362	MV64360	MV64360
FSB Speed	Frequency of the front-side/host bus	133 MHz	133 MHz	133 MHz	133 MHz	133 MHz	133 MHz	133 MHz	133 MHz
Memory	On-board DDR266 SDRAM with ECC	512 MB	512 MB	512 MB	1 GB	512 MB	128 MB	256 MB	1 GB
Flash Memory	On-board user flash (Intel Strata Flash)	64 MB	None	64 MB	64 MB	64 MB	None	None	64 MB
	1 MB boot flash	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes
PCI2.2 Interface	3.3V/5V, 64-bit, 66 MHz interface	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Ethernets	Gigabit ports accessible through PMC P4	Two (GbE0, 1)	One (GbE0)	Two (GbE0, 1)	Two (GbE0, 1)	Two (GbE0, 1)	One (GbE0)	Two (GbE0, 1)	Two (GbE0, 1)
Boot Mode	PPMC-280 can boot from boot flash or over PCI; defualt boot mode is variant dependent	Boot Flash	PCI	Boot Flash	Boot Flash	Boot Flash	PCI	Boot Flash	Boot Flash
PCI Subsystem ID	Assigned to the variant by Force Computers	0xB283	0xB281	0xB280	0xB282	0xB284	0xB285	0xB286	0xB287

Table 1: *Variants of PPMC-280*

Features	Description	Variant 120092	Variant 120048	Variant 120047	Variant 120049	Variant 120093	Variant 120094	Variant 120791	Variant 120673
Heat Sink	Standard is compliant to CMC mechanical specifications	Standard (P/N 221719)	Non-Standard (P/N 221421)	Non-Standard (P/N 221421)	Non-Standard (P/N 221421)	Standard (P/N 221719)	Non-Standard (P/N 221421)	Standard (P/N 221719)	Standard (P/N 221719)
Front panel bezel	-	Yes	No	No	No	Yes	No	No	Yes
* CMC Compliance	Full Conformance to CMC mechanical specifications	Yes	No	No	No	Yes	No	Yes	No
VxWorks T1.0.1	Dual CPU = Loosely Coupled-SMP	No	Yes	No	No	No	Yes	No	No
VxWorks T2.2	Dual CPU = Loosely Coupled-SMP	Yes	No	No	No	Yes	No	Yes	Yes
Linux – Monta Vista	Dual CPU = SMP Single CPU = LSP	Yes	No	No	No	Yes	No	No	Yes
Linux - Kernel. Org	Dual CPU = SMP Single CPU = LSP	No	No	Yes	Yes	No	No	No	No
Power-Boot	On CPU0 only	Yes	No	Yes	Yes	Yes	No	Yes	Yes

NB: * see “Physical Specifications” page 1-12 for details.

Software Support

PPMC-280 supports VxWorks and Linux operating systems (see “Variants of PPMC-280” page 1-4). Refer to the latest VxWorks /Tornado™ BSP for PPMC-280 Installation Guide (Order Number 221087 410 000), VxWorks /Tornado™ BSP for PPMC-280 Programmer’s Guide (Order Number 221088 410 000) and Linux Board Support Package for PPMC-280 installation guide(Order Number 221522 410 000).

Functional Block Diagram

The functional block diagram of PPMC-280 is shown in Figure 1.

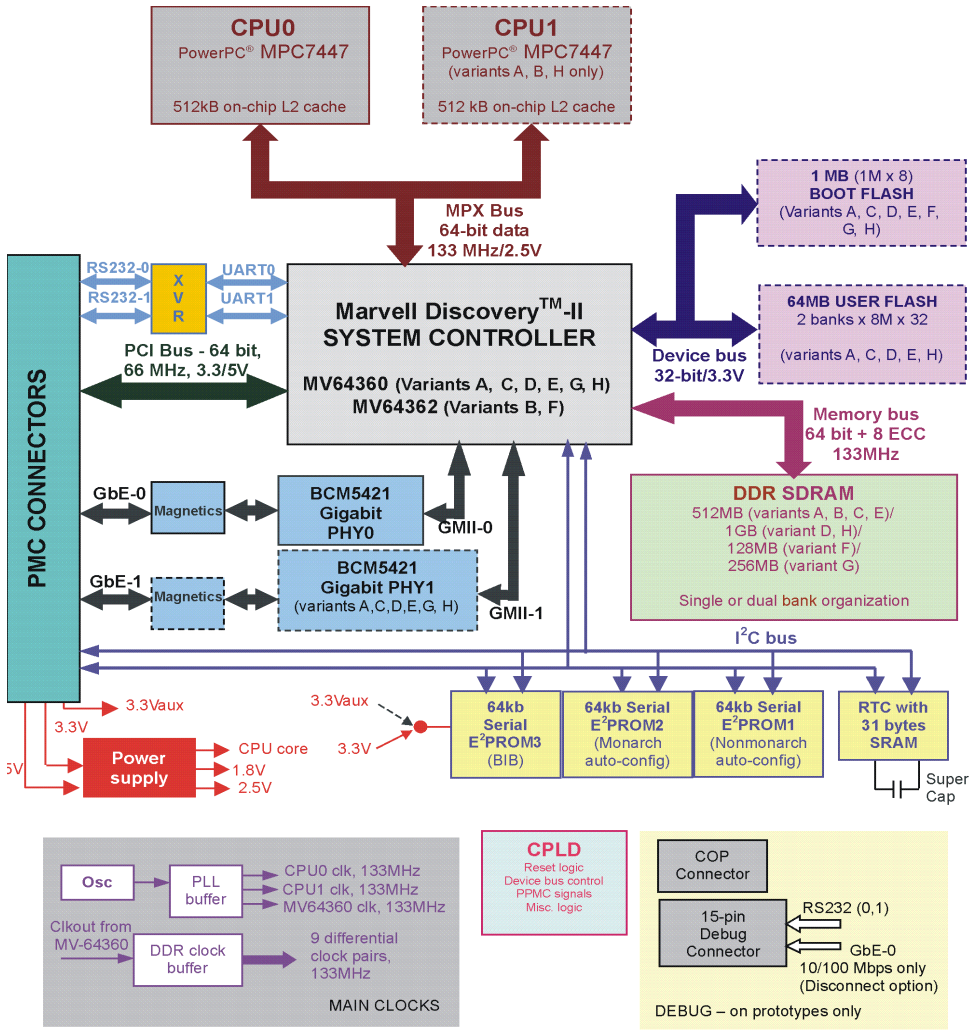


Figure 1: *Functional Block Diagram*

Note: Variant A=120092; B=120048; C=120047; D=120049; E=120093; F=120094; G=120791; H=120673

Board Layout

This Installation Guide refers to two sides (top and bottom) of PPMC-280:

- You can identify bottom side by the CPU, heat-sink, Ethernet Magnetics, and PMC connectors.
- You can identify top side by Super-capacitor.

The top and bottom layout of the PPMC-280 are shown in Figure 2 and Figure 3 respectively. See figure “Controls, Indicators and Connectors” (Chapter 4) and figure “Devices and Other Functions” (Chapter 3) for detailed information.

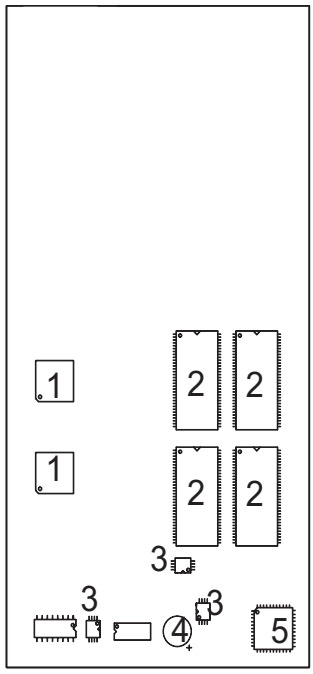


Figure 2: *Top Layout of PPMC-280 Showing Major Components*

The major components numbered in Figure 2 are listed here:

1. Ethernet PHY
2. DDR SDRAMs
3. EEPROMs
4. Super-capacitor

5. CPLD

The bottom layout of PPMC-280 is shown in Figure 3.

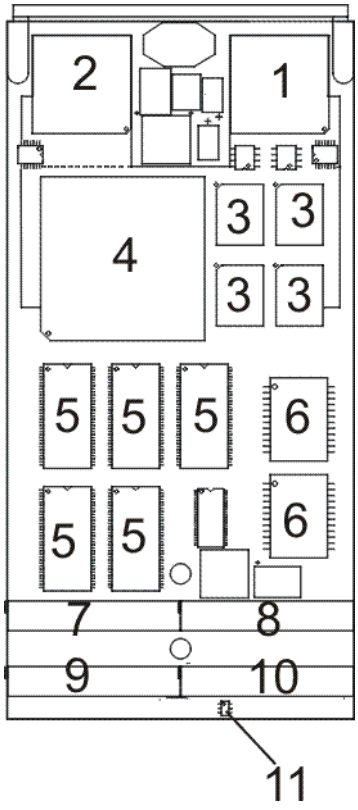


Figure 3: *Bottom Layout of PPMC-280 Showing Major Components*

The major components numbered in Figure 3 are listed here:

1. CPU 0 (On single-CPU variants 120047, 120049, and 120093, only CPU 0 is present.)
2. CPU 1 (On single-CPU variants 120094 and 120791, only CPU 1 is present)
3. User Flash
4. System Controller
5. DDR SDRAMs
6. Ethernet Magnetics
7. P1

8. P3
9. P2
10. P4
11. RTC

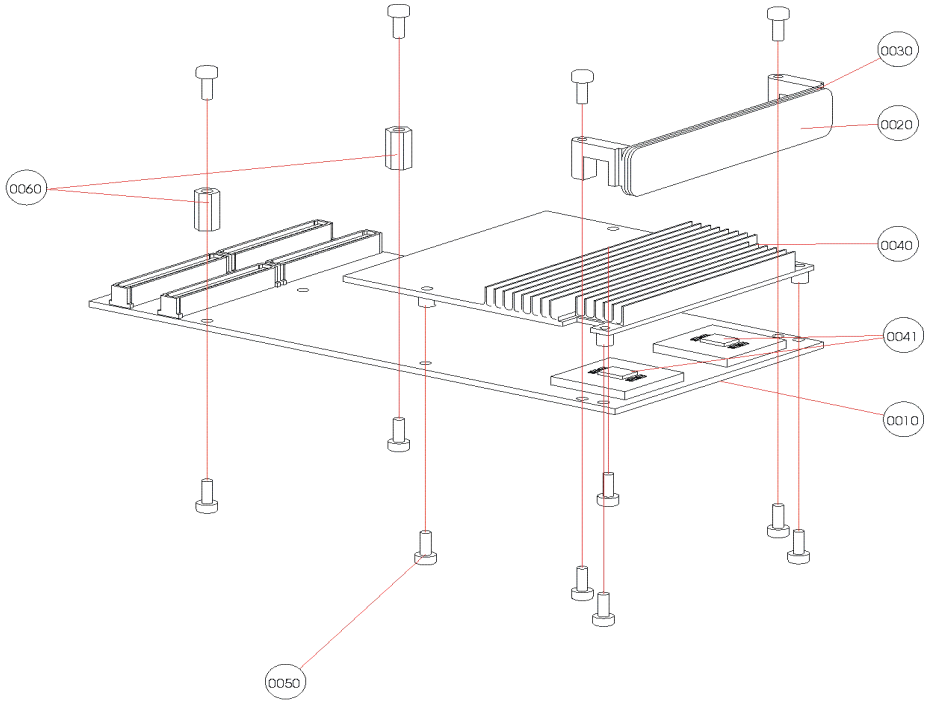


Figure 4: *Top Assembly exploded view for 120092 (variants 120093, 120791 and 120673 use the same heat sink)*

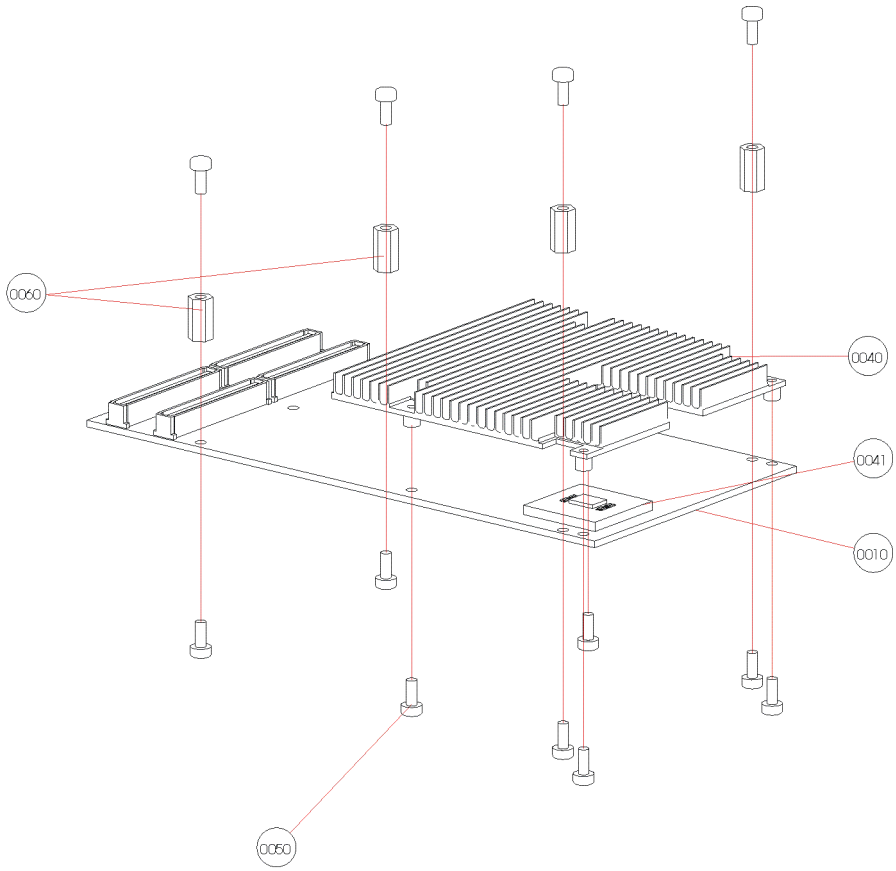


Figure 5: *Top assembly exploded view for 120049 (variants 120047, 120048 and 120094 use the same heat sink)*

Standard Compliance

PPMC-280 will meet the following standards:

Table 2: *Standard Compliance (PPMC-280 is yet to be qualified in the following standards)*

Standard	Description
IPC	Quality level requirements
IEC 68-2-1/2/3/13/14	Climatic environmental requirements.The PPMC-280 can be used in a restricted temperature range only. See "Environmental Requirements" on page 2-9 for details.
IEC 68-2-6/27/32	Mechanical environmental requirements
UL 1950 (standard CompactPCI chassis)	Legal safety requirements
FCC Part 15, Class A	EMI Requirements on System Level
EN 55022:1998, Class A	EMI Requirements on System Level
EN 55024:1998 IEC 61000-4-2 IEC 61000-4-3 IEC 61000-4-4 IEC 61000-4-5 IEC 61000-4-6 IEC 61000-4-8	EMS Requirements on System Level

The features relevant to PMC/Processor PMC standards that are supported by PPMC-280 are:

- 64-bit, 66 MHz, PCI 2.2-compliant interface to an IEEE P1386.1 PMC or VITA 32-199x Draft 0.5 Processor PMC compliant carrier board
- Universal signaling PCI interface (supporting both 3.3V and 5V)
- Four 64-pin EIA E700 AAAB connectors as per the EIA standard. These PMC connectors labelled P11, P12, P13, P14 (as entailed by the CMC specification P1386) are referred to as P1, P2, P3, and P4 in this Installation Guide.
- Monarch and Non-Monarch Operating Modes

Physical Specifications

Table 3: *Physical Specifications*

Variant#	Standoff height	Total height	Width	Depth	Weight	Comments
120092	10mm	13.5mm	74mm	149mm	190g	Includes bezel
120048	10mm	13.5mm	74mm	149mm	220g	Note (b)
120047	15mm	18.5mm	74mm	149mm	200g	Note (b)
120049	15mm	19.25mm	74mm	149mm	212g	Note (b)
120093	10mm	13.5mm	74mm	149mm	180g	Includes bezel
120094	10mm	13.5mm	74mm	149mm	210g	Note (b)
120791	10mm	13.5mm	74mm	149mm	160g	-
120673	10mm	14.25mm	74mm	149mm	200g	Includes bezel; Note (c)

(a) "Height" is measured as the vertical distance of the top of the tallest component on the top side (CMC side-2) of the PMC card from the carrier card. Hence, it includes the standoff height, the PCB thickness and the tallest component height on the top side.

(b) Variants 120048, 120047, 120049 and 120094 do not conform to the bottom-side (CMC side-1) component height specification, because the heat sink encroaches 44 mm into the 4.7mm maximum height envelope in the component area. See Figure 6:.

(c) Variant 120673 does not conform to the top-side (CMC side-2) component height specification for a 10mm stacking height card, since it uses stacked 1Gb DDR modules.

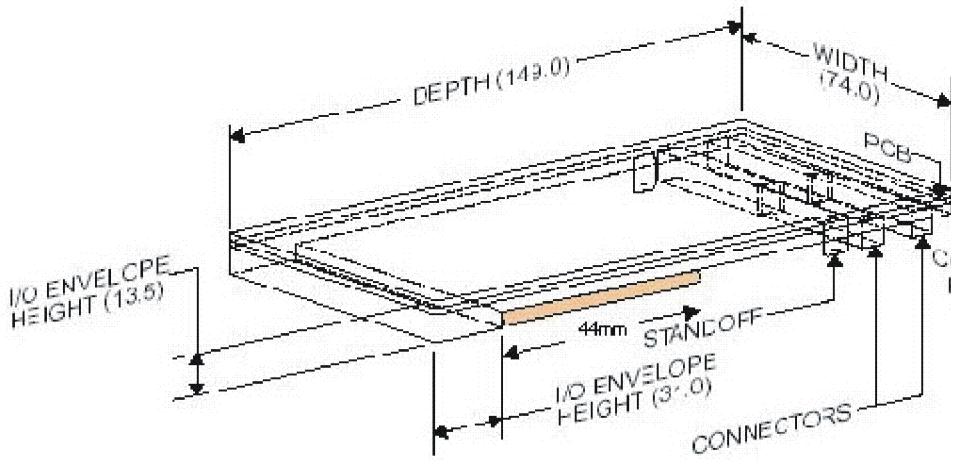


Figure 6: *Extent of deviation (44 mm) from CMC component envelope specification due to the non-standard heatsink(P/N 221421) used on variants 120048, 120049, 120047, 120094.*

Connector Types

PMC connectors: Four 64-pin EIA E700 AAAB connectors, current rating 1A/pin.

MTBF

Standard conditions for MTBF calculation

- Nonmobile operation
- Ground benign Gb
- 40°C mean ambient temperature
- No fans
- Continuous operation 8760 hours per year

Variant	General description	Minimum MTBF
120092/120048/120673	Dual-CPU variants	347,826 hours
120093/120047/120791/120094	Single-CPU, single-stack memory	422,476 hours
120049	Single-CPU, dual-stack memory	398,248 hours

Ordering Information

Order Numbers

When ordering PPMC-280, use the order numbers given below.

The order numbers are provided in Table 4.

Table 4: *Ordering Information Excerpt* [1)]

Order No.	Name	Description
120092	PPMC-280 Variant-120092	Dual 7447, 1GHz, 512MB, 64MB flash, Discovery II MV64360 – 2 GigE, Boot ROM boot
120048	PPMC-280 Variant-120048	Dual 7447, 1GHz, 512MB, 0MB Flash, Discovery II MV64362 – 1 GigE, PCI boot
120047	PPMC-280 Variant-120047	Single 7447, 733 MHz, 512MB, 64MB flash, Discovery II MV64360 – 2 GigE, Boot ROM boot
120049	PPMC-280 Variant-120049	Single 7447, 1GHz, 1GB, 64MB Flash, Discovery II MV64360 – 2 GigE, Boot ROM boot
120093	PPMC-280 Variant-120093	Single 7447, 1GHz, 512MB, 64MB flash, Discovery II MV64360 – 2 GigE, Boot ROM boot
120094	PPMC-280 Variant-120094	Single 7447, 733 MHz, 128MB, 0MB flash, Discovery II MV64362 – 1GigE, PCI boot
120791	PPMC-280 Variant-120791	Single 7447, 1 GHz, 256 MB, 0 MB flash, Discovery II MV64360 – 2 GigE, Boot ROM boot
120673	PPMC-280 Variant-120791	Dual 7447, 1GHz, 1GB, 64MB Flash, Discovery II MV64360 – 2 GigE, Boot ROM boot

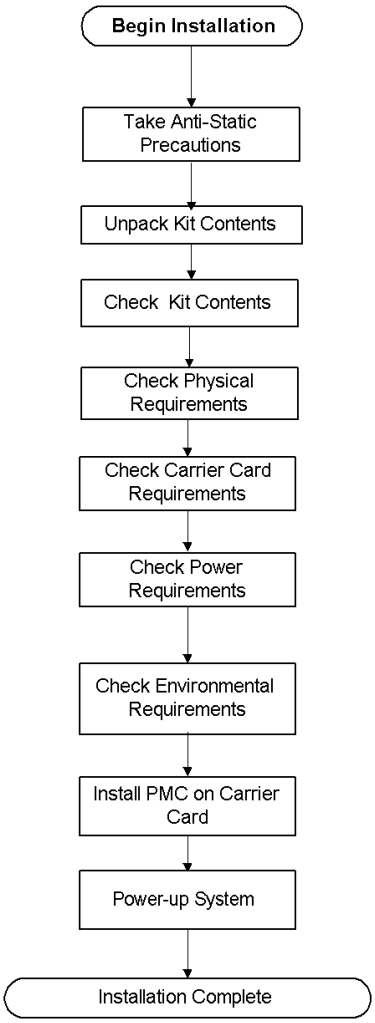
1) Status: October 2003

2

Installation

Action Plan

This chapter details the installation procedure of PPMC-280 on the carrier card. To install PPMC-280 on the carrier card, follow the steps shown in the diagram below.



Preparing for Installation

The following sections explain how to prepare for an installation. Topics include:

Note: Ensure that there is adequate airflow as per the recommendations, see "Thermal Requirements" page 2-10.

Taking Antistatic Precautions

Caution

When handling circuit boards and associated internal computer components, use an antistatic wrist strap or wear isolation gloves.

In addition to using an antistatic wriststrap or wearing isolation gloves, consider the following precautions:

- Do not allow a circuit board or other components to make contact with non-conductors, including your clothing.
- Keep loose circuit boards inside or on top of conductive plastic bags.
- Before touching a loose circuit board or component, discharge static electricity.

Unpacking Kit Contents

Start preparing for your installation by unpacking the card kit.

1. Verify that the order numbers on labels of your kit carton match the numbers for the product you ordered. If the order numbers do not match, contact your Force Computers sales representative.
2. Locate and put on an antistatic wriststrap.

3. Clip the wire attached to the wriststrap to the frame of your system chassis.
4. Remove all items from the carton.
5. Remove hardware components from conductive plastic bags in which they were packaged, and place components on the bags.

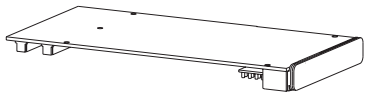
Note: Store the original packaging material in case a factory return is necessary.

The details of the kit contents are listed in Table 5 “Package Contents” on page 2-5.

Checking Kit Contents

Table 5 lists the contents of the card kit. Verify that the material you unpacked matches contents listed in Table 5.

Table 5:*Package Contents*

Part	Part Name	Part Number/Order Number
	Installation Guide	Order Number 221086 420 000 AA
	PPMC-280	120092/120047/ 120048/120049/120093/120094/120791/ 120673

Physical Requirements

PPMC-280 features the industry-standard PMC form-factor. The card must be placed on a carrier card.

Carrier Card Requirements

PPMC-280 is to be plugged into a carrier card that meets the following requirements:

- Carrier cards to support PPMC-280 should be compliant with the CMC/PMC standard specifications for carrier cards.
- If PPMC special signals are required, the carrier card should implement changes required by the Processor PMC specification. In order to take advantage of the special Processor PMC signals (MONARCH#, EREADY, RESETOUT#), the carrier card must support these, with a weak pull-up (5kohm) for EREADY.
- PCI clock and reset signals must be provided by the carrier card. All necessary PCI signal pull-ups should be provided by the carrier card. Since PCI arbitration is not provided by PPMC-280, another participant in the system should provide the PCI arbitration.
- If the carrier card uses the PMC I/O connector (P4), ensure that P4 is pin-compliant and voltage-compliant with the corresponding signals on PPMC-280.
- If the carrier card interfaces to the I^2C bus on PPMC-280, ensure that I^2C address clash is prevented.
- The carrier card needs to supply 3.3V and 5V power to PPMC-280:
  - Mandatory: 3.3V ± 5%
  - Mandatory.5V ± 5%
- PCI reset should be asserted by the carrier card for a minimum of 200 ms after 3.3V becomes stable on power-on.
- The following power up-sequencing requirement should be met (see “Power-up sequencing” page 2-7):
  - The 5V rail may power-up prior to the 3.3V rail (case A) or at the same time (case B) as the 3.3V rail. Either case A or case B is recommended.
  - If the 5V rail powers up after the 3.3V rail, the time delay between the two rails powering up should not exceed 10ms (case C).

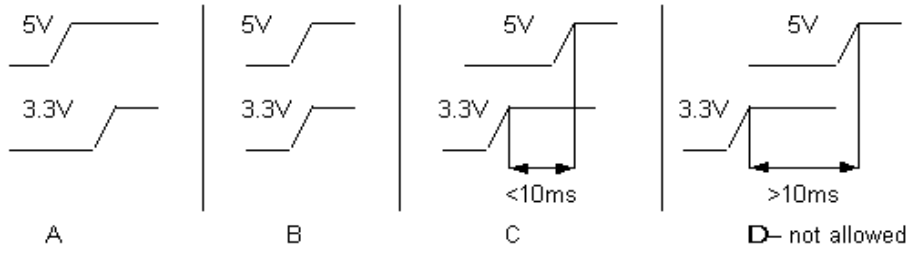


Figure 7: *Power-up sequencing*

- The following power down-sequencing requirement should be met (see "Power-down sequencing" page 2-7):
  - •The 5V rail may power-down after the 3.3V rail (case A) or at the same time as the 3.3V rail (case B). Either case A or case B is recommended.
  - •If the 5V rail powers down before the 3.3V rail, the time delay between the two rails powering down should not exceed 10ms (case D).

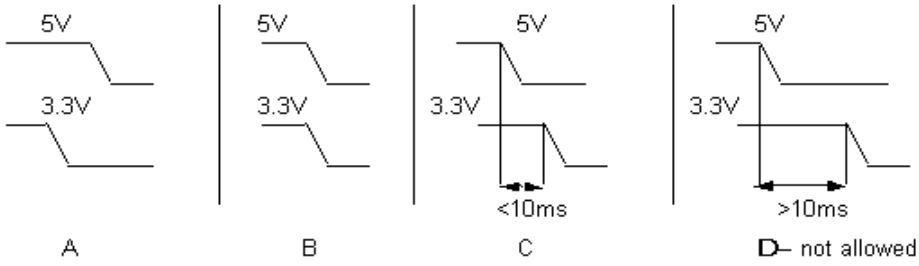


Figure 8: *Power-down sequencing*

- The PMC connectors (receptacles) on the carrier card should have a minimum current rating of 1A/pin.
- Carrier card for 120047/120049 must use 15mm tall PMC receptacles, capable of mating properly with 10mm plugs.

Note:

- **The carrier card has to supply 3.3Vaux if the BIB EEPROM has to be accessed when the main 3.3V rail is powered off.**
- **If you use K2 Test Card (P/N110869) as a carrier card, then the PPMC-270 Transposer card (P/N 120101) has to be used along with it. (Refer to "PPMC-280 Installation on K2 Test Card" on page 2-16).**

Power Requirements

The power requirement of PPMC-280 to be supplied by the carrier card is detailed in Table 6.

Table 6:*Power Requirement for PPMC-280*

TLA#	3.3V power	3.3V current/ pin	5V power	5V current/ pin	Measured instantaneous total power	Worst case total power (Sum of 3.3V and 5V power)
120092	23.76W	0.8A	13.2W	0.44A	33.79W	36.96W
120093	16.86W	0.57A	13.2W	0.44A	26.86W	30.06W
120048	23.76W	0.8A	11.95W	0.4A	32.54W	35.71W
120047	15.12W	0.51A	13.2W	0.44A	25.12W	28.32W
120049	16.86W	0.57A	14.15W	0.47A	28.51W	31.01W
120094	15.12W	0.51A	10.33W	0.34A	25.45W	25.45W
120791	16.86W	0.57A	13.2W	0.44A	26.86W	30.06W
120673	23.76W	0.8A	14.85W	0.5A	35.44W	38.61W

(a) Measured Instantaneous Total Power indicates real power numbers where the application usually does not exercise the 3.3V and 5V power rails simultaneously to the maximum. "Worst case total power" indicates the sum of maximum of measured 3.3V and 5V powers.

(b) Current/pin indicates the current flowing per 3.3V/5V power pin of the PMC connector. The PMC connector is rated for 1A/pin.

(c) Carrier card designers must consider worst-case power.

(d) The 5V power numbers in the table are applicable when both ethernet ports are operating in Gigabit mode. If operating in 10/100 mode, the power reduces by 1.25W per port.

Environmental Requirements

The conditions listed below refer to the surroundings of the board within the user environment.

Note: Operating temperatures refer to the temperature of the air circulating around the board and not to the component temperature.

Caution

Do not operate the product outside the specified environmental limits. High humidity, temperature and condensation may cause short circuits. Make sure the product is completely dry and there is no moisture on any surface before applying power.

Table 7: *Environmental Requirements*

Feature	Operating	Non-Operating
Temperature range	0 to 55^0C	–40° C to 85° C
Temperature change	±0.5 ° C per minute	±1 ° C per minute
Relative humidity	5% to 95% at 40° C (noncondensing)	5% to 95% at 40° C (noncondensing)
Altitude	–300m to 3000m	–300m to 12000m
Shock	5g/11 ms half sine	15g/11 ms half sine
Vibration	10 Hz to 15 Hz: 2 mm amplitude 15 Hz to 150 Hz: 2 g	10 Hz to 15 Hz: 5 mm amplitude 15 Hz to 150 Hz: 5g
Packaging free fall	100 mm/3 axis	1200 mm/all edges and corners

Thermal Requirements

Graphs shown in figures 8 to 12 below are recommended thermal and airflow operating conditions for different variants of PPMC-280. Airflow information can be extracted if the ambient temperature and the core frequency of the CPU are known. Continuous operation of the CPU and MV6436x junctions beyond the specified safety limits shown in the graphs is not recommended.

The airflow (LFM) indicated in the graphs is assumed to be at the lateral entry point of the heat sink.

Note: Measurement conditions applicable to Figures 9-13:

- **PPMC-280 is mounted on a standard CompactPCI® 6U carrier card, and the whole setup is plugged into a CompactPCI® backplane.**
- **The junction temperatures are extrapolated from the measured respective case temperatures and the thermal characteristics of the device.**
- **The "safety limit" of operation for each device is assumed 90% of the maximum specified junction temperature in the device datasheet.**
- **"CPU0" in the graphs for dual-CPU variants refers to the CPU that is closer to the fan.**

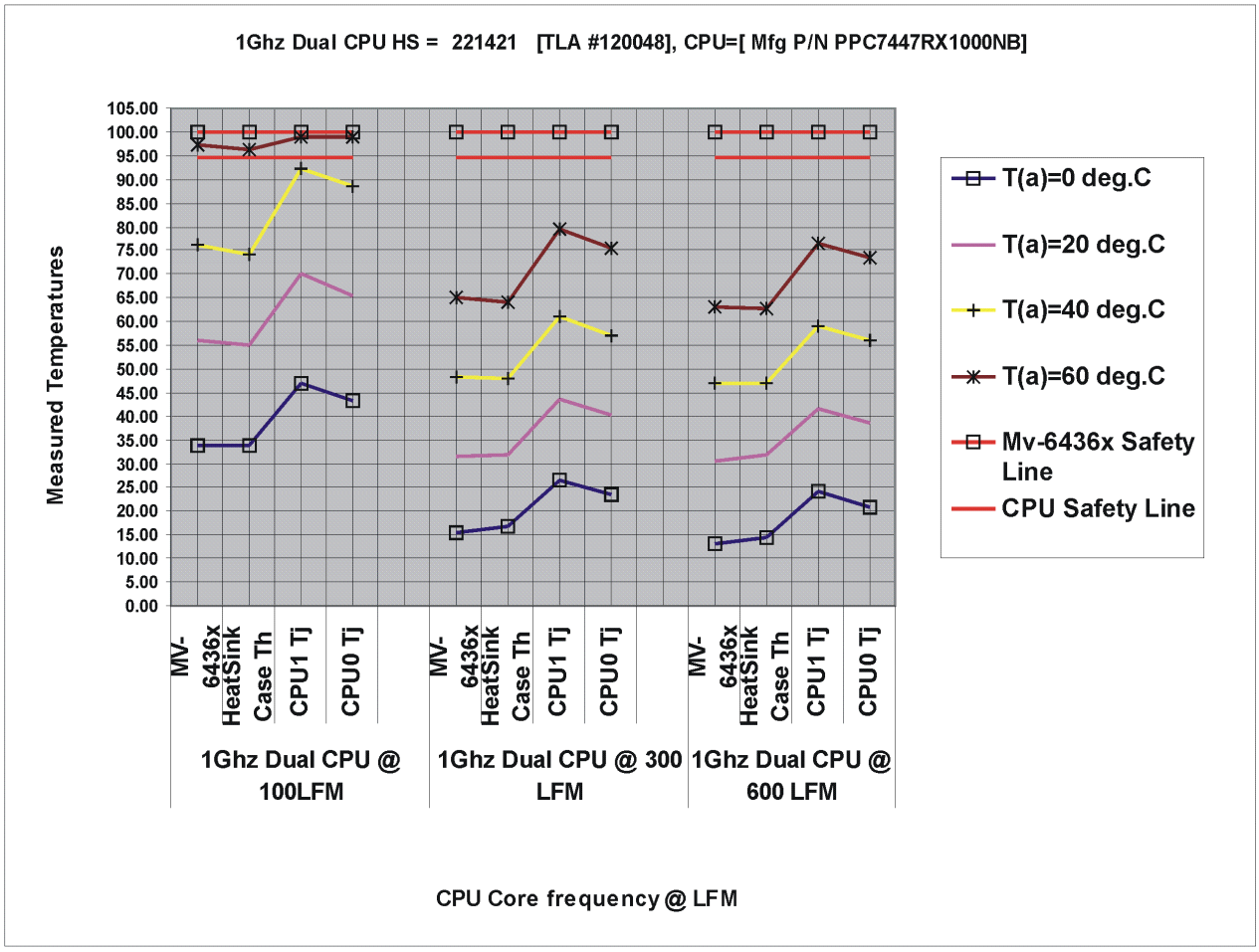


Figure 9: *Airflow and thermal characteristics for 120048.*

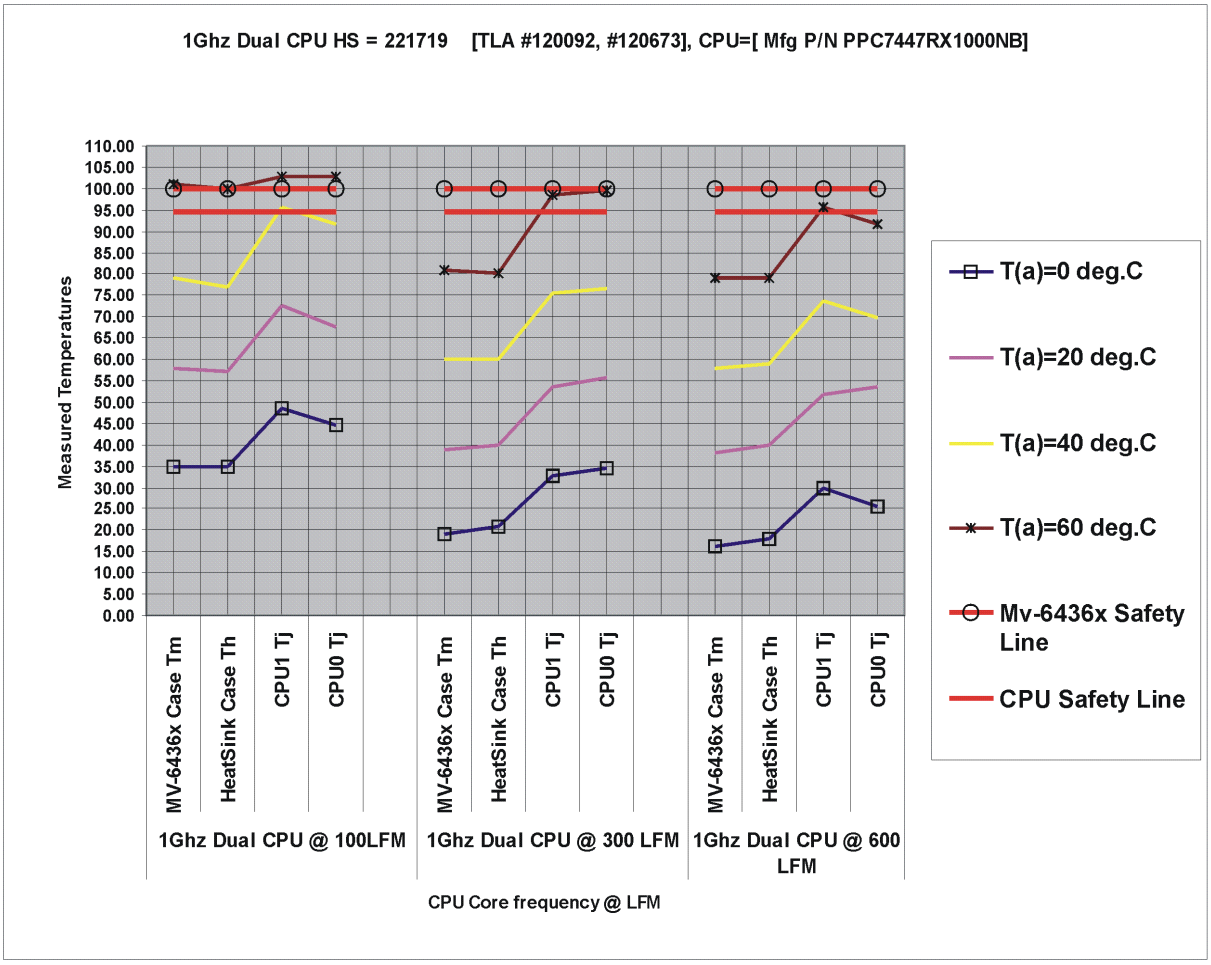


Figure 10: *Airflow and thermal characteristics for 120092, 120673.*

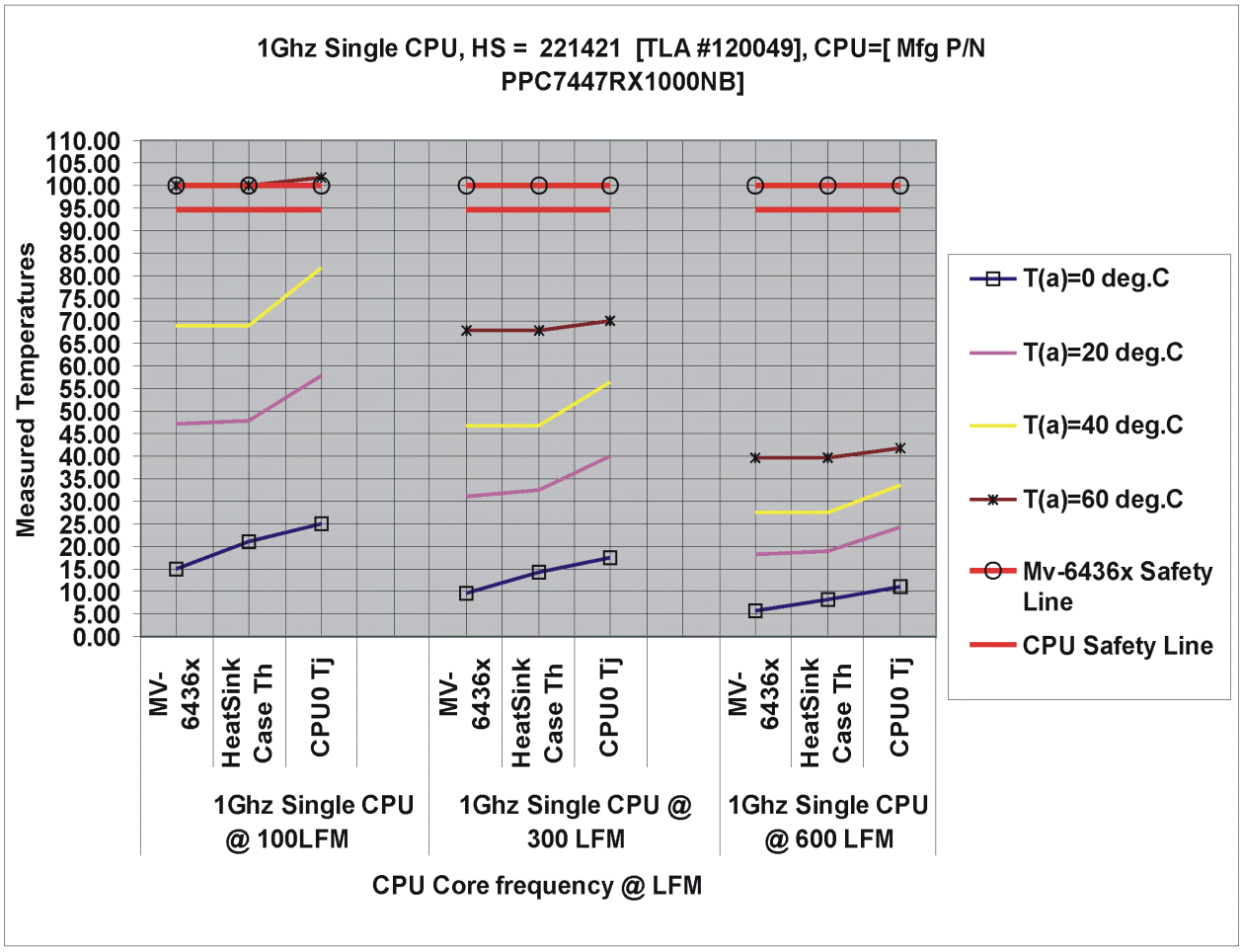


Figure 11: *Airflow and thermal characteristics for 120049.*

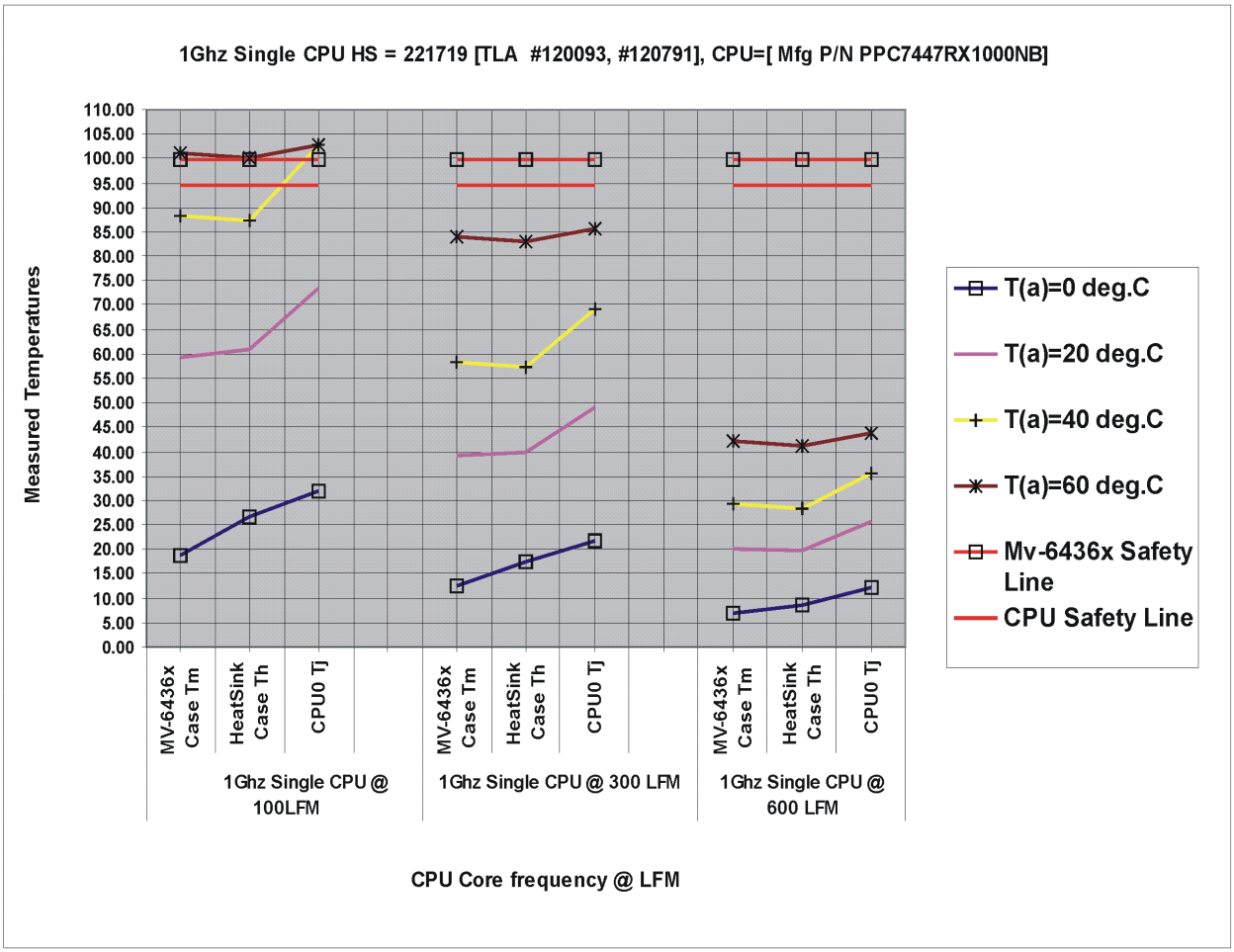


Figure 12: *Airflow and thermal characteristics for 120093, 120791.*

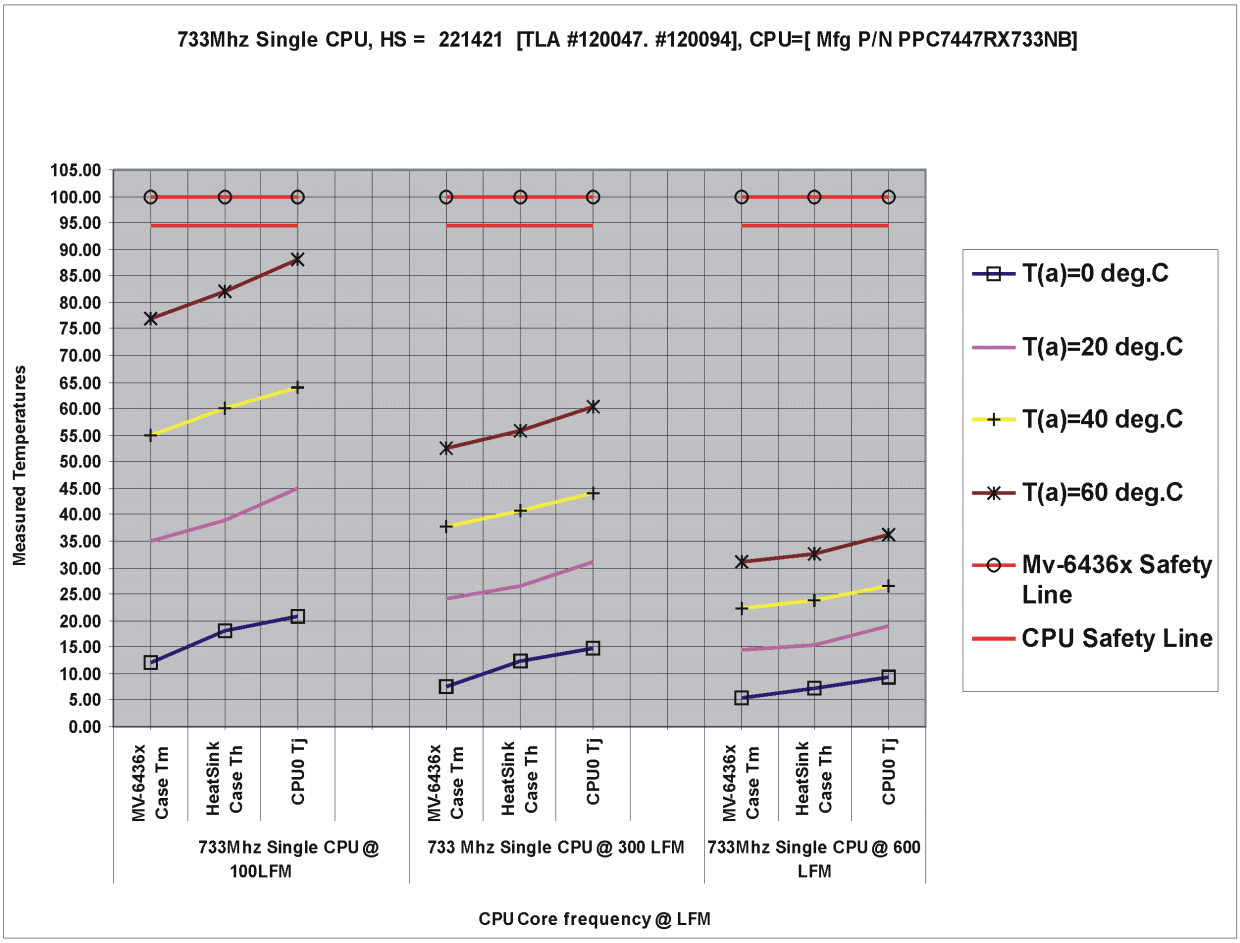


Figure 13: *Airflow and thermal characteristics for 120047, 120094.*

PPMC-280 Installation on K2 Test Card

Follow the steps mentioned in the section below to install PPMC-280 on K2 Test Card.

Note: The instructions detailed here do not describe how to install the carrier card and power up the board. Follow instructions detailed in the carrier card documentation (P/N K2TSTCARDIG) for installing the carrier card and powering up the board. In addition, refer "Assembly Instructions" page C-1 for information on assembling PMC-270 Transposer Card.

Caution

Always install PPMC-280 when power is turned off.

Installing PPMC-280

Follow these steps to install PPMC-280 on the carrier card:

1. Switch off power.
2. Remove the carrier card from the system according to the user's documentation.
3. Identify and locate the PMC slot on the carrier card into which you are installing PPMC-280 .
4. Remove corresponding PMC slot filler from the front panel of the carrier card.

5. Mount the PPMC-270 Transposer card on the K2 carrier card as shown in the figure below.

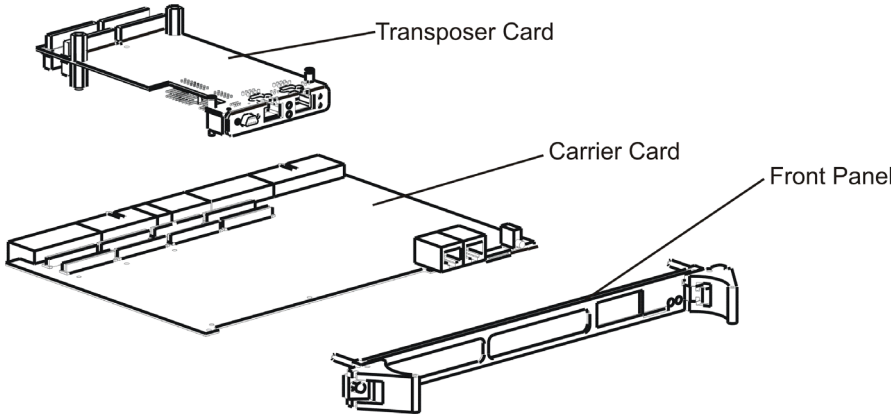


Figure 14: *Installing Transposer Card on Carrier Card*

6. Engage the connectors. Make sure the connectors are seated completely.

7. Mount the PPMC-280 card on the PMC-270 Transposer card as shown in Figure 15 “Installing PPMC-280 Card on Transposer Card” on page 2-18.

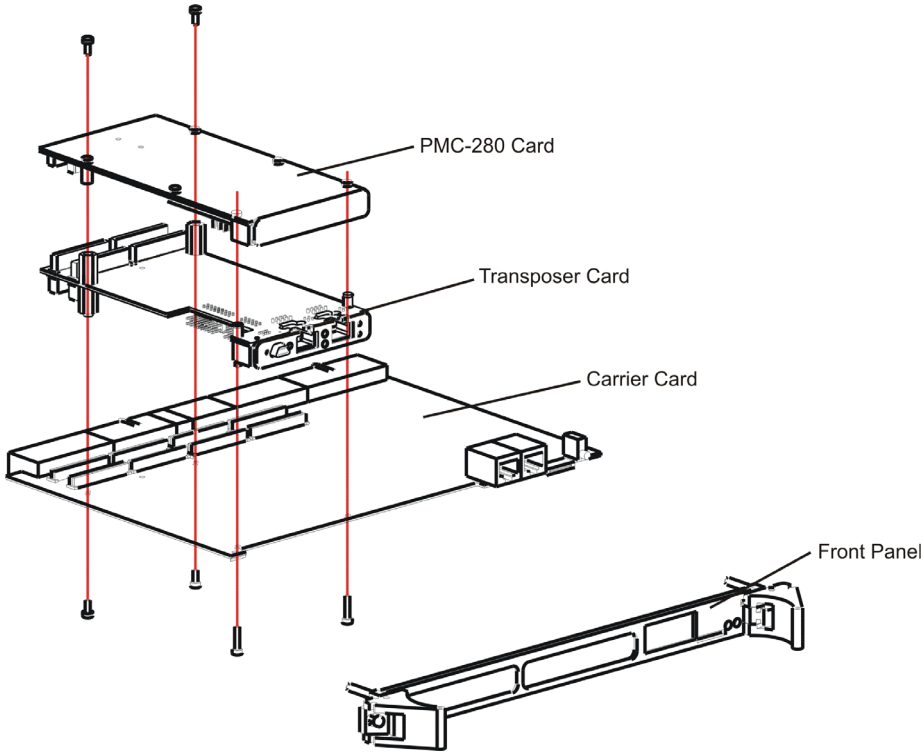


Figure 15: *Installing PPMC-280 Card on Transposer Card*

8. Secure PPMC-280 using four screws provided. Ensure that you screw PPMC-280 from the rear side of the carrier card through clearance holes.

Installation of PPMC-280 along with the PMC-270 Transposer card on the carrier card is now complete. A view of the PMC along with a PMC-270 Transposer installed on a K2 carrier card is shown in Figure 16.

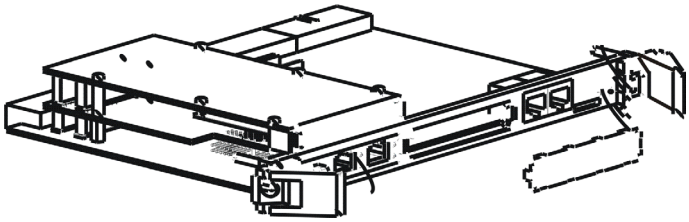


Figure 16: *Installation of PPMC-280 with Transposer Card on Carrier Card*

Removal Procedure

To remove PPMC-280 from the carrier card, follow the steps listed below:

1. Turn off system power (Ensure that you follow the steps to turn off power for the carrier card as per carrier card documentation.)
2. If the carrier card is installed into a backplane, remove the carrier card according to the documented procedure for the carrier card.
3. Remove screws that secure PPMC-280 and PMC-270 Transposer card to the carrier card.
4. Carefully disengage PPMC-280 from the PMC-270 Transposer card. PPMC-280 is now removed from the carrier card.

Board Power Up and Initialization

The steps listed below detail the board power up and initialization procedure:

1. Install PPMC-280 on the carrier card. (Refer to “PPMC-280 Installation on K2 Test Card” on page 2-16).
2. The MONARCH# signal of PPMC-280 has to be asserted by the carrier card when PPMC-280 is used as a Monarch. If PPMC-280 is to be used as a Non-Monarch, the carrier card must float the signal.
3. Connect the Serial Port 0 of PPMC-280 to the PC terminal using a cross wired cable. Ensure that the PC serial port is set for a baud rate of 115200.
4. Switch on system power. The power on LEDs (RefDes: CR8 for 3.3 V and CR9 for 5V) on PPMC-280 should glow to indicate that the board has powered up. If the Power Bad LED (Refdes CR18) is in the OFF state, it indicates that all voltage rails are within tolerance. (Refer to “LEDs” on page 4-3 for a detailed description of the LEDs on PPMC-280).
5. The Operating System/Boot Loader command prompt comes up on the terminal. The board is now fully configured and ready to accept valid commands given at the command prompt.

3

Devices and Other Functions

On-Board Devices

Note: This chapter describes features supported by the standard PPMC-280 variant, 120092. For features supported by other variants, please refer Table 1 "Variants of PPMC-280" page 1-4.

Details of the on-board devices are provided in this section. See Figure 2 and Figure 3 on Page 1-7 and Page 1-8 for the location of the on-board devices.

Table 8: *List of Major Devices*

Description
Two PowerPC MPC7447 RISC Microprocessors Motorola
MV64360 System Controller Marvell Technologies
4 x8Mx16 Intel® Strata Flash®
Two BCM5421 PHY
Three Serial EEPROMs AT24C64

Central Processing Unit

There are two PowerPC™ MPC7447 microprocessors from Motorola as the central processing unit. These operate with a core frequency of 1GHz. The combined heat sink for the CPUs is on the bottom side of PPMC-280.

The CPUs interface to each other and the System Controller through a 2.5V MPX bus (32-bit address, 64-bit data) that runs at 133 MHz.

Additional key features of the CPU are:

- On-die 512 K L2 cache
  - Running at core frequency
  - ECC logic
- Estimated typical power consumption of 8W
  - At 1 GHz and 1.1V core voltage.

CPU 0 and CPU 1

As there are two CPUs, one of the CPUs is designated as CPU 0, and the other CPU is designated as CPU 1. CPU 0 acts as the boot master as it boots up first. CPU 1 is the boot slave. CPU 1 starts booting only after CPU 0 triggers the system controller's inbuilt bus arbiter to allow CPU 1 bus access. Each CPU can identify whether it is CPU0 or CPU1 by reading the `Who Am I` register in the System Controller.

Note: The terms CPU 0 and CPU 1 in this section refer to the boot master and slave respectively and not the physical CPU 0 and CPU 1 shown in Figure 3 "Bottom Layout of PPMC-280 Showing Major Components" page 1-8.

PPMC-280 is designed to swap the CPUs on-board which helps to assign CPU 1 as the boot master. This feature provides flexibility of where to locate CPU on a single-CPU variant of PPMC-280 depending on thermal factors. On variants 120047, 120049, and 120093, the (sole) CPU is located so as to have better airflow in a standard CompactPCI chassis; on variants 120094 and 120791, the (sole) CPU is located to take advantage of the direction of airflow in a custom chassis.

In the dual-CPU environment, CPU0 boots up first, initializes the system controller, memory, and serial port0, before triggering CPU1 to boot. Refer to the software installation guide for details.

Boot Modes

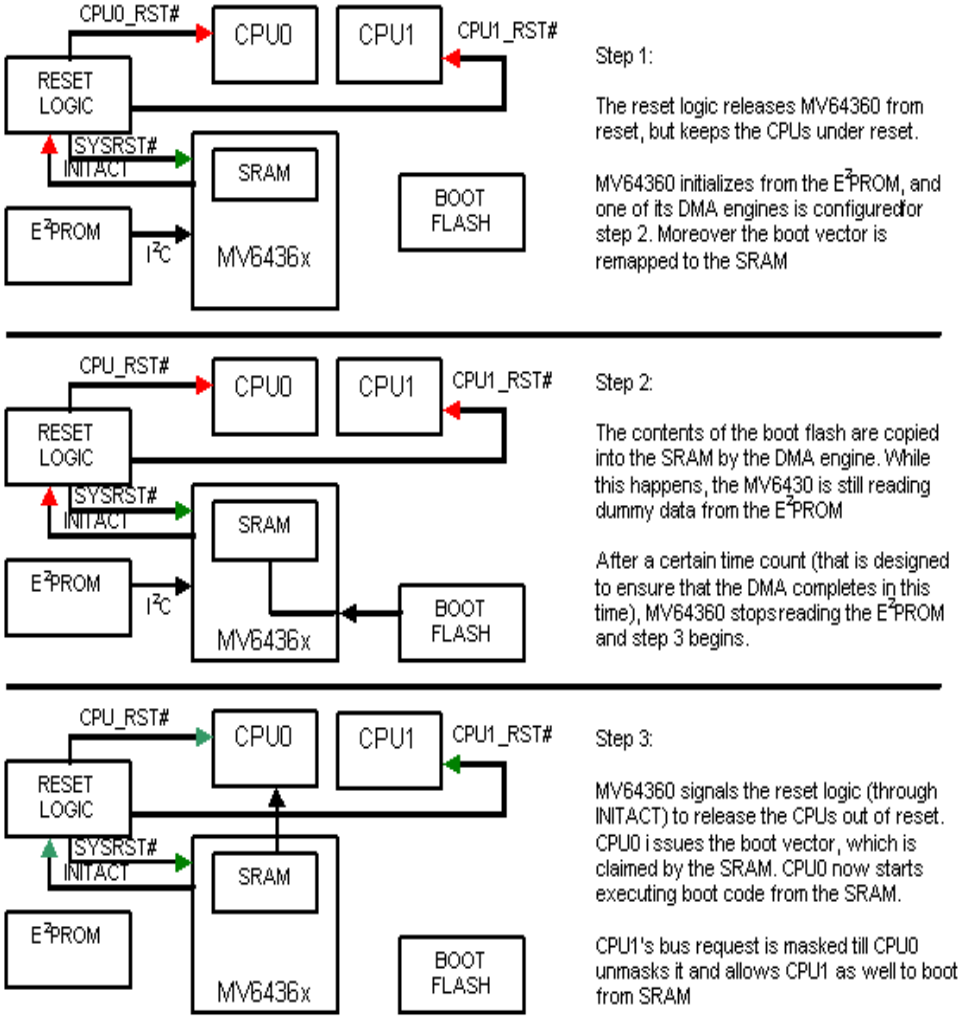
On variants 120092, 120047, 120049, 120791, 120673 and 120093, the boot flash+integrated SRAM combination is the default boot device. This boot mode is referred to as "boot-flash-boot" mode. However, variants 120048 and 120094 are configured to boot from PCI memory space. This boot mode is referred to as "PCI boot" mode. Auto-configuration of MV64360 from the I^2C EEPROM is critical to both boot modes.

BOOT-FLASH-BOOT MODE

The boot flash is an 8-bit wide device that resides on the device bus of MV64360. Though the boot flash stores the boot image, the CPU does not fetch boot code directly from the boot flash. This is because the MPC7447 issues 32-byte burst reads right out of reset, and the MV64360's device controller does not support 32-

byte bursts to an 8-bit device. Hence, the MV64360's integrated SRAM (which is a 32-bit wide device) is used as the actual boot device. The MV64360 is configured (during auto-configuration from I^2C) to remap the PowerPC boot vector to SRAM instead of boot flash.

The following steps describe the boot process in this mode:



PCI_BOOT Mode

In this boot mode, the MV64360 is auto-configured through I^2C such that the PowerPC boot vector is remapped to PCI space (instead of the default mapping to boot flash).

Note: Refer to "PCI Boot" page D-1 for additional information on PCI-Boot.

System Controller

PPMC-280 uses the Marvell Technologies MV64360 System Controller. The features utilized by PPMC-280 are detailed here.

CPU Interface

The following features are utilized:

- MPX bus at 133 MHz
- Internal bus arbiter
- Dual CPU support

DDR SDRAM Controller

The features utilized are:

- 64-bit DDR SDRAM interface
- 8-bit ECC
- Internally generated DDR differential clock output

PCI2.2 Interface

- 64-bit, 66 MHz, universal signaling (3.3V or 5V)
- Support for VPD as defined in PCI 2.2 specification

Device Controller

- 32-bit multiplexed device bus
- Support for Vital Product Data storage device on one chip select (DevCS3#)

Integrated 2Mb SRAM

Note: This feature is not supported by MV64362.

- 64-bit wide + 8-bit even parity
- Support for coherency with CPU caches (if required)

Two Gigabit Ethernet MACs

- IEEE802.3-compliant 10/100/1000Mbps Gigabit Media Independent Interfaces (GMII)
  - port0 and port1 of MV64360 are used
- Dedicated Serial DMA (SDMA) to transfer data/descriptors to/from memory

Note: MV64362 supports only one Ethernet interface.

Two Multi-Protocol Serial Port Controllers

- Used as two independent UART ports
- A dedicated serial DMA (SDMA) to transfer data and descriptors to and from memory

Interrupt Controller

Routes internally generated interrupts and external interrupts (on general-purpose pins) flexibly to two CPU interrupt outputs (separately for CPU0 and CPU1). Interrupts may also be routed to the PCI interrupt output in the Non-Monarch mode

IDMA Controller

Four channels for efficient data transfer between interfaces without significant CPU intervention

Watchdog Timer

- 32-bit down counter generating an NMI to the CPU periodically
- Expiry signal used to reset the system

I^2C Timer

- Both master and slave capability.

- Support for multi-master environment
- Support for auto-configuration on power-on through I^2C

Support for Dual Processing

- On power-on, MV64360 allows CPU0 to boot and keeps CPU1 bus request on hold. After CPU0 boots and initializes the system, it triggers the system controller's inbuilt bus arbiter to allow CPU 1 bus access and start booting.
- Separate interrupt outputs and interrupt mask registers for each CPU.
- Separate Doorbell interrupt register for each CPU, which can be used for CPU-to-CPU interrupt generation, external PCI device-to-CPU interrupt generation, or for a CPU to interrupt itself.
- `Who Am I` register which each CPU can read to determine its identity (CPU0 or CPU1)
- Eight semaphore registers as a locking mechanism for shared resources
- Independent synchronization barrier mechanisms for each CPU to enable synchronization of data transfer between interfaces.

General Purpose Ports

There are 32 general-purpose ports which may also be configured as interrupts.

MV64360 operates on a 1.8V core voltage. The CPU interface operates on 2.5V, DDR interface at 2.5V, and other I/Os at 3.3V.

Note: Refer to the silicon ID of the system controller chip on the board to identify the chip version. The datasheet of the corresponding version is available from Marvell Technologies.

On-board SDRAM

PMC-280 supports on-board DDR266 (133MHz clock, 266MHz data rate) SDRAM with ECC. Memory size and organization are variant-dependent, as shown in Table 9 "Memory organization on PMC-280 variants" page 3-9.

Table 9: *Memory organization on PMC-280 variants*

Variant	Memory size	Logical organization	Physical organization
120092, 120048, 120047, 120093	512MB	Single-bank, mapped to chip-select CS0# of MV64360/62	Nine 512Mb devices (8 for data, 1 for ECC)
120049, 120673	1GB	Dual-bank, one bank mapped to CS0# and the other to CS1#	Nine dual-stacks (eighteen 512Mb devices, nine per bank)
120094	128MB	Single-bank, mapped to CS0#	Nine 128Mb devices (8 for data, 1 for ECC)
120791	256MB	Single-bank, mapped to CS0#	Nine 256Mb devices (8 for data, 1 for ECC)

Note: The usage of stacked memory devices results in a non-conformance from the CMC side-2 component height specification by 0.75mm on variants 120049 and 120673.

Flash Memory

PPMC-280 supports 64 MB (4 devices x 8M x 16) of NOR-based Intel® Strata Flash® on the MV64360's device bus (demultiplexed). This is organized as two banks (Bank0 and Bank1) of 32MB each. Features include:

- Flexible block locking
- Block erase/program lockout during power transitions
- Compliant to Intel's Common Flash Interface (CFI), Scalable CommandSet (SCS) and Command User Interface (CUI) implementations

PPMC-280 also supports 1 MB of Boot Flash (AM29LV008BBE). This is a non-volatile device that stores the boot image (PowerBoot). A portion of the Boot Flash is used as VPD storage device. This is done by redirecting the DevCS3# chip select of MV64360/62 to BootCS#. On variant 120094, Boot Flash is not used as the boot device, but as the VPD device.

Note: Boot Flash is not used as the boot device on variants 120048 and 120094. These variants boot from PCI memory space. Refer to "Boot Modes" on page 3-4 for additional information.

PCI Interface

PCI interface between PPMC-280 and the carrier card is made through PMC connectors P1, P2 and P3. It is a 3.3V/5V, 64-bit (64-bit addressing also supported), 66 MHz PCI2.2 compliant interface implemented in MV64360. The connectors P1 and P2 carry the 32-bit PCI signals, whereas the P3 connector carries the 64-bit extension signals. Refer to Chapter 4 for Connector pin assignments.

PCI Signaling Voltage

PCI signaling voltage to be used can be 3.3V or 5V as decided by the carrier card. The PMC connectors P1 and P3 have V(I/O) pins which are in turn connected to the VREF (PCI reference voltage) pin of the MV64360. The carrier card should supply the V(I/O) pins with 3.3V or 5V to decide the PCI signaling voltage.

PCI Clock

The PCI clock is supplied by the carrier card. The clock frequency can be any value up to 66 MHz.

Note: PCI clock is independent of and asynchronous with respect to the processor bus and SDRAM frequencies.

PCI Vital Product Data

MV64360 provides support for Vital Product Data access through PCI as defined by the PCI2.2 specification. The VPD data structure is stored in the boot flash. Refer to the VxWorks/Tornado BSP Rel. 2.0 for PPMC-280 Programmers Guide (Order Number 221088 410 000) for more information.

Special Function Processor PMC Signals

PPMC-280 implements the Processor PMC signals/pins as defined in the VITA 32-199x standard.

Table 10: *Special Function Processor PMC Signals Implemented*

Signal Name	Function
PRESENT#	Is grounded on PPMC-280 to indicate to the carrier card that the Processor PMC is installed
MONARCH#	Enables Monarch-mode operation of PPMC-280. Is pulled up on PPMC-280. LED CR6 indicates the status of this signal.
EREADY	Open-drain output signal in Non-Monarch mode, and input signal in Monarch mode. Weak pull up (10k) on the Processor PMC. Used to inform the Monarch that all PPMCs are ready for PCI configuration. LED CR7 indicates the status of this signal.
RESETOUT#	Open-drain output under software control. May be used as an input to the carrier card reset logic. Time duration of RESETOUT# assertion is controlled by the software. If RESETOUT# assertion finally results in resetting PPMC-280 itself, the RESETOUT# output of PPMC-280 is tristated as soon as PCI_RST# is asserted by the carrier card.

Monarch and Non Monarch Operation

PCI enumeration in a system consisting of (one or more) Processor PMCs is performed by Monarch (The Processor PMC operating in Monarch mode). When the carrier card grounds the MONARCH# pin on the PMC connector, the software configures PPMC-280 as a Monarch and proceeds to perform PCI bus enumeration (Provided the EREADY signal is asserted). It acts as the PCI interrupt handler and enables PCI interrupt inputs. The PCI interrupt output of the MV64360 is disabled in the Monarch mode.

When the carrier card floats the MONARCH# pin, PPMC-280 operates as a Non-Monarch. In this mode, it deasserts EREADY till it has completed the on-board configuration, and then asserts it to indicate to the Monarch that it is ready for PCI enumeration.

Conventionally, PPMC-280 in the Non-Monarch mode does not handle PCI interrupts, and masks the PCI interrupt inputs from being routed through the interrupt controller, and the PCI interrupt output of the MV64360 is enabled.

Note:

- **CPU0 is responsible for Monarch and Non-Monarch status detection and related action.**
- **PPMC-280 can work on a carrier card that does not support the EREADY signal. In this case, PCI enumeration is begun as soon as Monarch status is detected.**
- **When the carrier card does not support the MONARCH# signal PPMC-280 will enter the Non-Monarch mode by default.**

PCI Interrupts

When PPMC-280 operates in the Monarch mode, it acts as a PCI interrupt handler by default. The PCI interrupts INTA#, INTB#, INTC#, and INTD# are routed from the PMC connector to the internal interrupt controller of the MV64360 through the general-purpose ports (GPPs) of the MV64360 configured as interrupt inputs. The interrupt output of MV64360 is disabled in this mode.

When in the Non-Monarch mode, PPMC-280 has one interrupt output that is wired to the PCI interrupt INTA#. In this mode, PPMC-280 does not handle the PCI interrupts by default. This is however possible through a BSP option.

Note: The PCI arbiter has to be provided by another participant in the system (usually the host card); the internal arbiter of MV64360 is disabled.

Different System Configurations for Monarch and Non-Monarch Mode

The system controller gets configured differently depending on the status of the MONARCH# signal, using separate EEPROMs for the Monarch and Non-Monarch modes. For details see “PCI Boot” page D-1

Ethernet Ports

PPMC-280 supports two 10/100/1000base-T Ethernet ports (GigE-0 and GigE-1) which can be accessed through the PMC I/O (P4) connector. The MAC-layer function is integrated in the MV64360 (two of the three in-built independent MACs are utilized). The physical-layer (PHY) is implemented as two independent

transceivers PHY0 and PHY1 (Broadcom BCM5421) for the two ports. The interface between the MAC and the PHY is GMII. PPMC-280 also uses the Serial Management Interface (SMI) which enables auto-negotiation and passing of status and control parameters between the MAC and the PHY.

The twisted pair network interface signals of the PHYs are isolated through magnetics. The isolated GigE signals are then routed to P4. The Ethernet ports can be exercised in either 10base-T, 100base-T or 1000base-T configuration on standard CAT5 UTP cable. 10base-T can also run on standard CAT3 and CAT4 UTP. Full-duplex operation is supported for 1000baseT, whereas both half- and full-duplex modes are supported for 10/100base-T.

Note: Refer to the BCM5421 datasheet for more information.

Serial Interface

Two RS232 serial ports (RS232-0, RS232-1) are accessible through the PMC I/O connector (P4). The UART controllers for the two ports are integrated in the MV64360. The MV64360 has internal baud rate generators which are configured to clock the UARTs at a baud rate of 115200 bps, deriving from an external Baud Clock input signal (BClkin) of 12.5 MHz. An external RS232 transceiver translates MV64360's UART signals to RS232 levels.
Port 0 (RS232-0) is used by CPU0 and Port 1 (RS232-1) by CPU1.

The serial ports are essentially meant for debug and software development. They utilize a minimum null-modem set of signals (TX and RX). The UART signals are multiplexed on the Multi-purpose pins (MPPs) of the MV64360 A cross-wired null-modem cable is required to interface either port to a PC serial port.

I^2C Bus

The MV64360 supports the two-wire serial I^2C interface, with a multiple-master environment. All devices on the bus support 7-bit addressing. The I^2C bus is wired to the following devices:

Table 11: *I^2C Bus Devices*

Device/Connector	I^2C Slave Address	Function
MV64360	Slave address programmable	• Acts as a bus master to perform CPU-initiated Read/Write access to I^2C bus devices • Supports slave operation with master external to PPMC-280
Serial EEPROM-1 (AT24C64)	1010011 in Monarch mode, 1010010 in Non-Monarch mode	MV64360 Auto-configuration in Non-Monarch mode
Serial EEPROM-2 (AT24C64)	1010010 in Monarch mode, 1010011 in Non-Monarch mode	MV64360 Auto-configuration in Monarch mode
Serial EEPROM-3 (AT24C64)	Default 1010100	BIB (board information block)
RTC	1010000	Accessing Real Time Clock registers
PMC connector P1	I^2C addresses of carrier card devices should not clash with those of any of the above.	• The carrier card can read the BIB from the serial EEPROM-3 • When PPMC-280 operates as a master, it is possible for it to read board identification/configuration information from an I^2C ROM devices, if implemented, on other cards in the system

The I^2C bus operates on the 3.3V rail. However, it is possible to access serial EEPROM-3 from the carrier card even with 3.3V powered off. This is because, when the 3.3V rail is powered off, EEPROM-3 can switch over to 3.3Vaux, an auxiliary 3.3V supply, which is fed to PPMC-280 through the PMC P1 connector, pin 12.

Serial EEPROMs

PPMC-280 has three serial EEPROMs.

Serial EEPROM-1

This 64 Kb (8kx8) device (AT24C64) holds data structures that enable the MV64360 to configure its internal registers automatically on power-up, provided serial ROM initialization of MV64360 is enabled. The MV64360 initializes from this device when PPMC-280 is in the Non-Monarch mode. The device has an I^2C address of 1010010 in the Non-Monarch mode, and an address of 1010011 in the Monarch mode. This EEPROM is write-protected in hardware to prevent corruption of the configuration data-structure.

Serial EEPROM-2

This 64 Kb (8kx8) device (AT24C64) is accessed by the MV64360 (provided serial ROM initialization is enabled) in the Monarch mode. The device has an I^2C address of 1010010 in the Monarch mode, and an address of 1010011 in the Non-Monarch mode. This EEPROM is write-protected in hardware to prevent corruption of the configuration data-structure.

Serial EEPROM-3

This 64 Kb (8kx8) device (AT24C64) holds the Board Information Block (BIB) data. The remaining part of the EEPROM (in excess of the BIB size) may be used as user memory. It is located at a default I^2C address of 1010100. EEPROM-3 operates by default on the 3.3V rail, but switches over to 3.3 Vaux when the 3.3V rail is powered off. This enables the carrier card (if it supplies 3.3Vaux) to access this EEPROM even when the 3.3V rail is powered off.

Real Time Clock

PPMC-280 supports a Y2K-compliant Real Time Clock (MAX6900) on the I^2C bus. The Real Time Clock (RTC) incorporates a real time clock/calendar (providing seconds, minutes, hours, day, date, month and year information) and 31 bytes of scratchpad SRAM. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap years up to the year 2100. The clock can be configured to operate in either the 24 hour format or the 12 hour format with an AM/PM indicator. Time and calendar data are stored in BCD format.

Write-protection can be enabled by means of a write-protect bit.

The RTC operates on a 32.768kHz crystal. It is also backed up by a super-capacitor.

Super-capacitor for RTC

When the board is powered down, the RTC is backed-up by a 0.2F super-capacitor. The super-capacitor is estimated to retain RTC data (sustain time-keeping) for a minimum period of 50 hours. While under typical conditions it could sustain the RTC for more than 50 hours. The guaranteed data retention period under board power-off is 50 hours only.

Note: Keeping the board powered off for more than 50 hours may result in RTC data loss.

Watchdog Timer

The MV64360 has an in-built watchdog timer. It consists of a 32-bit down-counter, pre-loaded by software. Periodically, at a certain count, the watchdog unit generates an interrupt which is routed through the MV64360's interrupt controller to either CPU. This continues so long as the CPU keeps servicing the watchdog and reloading the counter. In the event of the CPU failing to do so, the counter expires and the watchdog unit generates a watchdog expiry signal which is then used by the reset logic to hard reset the system. Refer to the VxWorks 5.5/Tornado 2.2 BSP Rel.2.0 for PPMC-280 Programmer's Guide (Order Number 221088 410 000) for more information.

Programmable Logic

PPMC-280 has an on-board Complex Programmable Logic Device (CPLD) which performs the following functions:

- System reset logic
- PCI boot trigger logic
- Processor PMC signal handling
- Device bus control signal generation
- Miscellaneous logic

4

Controls, Indicators and Connectors

LEDs

The LED indications are provided in Table 12. The location of the LEDs on PPMC-280 is shown in Figure 17 and Figure 18.

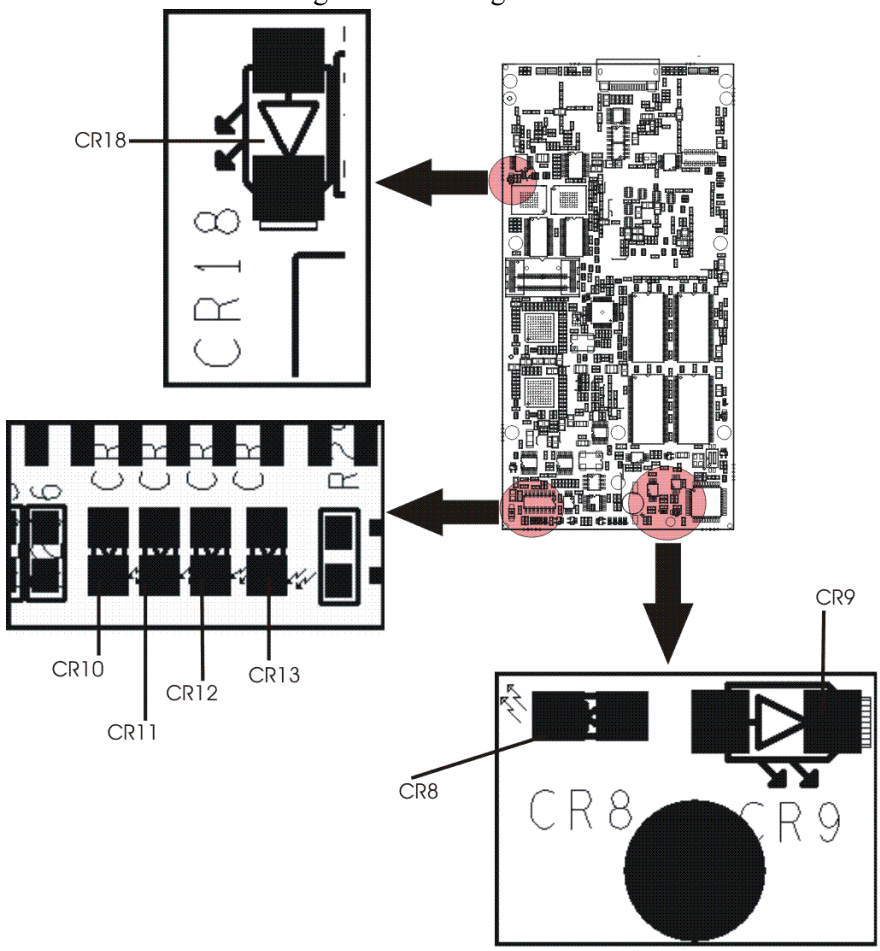


Figure 17: *Zoomed Areas for LED Indicators CR8, CR9, CR10, CR11, CR12, CR13,and CR18*

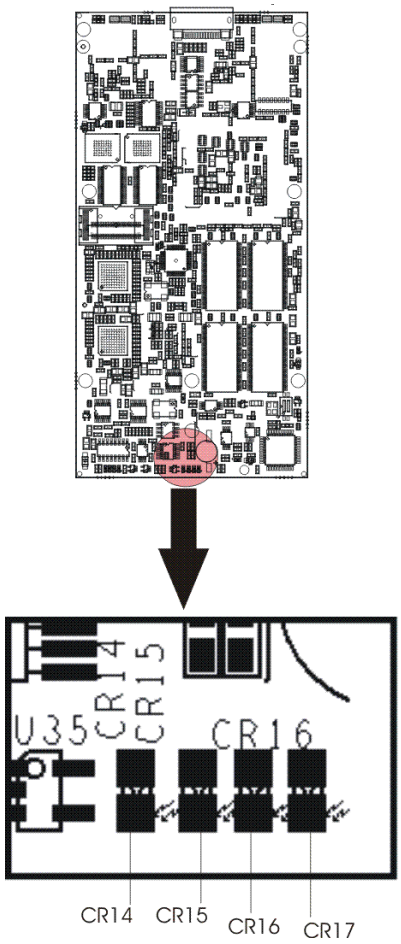


Figure 18: *Zoomed Areas for LED Indicators CR14, CR15, CR16, CR17*

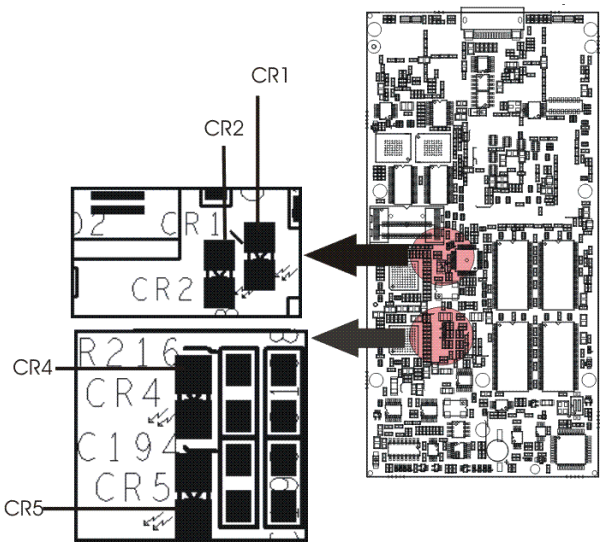


Figure 19: *Zoomed Areas for LED Indicators CR1, CR2, CR4,and CR5*

Table 12: *LED Indications*

LED RefDes	Function	Indication
CR18	Power Bad LED	OFF state indicates that all voltage rails are within tolerance ON state indicates that one or more of 3.3, 2.5, 1.8, and 1.1V rails are out of tolerance. **Note: The Power Bad logic does not monitor the 5V rail.**
CR8	Power ON LED 3.3V Rail	Green: Indicates that the 3.3V rail is powered ON.
CR9	Power On LED 5V Rail	Green: Indicates that the 5V rail is powered ON.
CR13	Ethernet 0 Quality	Twisted pair link quality indicator for GigE-0. The LED goes off when the signal-to-noise ratio is so low that the receiver is unable to recover data.
CR11	Ethernet 0 Receive Activity	Driven for about 80 ms each time there is receive activity on GigE-0.

Table 12: *LED Indications*

LED RefDes	Function	Indication
CR10	Ethernet 0 Transmit Activity	Driven for about 80 ms each time there is transmit activity on GigE-0.
CR12	Ethernet 0 Full Duplex	Glows when GigE-0 is in full-duplex mode.
CR4 and CR5	Link /Speed LEDs for Ethernet 0	Refer "Link/Speed LEDs for Ethernet0" page 4-7
CR17	Ethernet 1 Quality	Twisted pair link quality indicator for GigE-1. The LED goes off when the signal-to-noise ratio is so low that the receiver is unable to recover data.
CR15	Ethernet 1 Receive Activity	Driven for about 80 ms each time there is receive activity on GigE-1.
CR14	Ethernet 1 Transmit Activity	Driven for about 80 ms each time there is transmit activity on GigE-1.
CR16	Ethernet 1 Full Duplex	Glows when GigE-1 is in full-duplex mode.
CR1 and CR2	Link /Speed LEDs for Ethernet 1	Refer "Link/Speed LEDs for Ethernet1" page 4-7
CR3	Software debug LED	Bicolour LED for software debug; wired to MPP23 and MPP26 of MV64360/62. Refer "CR3 Function Table" page 4-6
CR6, CR7	Monarch LED (green) Eready LED(Yellowish-orange)	Refer "CR6 and CR7 Function Table" page 4-7

Table 13: *CR3 Function Table*

MPP23 (GPP23)	MPP26 (GPP26)	LED state
High (default)	High (default)	OFF
High (default)	Low	GREEN
Low	High (default)	YELLOW
Low	Low	OFF

Table 14: *CR6 and CR7 Function Table*

CR6	CR7	MEANING
OFF	ON	PPMC-280 is non-monarch and is yet to release EREADY
OFF	OFF	PPMC-280 is non-monarch, and has released EREADY
ON	ON	PPMC-280 is monarch, and is waiting for EREADY to be released
ON	OFF	PPMC-280 is monarch, and EREADY has been released

Table 15: *Link/Speed LEDs for Ethernet0*

CR4	CR5	Link/Speed
On	On	Up/1Gbps
Off	On	Up/10Mbps
On	Off	Up/100Mbps
Off	Off	No link

Table 16: *Link/Speed LEDs for Ethernet1*

CR1	CR2	Link/Speed
On	On	Up/1Gbps
Off	On	Up/10Mbps
On	Off	Up/100Mbps
Off	Off	No link

On-Board Connectors

PPMC-280 has four on-board PMC connectors.

PMC Connectors

Four 64 pin PMC connectors P1, P2, P3, and P4 are located on the bottom side of the board.

Note: As per the CMC specification (P1386), the PMC connectors are labelled P11, P12, P13, and P14, but are referred to as P1, P2, P3, and P4 in this document.

The location of the four PMC connectors is shown in Figure 3 “Bottom Layout of PPMC-280 Showing Major Components” page 1-8.

The pinouts of the four PMC connectors are shown in the following figures.

Note: # at the end of a signal name indicates that the signal is active low.

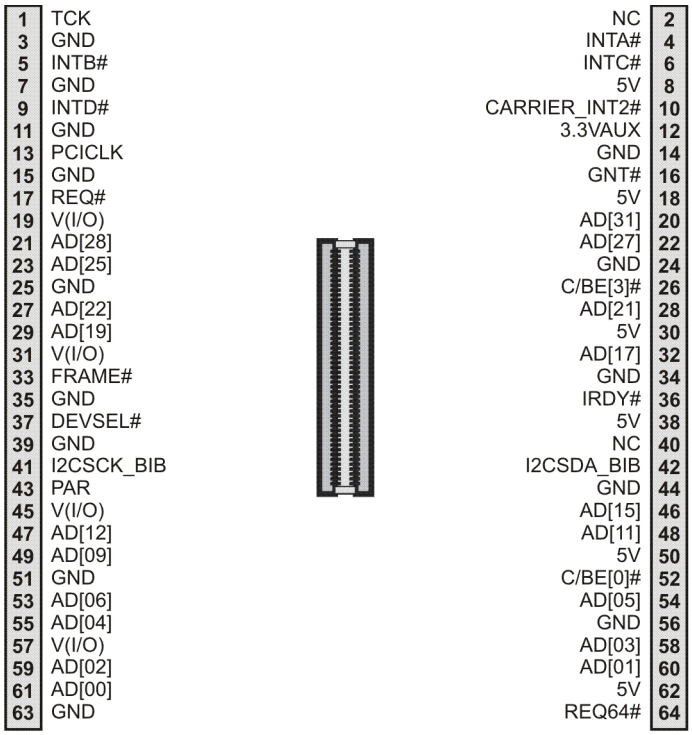


Figure 20: *Pinout of P1 PMC Connector*

Signal Groups in P1

POWER: +5V, V(I/O)PCI2.2: PCICLK, INT[A:D]#, AD[x], C/BE[x]#, FRAME#, DEVSEL#, IRDY#, REQ#, GNT#, PAR, REQ64#, TCK
SPECIAL FUNCTION PPMC: I2C: I2CSCK_BIB, I2CSDA_BIB (these pins are not part of the PMC pinout specification, but as per the PICMG2.15 PCI Telecom Mezzanine/Carrier Card Specification.
CARRIER_INT2# is a 3.3V tolerant carrier card interrupt to PPMC-280. This signal is wired to MPP25 of System Controller.
NC: Not connected

Note: Pins 2 and 40 are unused PMC-defined pins.

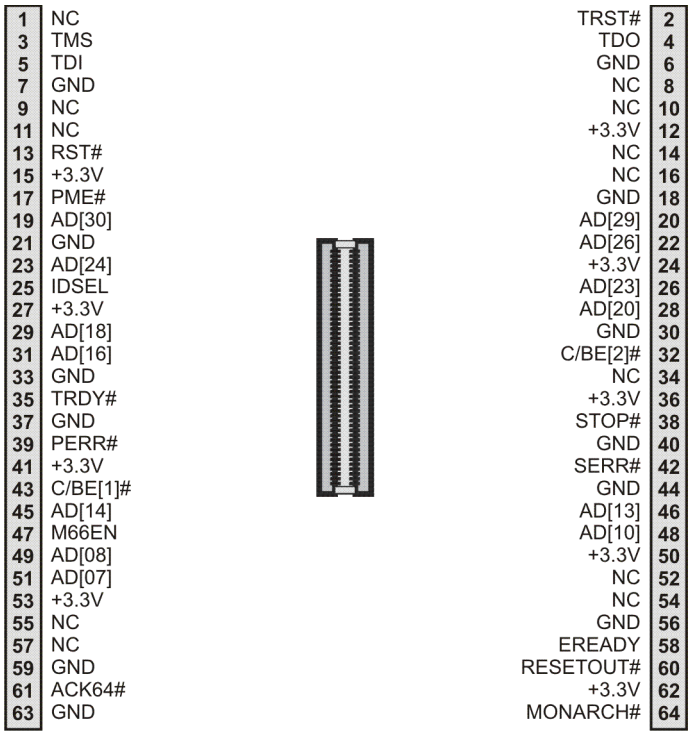


Figure 21: *Pinout of P2 PMC Connector*

Signal Groups in P2

POWER: +3.3V PCI2.2: TMS, TDI, TRST#, TDO, RST#, PME#, AD[x], C/BE[x]#, IDSEL, TRDY#, PERR#, ACK64#, STOP#, SERR#
SPECIAL FUNCTION PPMC: EREADY, MONARCH#, RESETOUT#
NC: not connected

Note: Pins 34, 52, 54 are unused PPMC-defined pins.

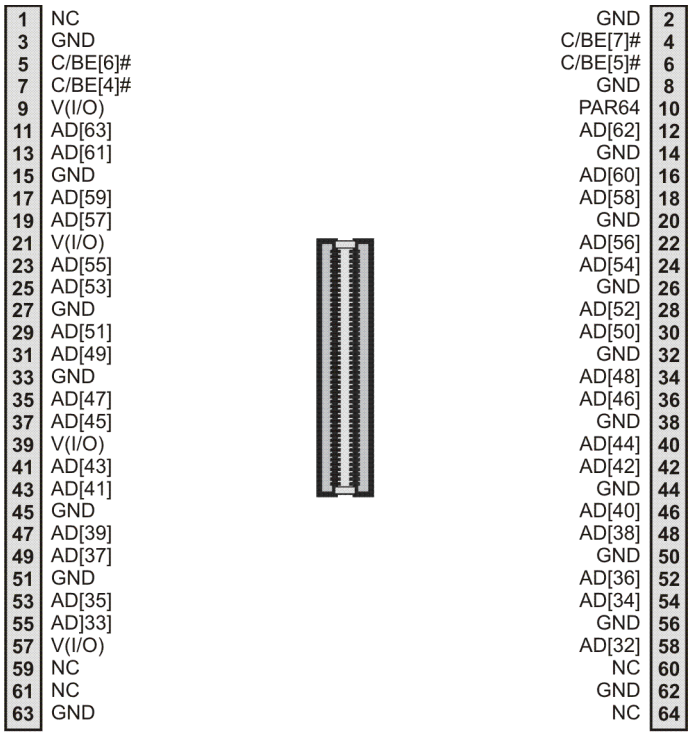


Figure 22: *Pinout of P3 PMC Connector*

Signal Groups in P3

POWER: V(I/O)
PCI2.2: AD[x], C/BE[x]#,
PAR64 NC: Not connected

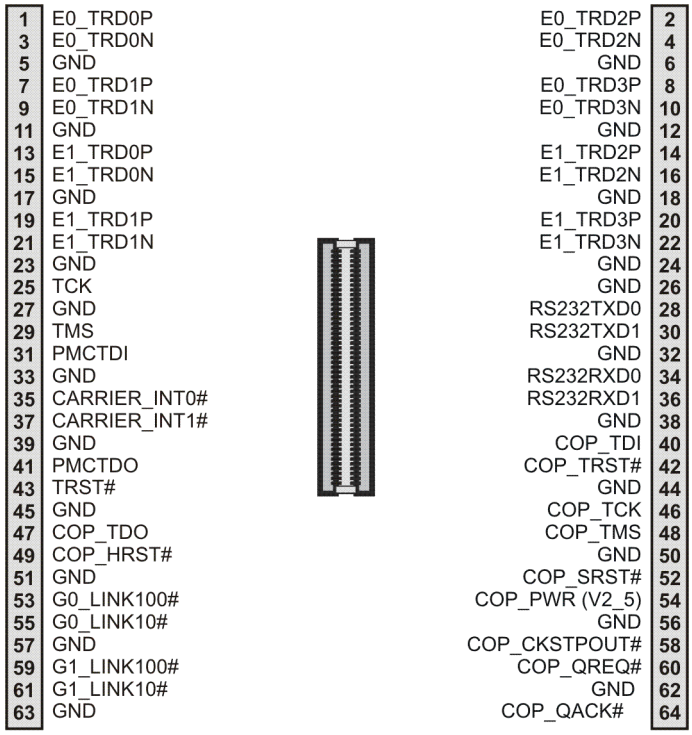


Figure 23: *Pinout of P4 PMC Connector*

Note: P4 pinout is compatible to PICMG ECR 2.15 Draft 0.7 Appendix D

The P4 PMC signal classification is provided in Table 17.

Table 17: *P4 PMC Signal Classification*

Signal Classification	Signals	Signal Description
Ethernet port 0 (GigE-0)	E0_TRD[0:3]P, E0_TRD[0:3]N	Gigabit Ethernet signals
Ethernet port 1 (GigE-1)	E1_TRD[0:3]P, E1_TRD[0:3]N	Gigabit Ethernet signals
SERIAL PORT 0 (RS232 levels)	RS232TXD0: transmit, RS232RXD0: receive	RS232 transmit and receive signals, typically ± 9V
SERIAL PORT 1 (RS232 levels)	RS232TXD1: transmit, RS232RXD1: receive	RS232 transmit and receive signals, typically ± 9V

Table 17: *P4 PMC Signal Classification (cont.)*

Signal Classification	Signals	Signal Description
Carrier card interrupts to PPMC-280	CARRIER_INT0#, CARRIER_INT1# (3.3V tolerant only)	3.3V tolerant interrupt signals to PPMC-280. These signals are wired to MPP6 and MPP7 of the system controller, respectively.
Ethernet Link/Speed LEDs	G0_LINK100#, G0_LINK10#; G1_LINK100#, G1_LINK10#	G0_LINK100# and G0_LINK10# are for Ethernet port 0 G1_LINK100# and G1_LINK10# are for Ethernet port 1 These are active low signals. G0_LINK100#, G0_LINK10#, G1_LINK100#, and G1_LINK10# are driven by BCM5421 PHY to indicate the Ethernet link/speed.
COP Signals	COP_TDO, COP_TDI. COP_TCK, COP_TMS, COP_TRST#, COP_QREQ#, COP_QACK#, COP_TRST#, COP_SRST#, COP_HRST#, COP_CKSTPOUT#, COP_PWR	These signals can be used for accessing the JTAG port of CPU.
JTAG Signals	TCK TMS PMCTDI PMCTDO TRST#	These signals can be used for accessing the JTAG ports of on-board devices

Note: JTAG and COP signals are exclusively for Force Internal Usage

The Ethernet link/speed and the corresponding signal status is tabulated below.

Table 18:*Ethernet Link/Speed and Signal Status*

Link/Speed	G0_LINK100#/G1_LINK100#	G0_LINK10#/G1_LINK10#
Up/1000 Mbps	LOW	LOW
Up/100 Mbps	LOW	HIGH
Up/10 Mbps	HIGH	LOW
No Link	HIGH	HIGH

Note: To use the signals (in the table above) to glow LEDs on the carrier card, ensure that suitable current limiting series resistors are used with the LEDs.

A

Hardware Resources Mapping

Resource Mappings

This section details the following:

- PPMC-280 memory map.
- I^2C Bus Addresses
- PCI Resources
- Device Bus Chip Select Mapping
- DDR SDRAM Chip Select Mapping
- External Interrupt Mapping to GPPs of MV64360
- Processor PMC Signal Access

PPMC-280 MEMORY MAP

Table 1: *MEMORY MAP*

Address Range (Hex)	Description	Size
FF800000 – FFFFFFFF	Boot Flash (BootCS#)	8MB
F2040000 – FF7FFFF	Unused	
F2000000 – F203FFFF	Integrated SRAM	256KB
F1010000 – F1FFFFFF	Unused	
F1000000 – F100FFFF	MV64360/64362 Internal Registers	64KB
A8000000 – F0FFFFFF	Unused	
A4000000 – A7FFFFFF	Reserved for User Flash expansion	Up to 128MB
A2000000 – A3FFFFFF	User Flash 1 (DevCS [1]#)	32MB
A0000000 – A1FFFFFF	User Flash 0 (DevCS [0]#)	32MB
90000000 – 9FFFFFFF	Unused	
89000000 – 8FFFFFFF	Unused	
88000000 – 88FFFFFF	PCI_0 I/O	16MB
86000000 – 87FFFFFF	PCI_0 Memory 3	32MB
84000000 – 85FFFFFF	PCI_0 Memory 2	32MB

Table 1: *MEMORY MAP*

82000000 – 83FFFFFF	PCI_0 Memory 1	32MB
80000000 – 81FFFFFF	PCI_0 Memory 0	32MB
20000000 – 7FFFFFFF	Reserved for SDRAM expansion	Up to 2GB
00000000 – 1FFFFFFF	On-board SDRAM (CS [0]#)	512MB

I²C Bus Addresses

The following table provides the I²C bus addresses for the default condition.

Device	7-bit I²C Address	Remarks
MV64360 slave	Programmable	Through slave address register of MV64360
Serial E²PROM-1	Monarch: 1010011 Non-Monarch: 1010010	The E²PROM is write protected in hardware.
Serial E²PROM-2	Monarch: 1010010 Non-Monarch: 1010011	The E²PROM is write protected in hardware.
Serial E2PROM-3	1010100	
RTC	1010000	Fixed address

PCI Resources

The only PCI device on PPMC-280 is the MV64360. The IDSEL input is routed straight to the PMC connector; so the IDSEL mapping of MV64360 (applicable when PPMC-280 is a Non-Monarch) is the responsibility of the carrier card/system designer. The arbitration signals (REQ#, GNT#) of MV64360 are also routed straight to the PMC connector to be used by the arbiter (which must exist somewhere else in the system).

The PCI interrupt output of MV64360 is wired to INTA#.

In the Monarch mode, PCI interrupts are handled by PPMC-280. They are mapped to General Purpose Ports (GPPs) of the MV64360.

Device Bus Chip Select Mapping

Shows what chip-selects (address windows) of MV64360 are allotted to the devices on the MV64360s device bus (mastered by the MV64360 alone).

Table 2: *Device Bus Chip Select Mapping*

Device	MV64360 Chip Select	Note
USER FLASH BANK0 (8Mx32)	DevCS0#,	
USER FLASH BANK1 (8Mx32)	DevCS1#	
BOOT_FLASH	BootCS#	DevCS3# is also directed to Boot Flash for VPD access.

External interrupt mapping to GPPs of MV64360/62

The interrupt controller of the MV64360/62 takes eleven hardware interrupt inputs through its General Purpose Ports (GPPs). The port mapping is shown on Table “External interrupts on GPPs of MV64360/62” .

Table 3: *External interrupts on GPPs of MV64360/62*

#	NAME	DESCRIPTION	GPP NO.
1	CARRIER_INT0#	Interrupt input from carrier card	6
2	CARRIER_INT1#	Interrupt input from carrier card	7
3	CARRIER_INT2#	Interrupt input from carrier card	25
4	PHY_INT#	Interrupt from either Ethernet PHY-0 or PHY-1	12
5	PCI_INTA#	PCI interrupts to be handled when PMC-280 is a monarch.	27
6	PCI_INTB#		29
7	PCI_INTC#		16
8	PCI_INTD#		17

PROCESSOR PMC SIGNAL ACCESS

Software can access the special Processor PMC signals through MV64360/62’s GPPs as shown on Table “PPMC special signal mapping to GPPs”

Table 4: *PPMC special signal mapping to GPPs*

#	SIGNAL	GPP NO.	REMARKS
1	MONARCH#	4	Input signal only
2	EREADY	31	When used as input (monarch mode)
		8	When used as output (non-monarch)
3	MV_RESETOUT#	2	Assert low to cause RESETOUT# assertion

Table 5: *Miscellaneous signals mapped to GPPs of MV64360/62*

Group	Signal	GPP #	Remarks
Serial port 0	UTXD0	0	Serial port 0 transmit
	URXD0	1	Serial port 0 receive
Serial port 1	UTXD1	3	Serial port 1 transmit
	URXD1	5	Serial port 1 receive
Serial baud	MV_BAUDCLK	20	Baud clock input (50MHz)
CPU signals	MPP_CPU0_MCP#	21	Machine check interrupt input to CPU0 for debug only.
	MPP_CPU1_MCP#	22	Machine check interrupt input to CPU1 for debug only.
	TBEN	10	CPU Time-base enable signal for debug only.
Watchdog	WDOG_EXPIRY#	19	Watchdog counter expiry signal
Initialisation/ configuration	INITACT	28	MV64360/62 I^2C configuration active
	MPP_PCIBOOT	9	shown on Table “PCI Boot”
Debug	DEBUGLED _GREEN	23	Software debug LED, shown on Table “LED Indications”
	DEBUGLED _YELLOW	26	Software debug LED, shown on Table “LED Indications”
PCI	PME#	30	PCI Power management enable

Note: The GPPs indicated in Tables 3-5 above should be used only for intended functions. Usage otherwise may result in unpredictable operation.

ETHERNET PHY ADDRESSES

The two Ethernet PHYs on PPMC-280 have the following PHY addresses:

PHY0 (i.e. Ethernet port 0): 00001b
PHY1 (i.e. Ethernet port 1): 00011b

B

Troubleshooting

Troubleshooting

This appendix provides a hint list for detecting erroneous system configurations and any untoward or unusual behavior of PPMC-280. It cannot replace a serious and sophisticated pre- and post- sales support during application development.
If it is not possible to fix a problem with the help of this chapter, contact your local sales representative or FAE for further support.
.

Problem	Possible Reason	Solution
Unable to insert board into carrier card	Damaged plugs, bent or broken pins	1. Ensure that the voltage key(s) on the carrier card are properly inserted into the corresponding key-holes on PPMC-280. 2. Check PMC connector on carrier card for bent or broken pins 3. Replace carrier card.
	Board defect	Replace board
	Screws of PPMC-280 not removed	1. Ensure that screws for the stand-offs and bezel on PPMC-280 are removed. 2. Insert the board 3. Use the screws to fasten the board from the bottom of the carrier card.
Powering-on the board fails	Power Supply voltages for device not within the specified range	1. Check that voltages are within their specific ranges 2. Check that power supply is capable to drive the respective loads.
	Blown fuse	Check and replace fuse **Note: There is no fuse on PPMC-280, but might be present on the carrier card.**

Problem	Possible Reason	Solution
	Damaged plugs, bent or broken pins	1. Check PMC connector on carrier card for bent or broken pins 2. Replace carrier card.
	The PMC-270 Transposer card is not completely inserted in the test card or PPMC-280 is not completely in the Transposer card	Ensure that both Transposer card and PPMC-280 are assembled and secured by screws as described in the installation chapter.
Power-bad LED glows	One of the power rails is out of tolerance	Check the 3.3V rail voltage
Board does not boot	Card is not properly installed on PMC slot	1. Check that the card is seated properly with no gap between the PMC plugs and the base of the receptacles. 2. Ensure that the voltage key(s) on the carrier card are properly inserted into the corresponding key-holes on PPMC-280. 3. Ensure that both the Power-ON LEDs CR8 and CR9 are lit and Power bad LED CR18 is not lit.
	Power Supply not proper (The 3.3V and 5Vsupply from the carrier card might be inadequate in terms of current capability or tolerance)	Verify that the power supply meets power supply requirements as given under “Power Requirements” page 2-8.
	Reset improper (The PCI reset sourced by the carrier card results in system reset on PPMC-280. This may have an inadequate pulse-width or might occur repeatedly)	Ensure that the PCI reset stays asserted for a minimum of 200 ms after power becomes stable

Problem	Possible Reason	Solution
	System Controller not able to successfully initialize from EEPROM.	Check if CR3 glows green immediately on power-up, and then yellow. This indicates that the system controller has initialized and copied the boot-image from boot-flash into SRAM (applicable only for boot-flash boot variants).
	Serial port is not OK	1. Check if LED CR3 glows green momentarily immediately after power-on, and then turns yellow, and finally turns off. This sequence indicates that the board is booting successfully but there is probably something wrong with the serial port. (Applicable to variants 120092, 120047, 120049, and 120093) 2. Check whether the correct serial port (Port 0) is used 3. Verify if the terminal is configured to the right baud rate 4. Ensure a null-modem cable is used

Problem	Possible Reason	Solution
	Processor PMC-related issues	1. Verify if PPMC-280 is assigned the Monarch status 2. Verify there are not more than one Monarchs in the system 3. Verify if there is another Non-Monarch PPMC in the system which does not flag EREADY 4. Check IDSEL and IRQ mappings on the carrier card 5. If PPMC-280 is in the Non-Monarch mode, verify if the Monarch waits till PPMC-280 flags EREADY 6. Ensure that the PCI clock, reset and VI/O from the carrier card are OK
	Hangs in I^2C initialization	Verify if there is an address conflict on the carrier card
Board runs unstable	Disregard of environmental requirements	Check that temperature inside system stays within specified ranges for all system devices
	Keeps rebooting unexpectedly	Check the PCI reset from the carrier card
	Drivers are missing, faulty or do not match hardware	1. Check that all used hardware parts have a driver matching the hardware 2. Reinstall hardware drivers
	Board defect	Replace board

Problem	Possible Reason	Solution
PCI In-operational	PPMC-280 requirements or PCI specifications are not met by the carrier card	1. Verify the PCI interface voltage (V I/O), PCI clock, PCI reset and PCI arbiter on the carrier card meet the PCI2.2 specifications 2. Ensure that all pull-ups necessitated by the PCI2.2 specifications are provided on the carrier card 3. If PPMC-280 is installed on a 32 bit PMC slot, ensure that the REQ64# signal to this slot is separately pulled high 4. Ensure that the PCI reset stays asserted for a minimum of 200 ms after power becomes stable
	Board defective	1. Ensure that the PCI interface in the system works without PPMC-280 2. If the PCI interface in the system works without PPMC-280, then replace the board.
PPMC-280 does not operate in the Monarch mode	PPMC-280 does not recognize the Monarch status	Verify that the Monarch signal of PPMC-280 is pulled low by the carrier card
	Another Non-Monarch board in the system is not releasing the EREADY signal	1. Ensure that the EREADY signal is released by other Non-Monarch boards in the system 2. If required, re-boot and verify if PPMC-280 operates in the Monarch mode 3. If not critical, you may also disconnect the EREADY signal of the offending board from the other boards

Problem	Possible Reason	Solution
	Two or three Monarchs in the system	Ensure that the carrier card does not assign Monarch status to more than one board
PPMC-280 does not operate in Non-Monarch mode	The Non-Monarch status is not recognized	Ensure that the carrier card has tristated/left unconnected the Monarch signal of PPMC-280
Ethernet is in-operational (Network download of Linux fails)	Network link is not OK	1. Verify if the link activity LED is glowing on PPMC-280. 2. Verify that the Ethernet cable and the external link is fine
	Board failure	Replace board
	Ethernet port configuration (MAC address, IP address) is not proper.	Check that MAC address can be read and is correct. Also ensure that the IP address that is assigned to the port is appropriate. Refer to the Software documentation for details.
Ethernet unstable or system crash	Improper IP address assignment to the ethernet ports (when using more than one port)	Ensure that the IP address assignment is such that the Ethernet ports are on different subnets
RTC in-operational	Super-capacitor drained if the board has not been powered on for a long time (more than 50 hours)	Power-on the board and reconfigure the RTC. Wait for at least ten minutes for the super-capacitor to charge up
Board hangs or becomes unstable	No adequate airflow	Check if the airflow is adequate-see “Thermal Requirements” page 2-10.

C

Assembly Instructions

Assembly Instructions for Transposer Card

The following figures and instructions demonstrate the procedure to be followed to assembling the PPMC-270 Transposer Card with K2 test card.

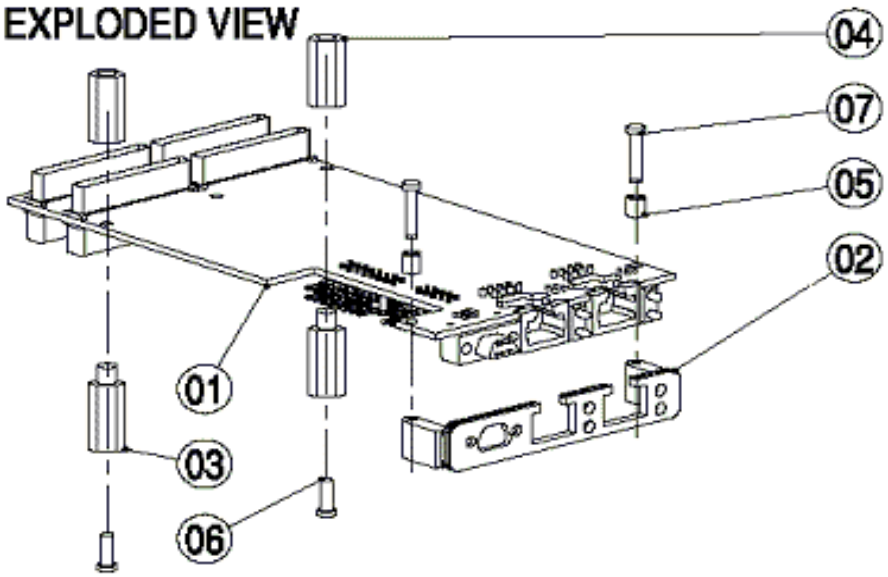


Figure 1: *Top Assembly of PMC 270 transposer card, exploded view.*

ITEM NO.	QTY	PART	DESCRIPTION
01	1	SR270 / K2-TRANSPMC0	Base assy, transposer card,PMC270 / K2
02	2	FPNLPMCBZL-PMC270T	FPNL Bezel PMC270/ K2 transposer card
03	2	QSTNDF10x4.5MM	Standoff female / male M2.5x10 mm
04	2	QSTDF-F/F-2.5x15	Standoff female / female M2.5x15 mm
05	2	QSPACER-M2.5x5	Spacer M2.5x5 mm
06	2	QSCR-M2.5x5	Screw M2.5x5 mm
07	2	QSR-M2.5x20CHEESE	Screw M2.5x20 mm

FINAL **ASSEMBLY** OF PMC 280 ON PMC 270 TRANSPOSER CARD

Assembly process - 1

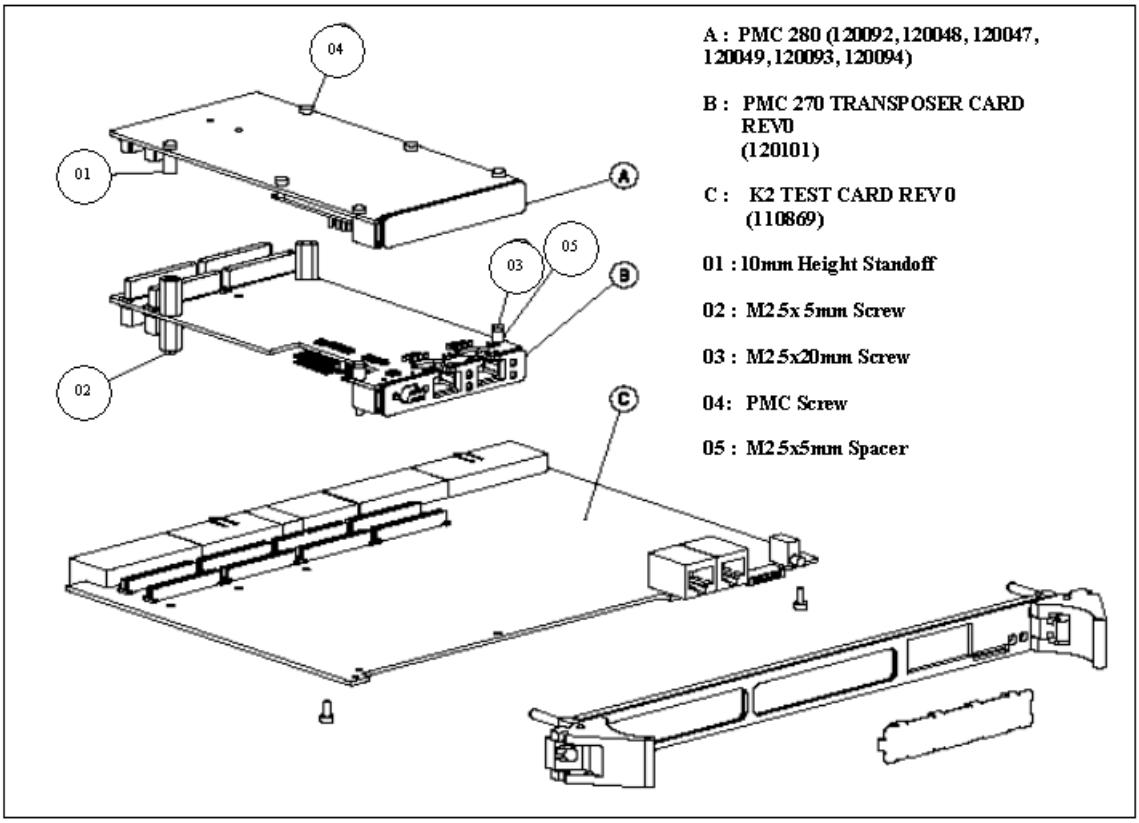


FIGURE 8.0.5.1 : Final Assembly **OF PMC 280 ON PMC 270 TRANSPOSER CARD,** Assembly process - 1

DESCRIPTION: (FIGURE 8.0.5.1)

1. Remove 01 from board A.
2. Remove 02 and 03 from board B.

Assembly process - 2

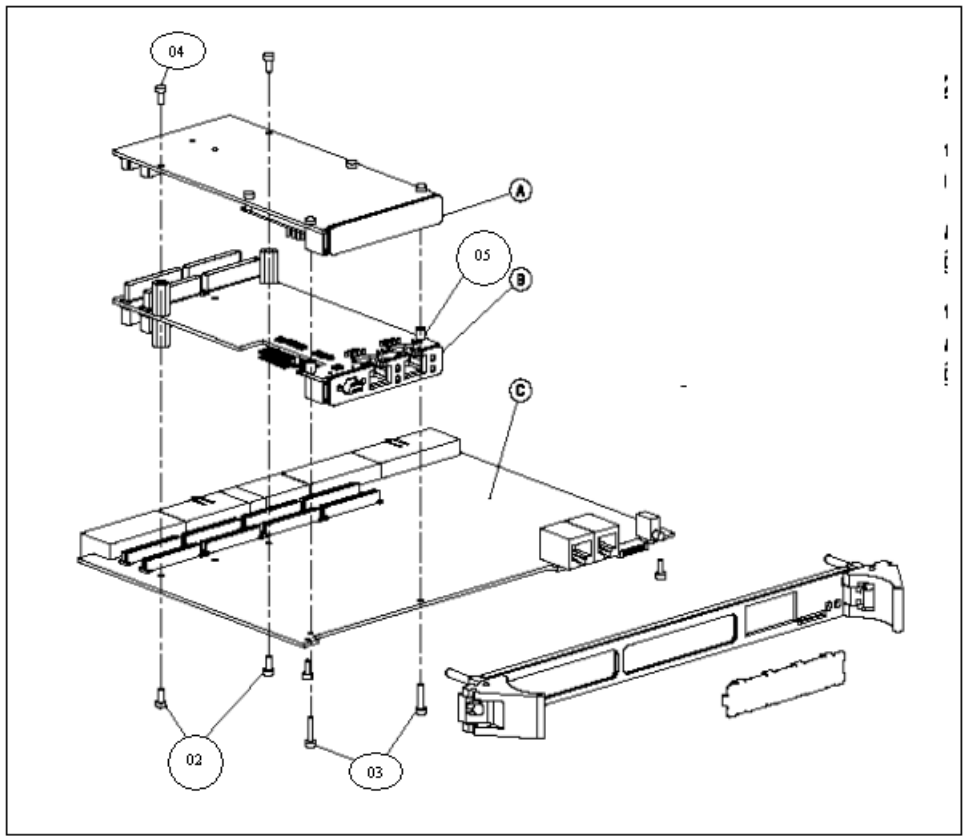


FIGURE 8.0.5.2 : Final Assembly **OF PMC 280 ON PMC 270 TRANSPOSER CARD** Assembly process - 2

DESCRIPTION: (FIGURE 8.0.5.2 **)**

1. Assemble A and B by using srew 04.
2. Assemble B and C by using srew 02.
3. Assemble A , B and C by using srew 03.

Assembly process - 3

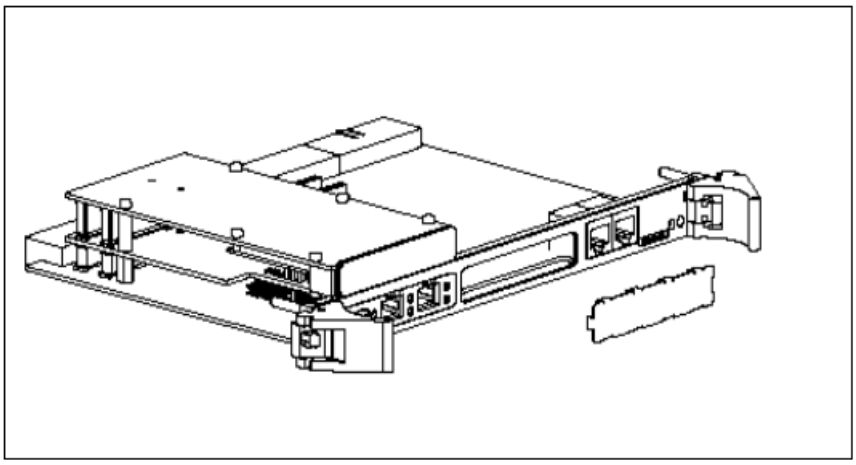


FIGURE 8.0.5.3: Final Assembly **OF PMC 280 ON PMC 270 TRANSPOSER CARD ,**Assembly process – 3

DESCRIPTION: (FIGURE 8.0.5.3 **)**

Final Assembly of board A , B AND C

D

PCI Boot

PCI Boot

Additional information on PCI-Boot is given in the following sections.
Variants B and F boot from PCI space - typically the memory of the monarch or a peer PCI subsystem, referred to as the "boot host". In PCI boot mode, the PPMC-280 would typically be in non-monarch mode; the system monarch would want to keep the PPMC-280 CPUs held under reset till it desires to trigger them to boot; ideally, the monarch would do this after it has enumerated PCI and set up the target memory location for PPMC-280 to boot from. PPMC-280 also supports PCI boot in the monarch mode, in which case the "boot host" would be a non-monarch.

The following features/steps are integral to accomplishing PCI boot on PPMC-280:

- E^2PROM-1 and E^2PROM-2 are factory-programmed with the data-structures for PCI boot.
- On system reset, MV64360/62 initiates an I^2C read sequence from a target I^2C device at address 1010010. In the non-monarch mode, this address belongs to E^2PROM-1 whereas in the monarch mode, this address belongs to E^2PROM-2. While I^2C configuration happens, the CPU(s) is/are still held under reset.
- The MV64360/62's CPU address decoders are configured in such a way that the PowerPC® reset vector is mapped to the PCI space. The data structures also include minimal register settings for the CPU and PCI interfaces of the MV64360/62. The table below broadly describes the actions performed by I^2C configuration prior to boot. When I^2C configuration ends, MV64360 releases the INITACT signal to indicate to the reset logic that the CPUs can now be released from reset.
- The reset logic still keeps the CPUs on PPMC-280 under reset as long as the MPP_PCIBOOT signal is high. This signal is mapped to a GPP of the MV64360/62.
- PPMC-280 is triggered to wake its CPUs out of reset (asserting the MPP_PCIBOOT signal low) by the "boot host". Before this trigger, however, the "boot host" might need to carry out a few other operations (see example further below in this chapter).
- The MV64360/62 now receives the reset vector and redirects it to PCI space.

Table 6: *Important I^2C Configuration steps for PCI boot:*

Step	Non-monarch mode (E^2PROM-1)	Monarch mode (E^2PROM-2)
Configures relevant GPPs of MV64360/62 for INITACT and MPP_PCIBOOT.	Yes	Yes
Configures relevant GPP of MV64360/62 for EREADYOUT	Yes	No
Disables the BOOTCS# chip-select	Yes	Yes
Maps PowerPC™ reset vector to PCI (sets the "PCI Memory 0 Base address" of MV64360/62 to 0xFF800000) and opens a PCI memory window of 8MB (sets the "PCI Memory 0 Size Register" to 0x0000007F)	Yes. This causes the PowerPC reset vector 0xFFF00100 to hit the PCI memory window. The boot vector that appears on the PCI bus depends on what value the monarch sets the MV64360/62's PCI Memory 0 Remap address register to	Yes. See next step.
Sets"PCI Memory 0 Remap Address register" of MV64360/62 to 0x00000880	No	Yes. Thus the boot vector that appears on the PCI bus is 0x08F00100
Sets the Internal Register base address in MV64360/62's PCI configuration space to 0x80000000	No	Yes
Configures the PCI Command and Status register of MV64360/62 for master enable, memory and I/O decode	No (this step is expected to be performed by the monarch)	Yes
Asserts EREADYOUT low	Yes	No

Note: Note: The default values programmed into the "PCI Memory 0 Size", "PCI Memory 0 Remap Address" and "PCI Internal Registers Base Address (configuration space)" registers of MV64360/62 through I^2C configuration may need to be altered to suit system requirements. For instance, the boot vector 0x08F00100 that the PPMC-280 presents in the monarch mode may be in conflict with some other address in PCI space.

Example - Steps

These are the steps that might need to be performed by the "boot host" to correctly configure the PPMC-280 for PCI boot:

PPMC-280 in non-monarch mode (the "boot host" is assumed the monarch)

a) The monarch sets up the target image at a certain location in its memory

b) Upon release of EREADY, the monarch enumerates the PCI bus. As part of this, it configures the PCI Command and Status register of MV64360/62 so that, at a minimum, the MV64360/62 has the ability to act as a PCI master, and to respond to PCI memory accesses.

c) The monarch also configures "PCI Memory 0 Remap Address Register" of the MV64360/62 to an appropriate value so that the boot vector that PPMC-280 will later put out on the PCI bus will hit the starting location of the boot image in the memory of the monarch.

d) The monarch then triggers the PPMC-280 to boot by writing a "0" to MV64360/62's internal 32-bit GPP Value Register (offset 0xF104). This causes a high-to-low transition on the MPP_PCIBOOT signal, which triggers the CPLD on PPMC-280 to bring the CPUs out of reset.

PPMC-280 in monarch mode

a) The "boot host" sets up target image at a certain location in its memory. Its PCI-to-memory address translation windows are configured in a manner that will allow the boot vector from the PPMC-280 to hit the starting location of the boot image.

b) The "boot host" triggers the PPMC-280 to boot as in step (c) above.

Note: Since the PCI boot mechanism on the PPMC-280 is heavily dependent on the reset configuration of the MV64360/62 and the correct configuration of PCI addresses, the system designer must keep in mind the implications of un-foreseen resets or PCI address reconfiguration.

An example situation is described below:

– The PPMC-280 is in the monarch mode and boots from a PCI memory address 0x08F00100 i.e. it copies the compressed boot image from this location to its local memory, where it uncompresses it and loads the operating system.

- The operating system comes up and enumerates PCI. While doing so, it changes the PCI Base Address Registers (BARs) of the "boot host" card.
- A local reset occurs on the PPMC-280 because of a watchdog expiry or a manual reset. The PPMC-280 now presents the boot vector 0x08F00100 on the PCI bus, but this address is not claimed by the "boot host" because its BARs have been reprogrammed. Hence, the PPMC-280 fails to reboot.

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Product Error Report

Product:	Serial No.:
Date Of Purchase:	Originator:
Company:	Point Of Contact:
Tel.:	Ext.:
Address:	
Present Date:	
Affected Product: ❑ Hardware ❑ Software ❑ Systems	Affected Documentation: ❑ Hardware ❑ Software ❑ Systems
Error Description:	

This Area to Be Completed by Force Computers:

Date:

PR#:

Responsible Dept.: ❑ Marketing ❑ Production

Engineering ➠ ❑ Board ❑ Systems

+ Send this report to the nearest Force Computers headquarter listed on the address page.