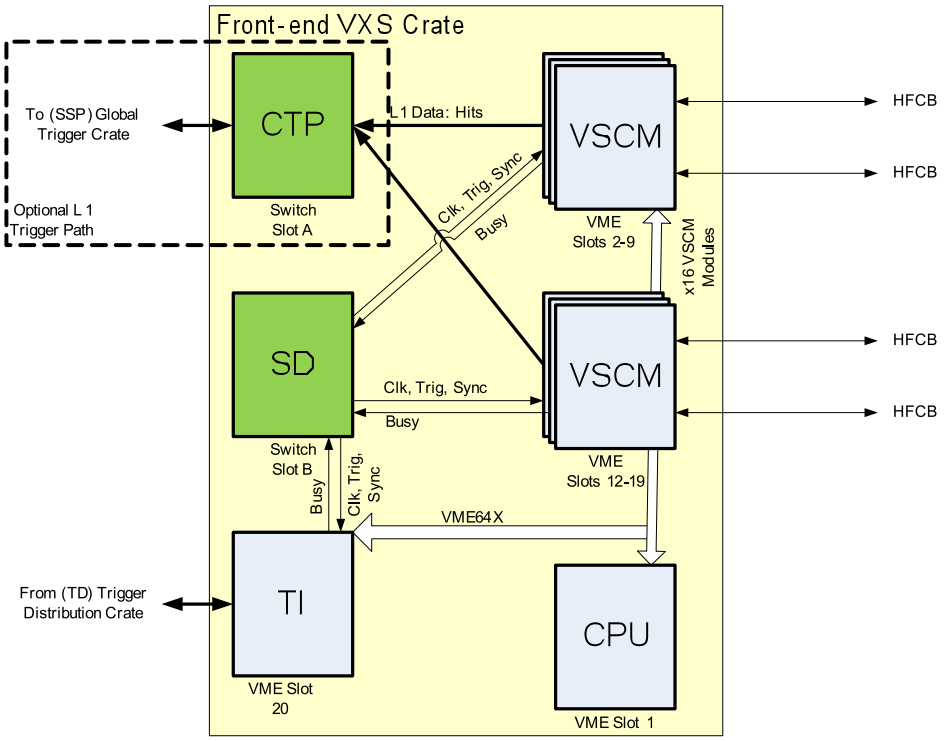
CLAS SVT: VXS-Silicon-Control-Module (VSCM)

1 Introduction

The VSCM is a VME/VXS module that communicates with multiple FSSR2 chips on the Jefferson Lab Hybrid Flex Circuit Board (HFCB). The VSCM is responsible for configuring the FSSR2 registers, providing analog calibration pulses to the FSSR2 chips, delivering/monitoring proper control signals (clock, reset, status), and capturing serialized event data from the FSSR2. Each VSCM can interface to 2 HFCB modules and each HFCB has 4 FSSR2 chips. Up to 16 VSCM modules can reside in a VXS crate. When multiple VSCM modules are used additional cards are required to ensure event & timing synchronization. These additional modules are shown in Figure 1a and are the Trigger Interface (TI) and Signal Distribution (SD), which are part of existing Jefferson Lab 12GeV DAQ electronics. The VSCM does support a stand-alone mode useful when only 1 or 2 HFCB interfaces are used.

Figure 1a: VSCM in the 20 Slot VXS Crate



2. Purpose of the module

The main purpose of the VSCM is to convert the FSSR2 data-driven information stream into sparsified & triggered events that are correlated with external detectors. Idle status words are suppressed to minimize event size, but these status words are monitored to for diagnostic purposes of the individual FSSR2 chips. The event builder of the VSCM uses the BCO clock timestamp from each FSSR2 data word and matches it to the global system clock timestamp. Since the BCO clock is derived from the global system clock, triggers received by the VSCM will cause the event builder to extract hits with specific BCO timestamps that correspond to a

programmable time window where the physics event could have occurred on the HFCB. When a trigger is received the appropriate FSSR2 data words are copied into a new event buffer and pushed into an event FIFO. These events can be readout in order with other modules in the system and event-level synchronization across all modules in the system is maintained.

3 VME Interface

The VME interface is used to provide access to configuration registers on the VSCM, bridge access to the FSSR2 registers, and provide a high bandwidth interface to the CPU for event readout. The A32 address space is dedicated to the event builder FIFO, roughly 2MB in size, and can be read using single-cycle and block transfer VME protocols. Typically block transfer protocols will be used for event readout and specifically the 2eSST is intended for use to maximize performance. The 2eSST protocols provides a near 200MB/s sustained transfer rate and supports the proprietary Jlab token-passing scheme that allows a single DMA operation on the CPU to transfer data from all VSCM modules in a sequential manner eliminating overhead compared to individual board transfers.

4 Event Builder

The event builder buffers all data received by all FSSR2 chips for a programmable latency time of up to 16μ. The FSSR2 data is tagged with a Global Trigger timestamp (48bits, 8ns resolution). In CLAS12, the trigger latency will be around 8μs. The VSCM is setup to extract event data within a programmable “lookback” window relative to the received trigger. Since the FSSR2 data is tagged with the equivalent global trigger timestamp, the event builder takes FSSR2 data words with global trigger timestamps that fall within the programmed “lookback” window. These data words are copied into the event FIFO and marked with the event number, trigger time, and other useful DAQ related bits to add redundancy helping to ensure reliable event-level synchronization with error checking. FSSR2 data words can be reported multiple times if trigger happen to have overlapping “lookback” time windows that include the same FSSR2 data word.

5 Event Buffer

The event buffer uses a 2MB external SRAM to form a large event FIFO. This buffer is large enough to hold several hundred events assuming 100% occupancy. This allows the event builder to create blocks of many events which significantly improves readout efficiency.

6 Calibration Pulser

The calibration pulser circuit provides a 2Vpp dynamic range, up to 125Msps, and 14bit resolution (for pulse height steps to be in sub mV increments). The bandwidth is sufficient to allow ~10ns rise times to be delivered over several feet of 50ohm coax cable terminated with 50ohms. Two independent outputs are provided to drive both HCFB modules. The pulser signal phase can be placed with a deterministic phase relationship to the BCO clock that drives the FSSR2.

7 FSSR2 Data Path

The FSSR2 chips provide event data through up to 6 LVDS pairs with a source synchronous clock. The VSCM supports receiving data from all 6 LVDS pairs from each FSSR2 running at 70MHz DDR (840Mbps from each FSSR2). Xilinx Spartan 6 FPGA chips are used to buffer and deserialize data from 2 FSSR2 chips each. Four of these chips are used to support 8 FSSR2 simultaneous data streams (coming from 2 HCFB interfaces), which send their information to the master FPGA where the event builder resides.

8 VSCM General Specifications

Triggering	
Trigger Rate (Peak @ 100% Occupancy)	~30MHz
Trigger Rate (Sustained @ 24% Occupancy)	10kHz
Trigger Latency (max)	16µs
Event Builder	
Event Buffer Size	2048kbyte
Event Buffer Max Events	limited by buffer size and event size
Event Buffer Max Hits	~500,000
Event Readout Rate (max)	200Mbytes/sec
FSSR2	
BCO Clock Period	128ns – 400ns
FSSR2 Readout	840Mbps