Nuclear Physics Division
Fast Electronics Group

Description and Requirements
for the
VXS SCM

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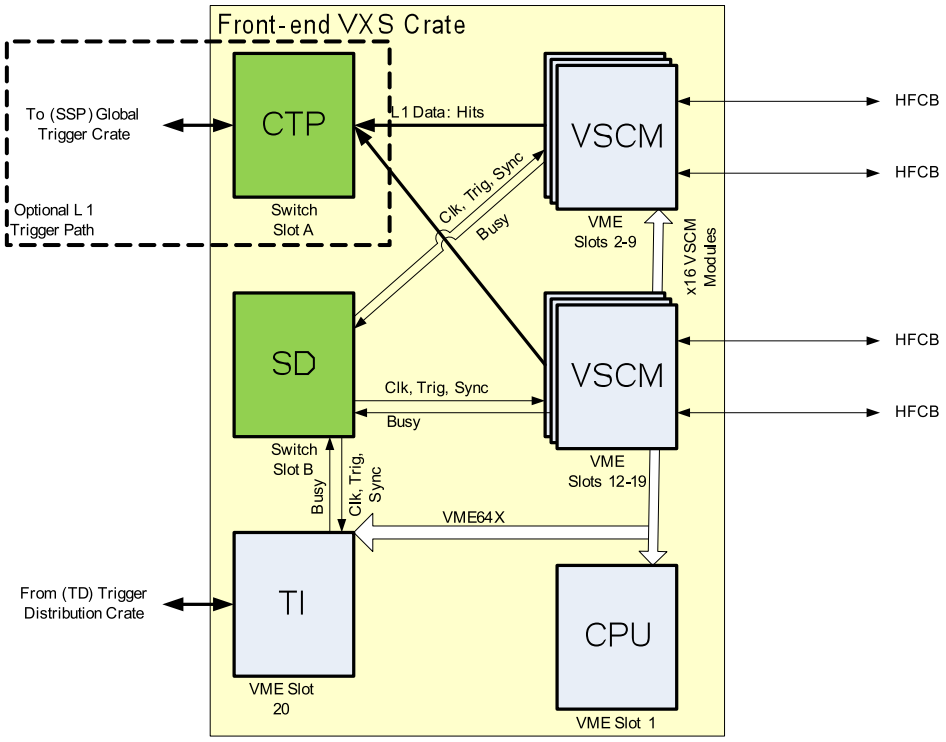
1 Introduction

The VSCM is a VME/VXS module that communicates with multiple FSSR2 chips on the Jefferson Lab Hybrid Flex Circuit Board (HFCB). The VSCM is responsible for configuring the FSSR2 registers, providing analog calibration pulses to the FSSR2 chips, delivering/monitoring proper control signals (clock, reset, status), and capturing serialized event data from the FSSR2. Each VSCM can interface to 2 HFCB modules and each HFCB has 4 FSSR2 chips. Up to 16 VSCM modules can reside in a VXS crate as shown in Figure 1a. When multiple VSCM modules are used additional cards are required to ensure event & timing synchronization. These additional modules are shown in Figure 1a and are the Trigger Interface (TI) and Signal Distribution (SD). Please refer to the particular module manual for further information. The VSCM does support a stand-alone mode useful when only 1 or 2 HFCB interfaces are used.

Figure 1a: VSCM in the 20 Slot VXS Crate



2. Purpose of the module

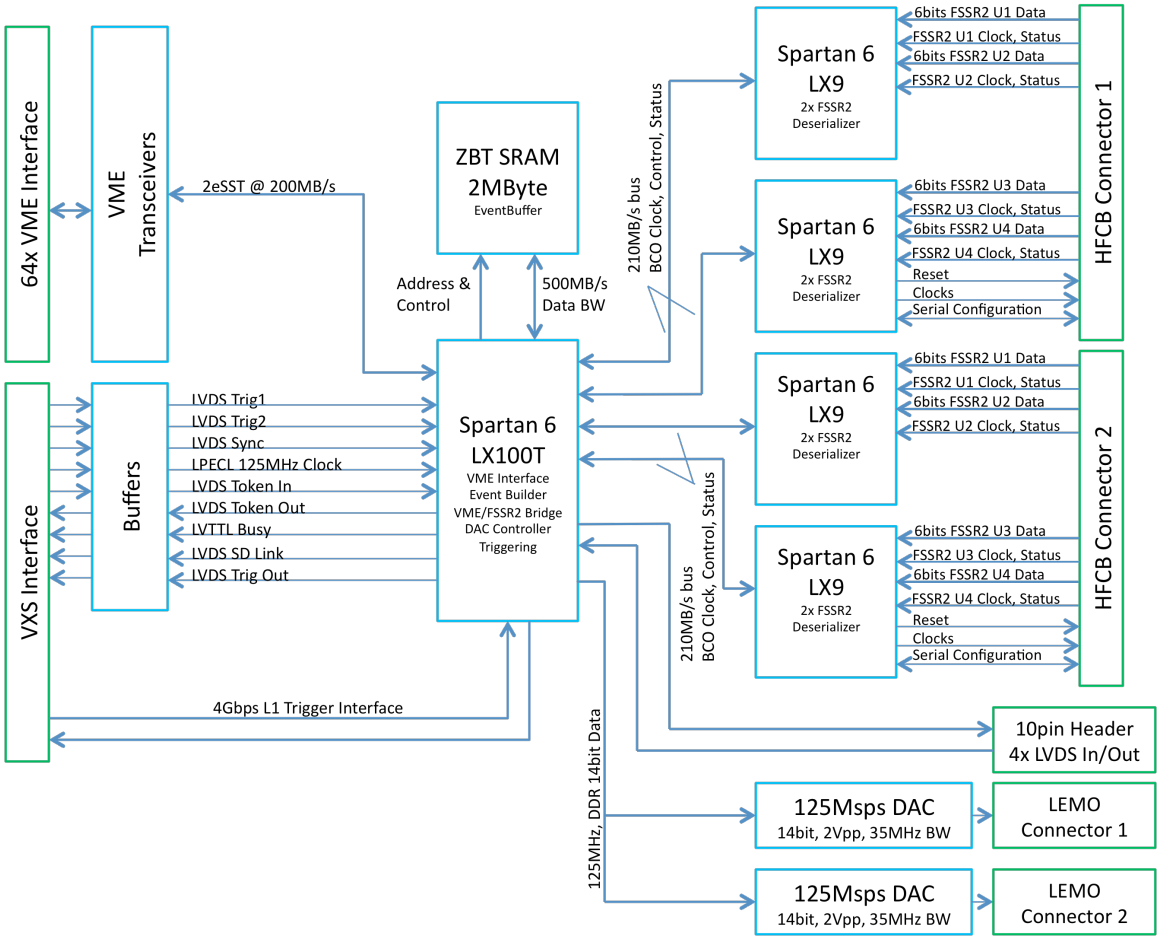
The main purpose of the VSCM is to convert the FSSR2 data-driven information stream into sparsified & triggered events that are correlated with external detectors. Idle status words are suppressed to minimize event size, but these status words are monitored to for diagnostic purposes of the individual FSSR2 chips. The event builder of the VSCM uses the BCO clock timestamp from each FSSR2 data word and matches it to the global system clock timestamp. Since the BCO clock is derived from the global system clock, triggers received by the VSCM will cause the event builder to extract only hits with specific BCO timestamps that correspond to a programmable time window where the physics event could have occurred on the HFCB. When a trigger is received the appropriate FSSR2 data words are copied into a new event buffer and pushed into

an event FIFO. These events can be readout in order with other modules in the system and event-level synchronization across all modules in the system is maintained.

3. Functional Description

In Figure 3a the block diagram of the VSCM is shown. The LX100T FPGA performs most of the work providing the VME interface, event building, event buffer logic, DAC waveform generator, L1 trigger logic, and synchronizes all FSSR2 data paths. Further details on each of these pieces are discussed below.

Figure 3a: VSCM Block Diagram



3.1 VME Interface

The VME interface is used to provide access to configuration registers on the VSCM, bridge access to the FSSR2 registers, and provide a high bandwidth interface to the CPU for event readout.

The A32 address space is dedicated to the event builder FIFO, roughly 2MB in size, and can be read using single-cycle and block transfer VME protocols. Typically block transfer protocols will be used for event readout and specifically the 2eSST is intended for use to maximize performance. The 2eSST protocols provides a near 200MB/s sustained transfer rate and supports the proprietary Jlab token-passing scheme that allows a single DMA operation on the CPU to transfer data from all VSCM modules in a sequential manner eliminating overhead compared to individual board transfers.

The A24 address space is reserved for board register access. This address range does not support block transfer modes. Register access details will be provided in the board register description section discussed later.

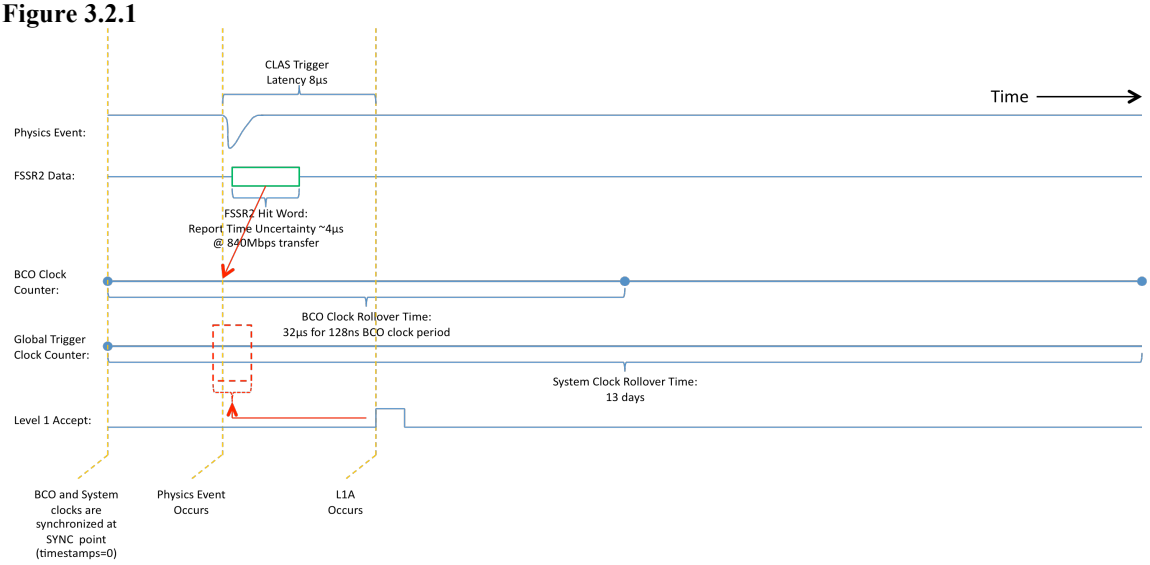
3.2 Event Builder

The event builder buffers all data received by all FSSR2 chips for a programmable latency time of up to 32μ . The FSSR2 data is tagged with a Global Trigger timestamp (48bits, 4ns resolution). The FSSR2 outputs hit/ADC/channel data tagged with a BCO clock number, but the start time of the BCO clock and Global Trigger clock is the same. Even though the 8bit BCO clock number rolls over after 32µs (based on 8MHz BCO clock), it can easily be matched to the global timestamp because the time elapsed from BCO clock timestamp to receipt of the data by the main FPGA (~4µs @ 840Mbps) is much less than the rollover time (32µs). This allows a BCO clock number to easily be translated to the Global Trigger timestamp.

In CLAS, the trigger latency is expected to be around 8µs. The VSCM is setup to extract event data within a programmable "lookback" window relative to the received trigger. Since the FSSR2 data is tagged with the equivalent global trigger timestamp, the event builder takes FSSR2 data words with global trigger timestamps that fall within the programmed lookback window. These data words are copied into the event FIFO and marked with the trigger number, trigger time, and other useful DAQ related bits to add redundancy helping to ensure reliable event-level synchronization with error checking. FSSR2 data words can be reported multiple times if trigger happen to have overlapping lookback time windows that include the same FSSR2 data word.

Figure 3.2.1 shows a general timing diagram the may help to see how the event builder is able to select the correct FSSR2 data words that should be associated for a given trigger. First, all readout modules in the trigger system are derived from the same global clock (FSSR2 use a BCO clock that is derived from this same clock). All onboard global clock counters and FSSR2 BCO clock counters are synchronously reset. When a physics event occurs, the FSSR2 spits out a corresponding data word in up to 4µs. The VSCM receives this data word and uses the BCO clock number to figure out the corresponding Global System Clock timestamp. About 8μs later a Level 1 accept trigger is received. The VSCM uses the programmable lookback window registers to extract all FSSR2 data words that are tagged with a Global Clock timestamp that satisfy the lookback window requirements. This logic ensures that the FSSR2 events extracted are those associated a time window having afixed latency timing requirement with respected to the physics event.

Figure 3.2.1



3.3 Event Buffer

The event buffer uses the 2MB external SRAM to form a large event FIFO. This buffer is large enough to hold several hundred events assuming 100% occupancy. This

allows the event builder to create blocks of many events, which decreases data overhead.

3.4 Calibration Pulser

The calibration pulser circuit provides a 2Vpp dynamic range, up to 125Msps, and 14bit resolution (for pulse height steps to be in sub mV increments). The bandwidth is sufficient to allow ~10ns rise times to be delivered over several feet of 50ohm coax cable terminated with 50ohms. Two independent outputs are provided to drive both HCFB modules. The pulser signal phase can be placed with a deterministic phase relationship to the BCO clock that drives the FSSR2.

3.5 FSSR2 Data Path

The FSSR2 chips provide event data through up to 6 LVDS pairs with a source synchronous clock. The VSCM supports receiving data from all 6 LVDS pairs from each FSSR2. Assuming sufficient eye opening though the HCFB cabling, the VSCM is fully capable of receiving DDR data at up to 70MHz (840Mbps per FSSR2). Low cost Spartan 6 FPGA chips are used to buffer and deserialize data from 2 FSSR2 chips. Four of these chips are used to support 8 FSSR2 simultaneous data streams (coming from 2 HCFB interfaces). Each Spartan 6 deserializer FPGA will combine the 2 FSSR2 data streams into a single higher speed data stream that is sent to the main Spartan 6 processing FPGA.

3.6 VXS/Front Panel I/O

The VXS connection is used to interface to the trigger system without the need for loose cabling. This interface provides the following signals:

Signal	Description	Direction	Signal Type
Clock	125MHz System Synchronous Clock	Input	LVPECL
Trig1	L1 accept trigger bit, synchronous to clock	Input	LVPECL
Trig2	L1 accept trigger bit, synchronous to clock	Input	LVPECL
Sync	L1 synchronization bit, synchronous to clock	Input	LVPECL
Busy	Module busy signal	Output	LVTTL
Token In	Used in VME 2eSST token passing scheme	Input	LVDS
Token Out	Used in VME 2eSST token passing scheme	Output	LVDS
Trigger Out	Module trigger bit	Output	LVDS
SD Link	Undefined serial link to SD	Output	LVDS
L1 Trigger	5Gbps link used to generate L1 trigger	Input/Output	CML

Clock

This clock signal is derived from the TI or Trigger Distribution Crate and is used to allow synchronous operation across multiple modules within a crate as well as across multiple crates.

Trig1, Trig2

These trigger bits tell the module when to capture and store an event. Upon receipt of a trigger signal, the VSCM will parse the front-end data and extract physics event data that matches a time-window related to the received Trig1/Trig2 time.

Sync

The sync signal is used to align/start board timers at the same time as other boards in the crate and system. This signal will also be used to reset the FSSR2 chips to ensure the BCO clock timer are synchronized to the VSCM global timer.

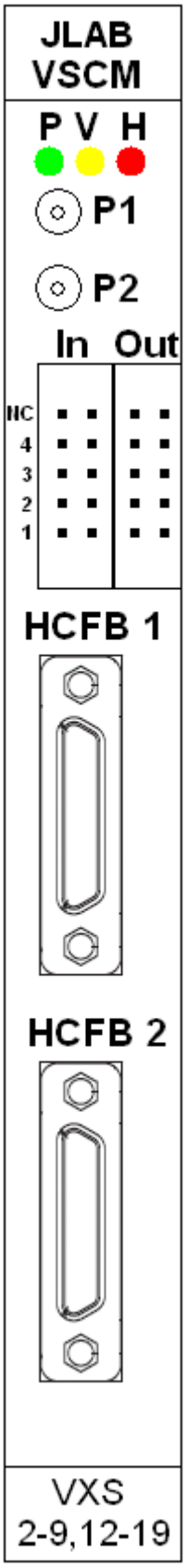
Busy
Busy is normal held low, but if the VSCM module event buffers become close to full the busy signal can be set high to signal that the trigger supervisor must stop sending triggers so the module buffers to not overflow. If buffer overflows happen event synchronization from this module to another is lost.

Token In/Token Out
These are used by the VME interface when performing 2eSST transfers with token passing.

SDLink
Currently a undefined serial link to the Signal Distribution board.

L1 Trigger
This is a high speed serial link to the Crate Trigger Processor used to send processed front-end data to the Global Trigger System that can be correlated with other modules/detectors to generate a L1 trigger accept. Currently the SVT is not planned to be part of the L1 trigger, but the VSCM supports this feature if it is desired in the future. Potentially some level of track reconstruction on the SVT could be done in hardware to provide a high level trigger that would benefit experiments.

4. Specifications



MECHANICAL
- Single width VITA 41 Payload Module

HIGH SPEED SERIAL P0 INPUTS/OUTPUTS:
- 125MHz LVPECL Clock
- Trig 1, Trig 2, Sync Inputs
- 2x 2.5-3.125Gbps Lanes to CTP

Front Panel INPUTS/OUTPUTS:
- 2x HCFB Microdot Connectors
  - 6x LVDS 70MHz DDR lines per FSSR2
  - Serial Configuration
  - 3-10MHz programmable BCO clock
  - 0-70Mhz programmable RCLK
- 2x LEMO DAC Transformer Isolated Calibration Outputs
- 4x LVDS Outputs
- 4x AnyLevel Inputs (LVPECL, ECL, LVDS)

INDICATORS: (Front Panel)
- Power OK – Green LED
- VME DTACK – Red LED
- HCFB Status – Yellow LED

EVENT BUILDER:
- 2MB Event FIFO
- High trigger rate capable >>10kHz
- 32µs maximum trigger latency

DIAGNOSTICS:
- Per channel scalers (1,024)
- FSSR2 data integrity monitor
- FSSR2 chip status
- Event builder status

PROGRAMMING:
- On board JTAG Port, VME

POWER REQUIREMENTS:
- +5.0v @ 4A Typ

ENVIRONMENT:
- Commercial grade components (70 Celsius)

5. PCB Layout View