The Trigger and Clock Distribution for GLUEX Experiment (or 12 GeV Upgrade Experiments?)

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Abstract

Trigger and Clock distribution system for the GLUEX[1] experiment at the Continues Electron Beam Accelerator Facility (CEBAF) 12 GeV upgrade [2] in TJNAL is described. The trigger and clock distribution system includes Trigger Supervisor (TS)[3] printed circuit board (PCB), Trigger Distribution (TD)[4] PCB, Trigger Interface (TI)[5] PCB, Signal Distribution (SD)[6] PCB, VXS crates [7] and optical fibres. The TS is the main hardware interfacing between the trigger system[8] and Data Acquisition system (DAQ)[9], and it is the sources for the distributed trigger and clock signals. The SD and TD modules are the main fan out hardware. The TI is the main hardware interfacing between the DAQ and the front end electronics. Together with bundled optical fibres, the dedicated high speed point to point connections between the switch slot and payload slots on P0 connectors in VXS crate are used for signal transmission.

Field Programmable Gate Arrays (FPGA) are utilised on all boards in the system to provide programmability. The prototype was intensively tested on the bench. The trigger and clock distribution system is under mass production, and will be installed for the experiment by 2013.

Keywords:

Data Acquisition (DAQ), Trigger distribution, Clock distribution, 12 GeV upgrade, CEBAF (Continuous Electron Beam accelerator Facility), Electronics System

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I. INTRODUCTION

GlueX experiment is the first experiment in the new experiment hall (HallD) as part of the 12GeV upgrade of the Continues Electron Beam Accelerator Facility (CEBAF) at Thomas Jefferson National Accelerator Laboratory (TJNAL). The CEBAF accelerator consists of a pair of superconducting radiofrequency linacs linked by recirculation arcs for up to five acceleration passes. It serves three experimental halls with simultaneous, continuous-wave beams, with a final energy of up to 6 GeV thanks to incremental improvements in cryomodule technology. The 12 GeV upgrade will double the beam energy by using higher performing seven cell cavities while maintaining the overall length of the original cryomodule design. Using space already available in the accelerator tunnels, add another recirculationg arc to boost the energy to 12 GeV in the newly constructed experiment hall.

The 12 GeV Upgrade is a unique opportunity for the nuclear physics community to expand its reaches into unknown scientific areas. For the first time, researchers will be able to probe the quark and gluon structure of strongly interacting systems to determine whether QCD (quantum chromodynamics), the theory believed to describe strong interactions, gives a full and complete description of hadronic (3 quark) systems. JLab at 12 GeV will make profound contributions to the study of hadronic matter-the matter that makes up everything in the world.

The new experimental Hall will use the electron beam to produce a coherent bremsstrahlung beam and house a solenoid detector to carry out a program in gluonic spectroscopy to experimentally test current understanding of quark confinement. All three existing halls will be upgraded to receive the new Five-pass, 11 GeV beam. The additional experimental equipment proposed for Halls A, B and C take full advantage of currently installed apparatus. Figure 1 shows a picture of the GlueX detector setup.

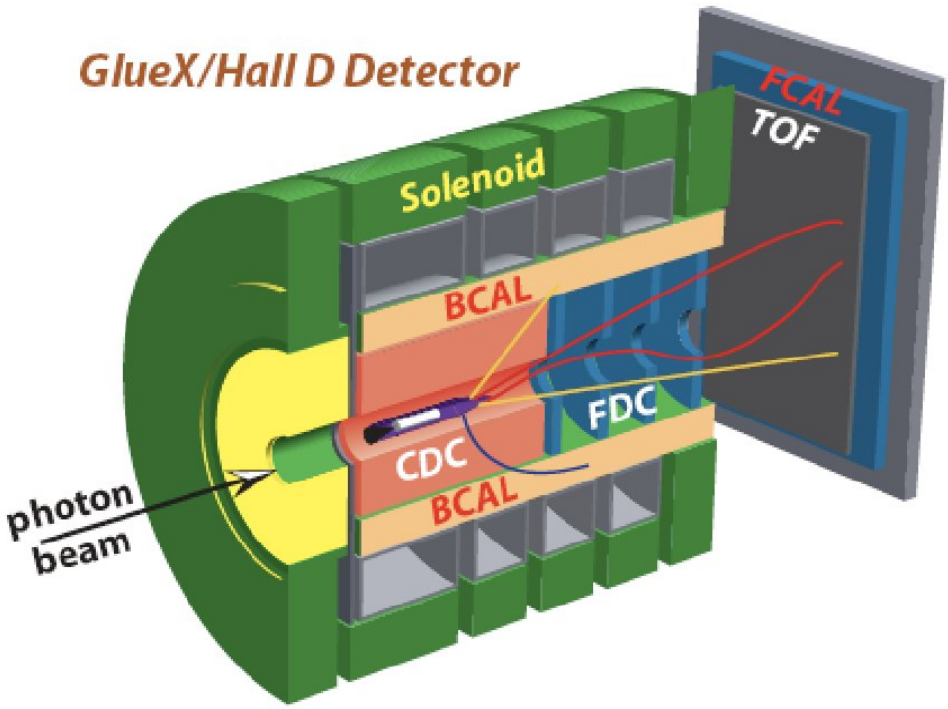

Figure 1 GlueX experiment for CEBAF 12 GeV upgrade

The detector is enclosed in a superconducting solenoid magnet. From inside to outside, the detector includes Central Drift Chamber (CDC), Forward Drift Chamber (FDC), Time Of Flight detector (TOF), Barrel Calorimeter (BCAL) and Forward Calorimeter (FCAL). These detectors are used to measure the momentum and the energy of the secondary particles.

The signals from the detector are amplified, shaped, and/or discriminated, and converted to digital data. The digital data are stored temporarily on the front end readout electronics (ADC modules or TDC modules) in the front end crates. For the GlueX experiment, there are about sixty front end crates in the experiment hall sitting around the detector in the racks. The VME Switched Serial (VXS) crates are used in the experiment. The VXS crate has the advantage of VME64x and dual star high speed switching. Each of the two switch slots is connected to the other slots (payload slots) using eight dedicated high speed differential signals.

The trigger system uses the detector characters to select the interesting beam target interaction events by primarily using the calorimeter (BCAL and FCAL) energy measurements. The pipelined trigger will be formed every 4ns with trigger acceptance rate up to 200 kHz. The final trigger signal (up to 200 kHz rate) will initiate the detector information readout by the Data Acquisition (DAQ) system.

The DAQ system is built on the VME ReadOut Controller (ROC). The ROC uses the VME bus to readout the data from front end modules. Because of the readout overhead, it is more efficient to group the data in blocks of triggers (events) for readout, especially at high trigger rates. Each ROC has a fraction of the detector

data. The online computers will assemble the data from all ROCs, and form event, which includes the full detector data. The DAQ can further select events, and save the data to permanent storage.

Trigger/clock distribution system is the interface between the trigger system and DAQ system. Figure 2 shows a diagram of the distribution scheme. It distributes a universal clock of frequency of 250 MHz to pipeline the system. It distributes the event selection result, trigger, from trigger system and initiate the detector information readout, the data acquisition (DAQ) process. It distribute a encoded SYNC signal for the system synchronization. The front end electronics status is monitored by the distribution system, and make sure the smooth running of the experiment.

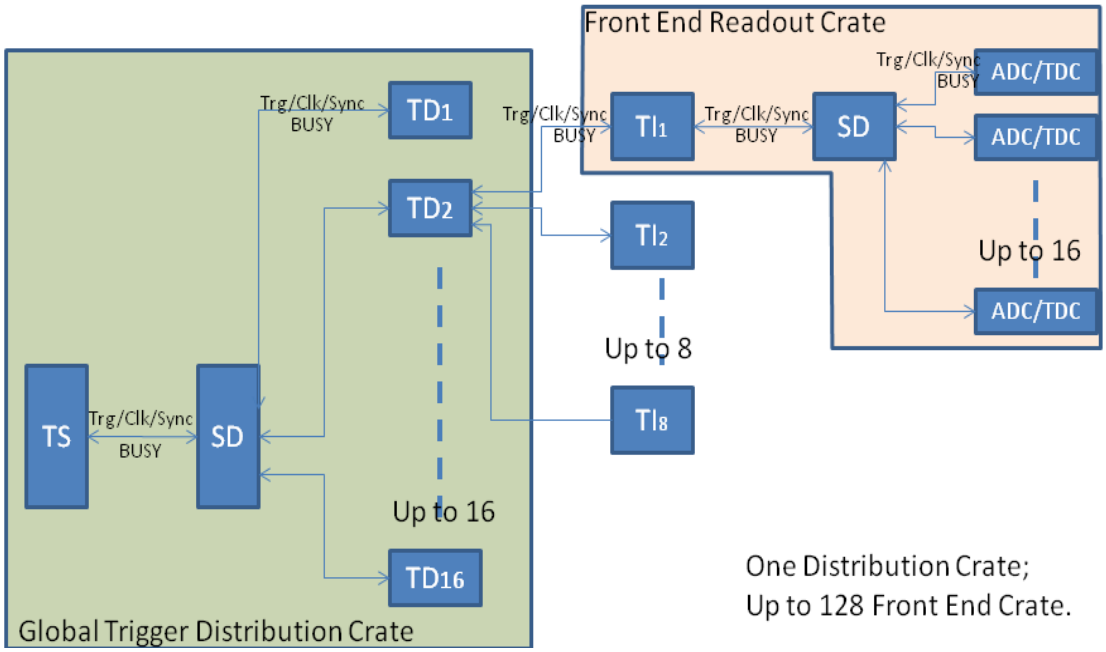

Figure 2 Diagram of the trigger and clock distribution system

The main hardware of trigger and clock distribution system includes a Trigger Supervisor (TS) printed circuit board, Signal Distribution (SD) printed circuit boards, Trigger Distribution (TD) printed circuit boards, Trigger Interface (TI) printed circuit boards, VXS crates and optical fibres. The TS, one SD and up to sixteen TD modules sit in the global trigger/clock distribution crate. There are one TI and one SD in each front end crate. The trigger signal is controlled by the TS, and the trigger word (trigger plus trigger information) is serialized by TS. The serialized trigger word is fanned out by the SD and TD. The TI receives the serialized trigger word and decodes these signals, then send to the front end crate (fanned out through SD), and initiate the DAQ (ROC readout).

The electronics boards are custom designed and produced for the 12 GeV upgrade. Field Programmable Gate Arrays (FPGA) are used for trigger/clock/sync generation, control and decoding. Optical Fibres and high speed differential backplane connections are used to transmit signals at high speed and long distance.

The trigger and clock distribution hardware will be discussed in next section. The system synchronization will be discussed in the third section. And the current status will be shortly discussed in the last section.

II. HARDWARE DISCRIPTION

A. Trigger Supervisor(TS)

1) TS Overview

TS is the very top PCB module in the trigger and clock distribution system. The TS is hardware decision making module for the Data Acquisition (DAQ) system. It accepts trigger decisions from the Global Trigger Processor(GTP), and it further processes the trigger signals and sends the trigger signals down to the Trigger Interface (TI) modules through Signal Distribution (SD) board and the Trigger Distribution (TD) modules to initiate data acquisition process.

TS supplies a 250 MHz system clock for trigger and data acquisition. The trigger and the front end data acquisition modules are pipelined on the 250 MHz clock. The system is almost dead time free and fits the character of continues beam of CEBAF.

The TS can also accept arbitrary external inputs and supply monitoring outputs for the added flexibility and tests of the DAQ system. Figure 3 is a picture of the TS printed circuit board (PCB).

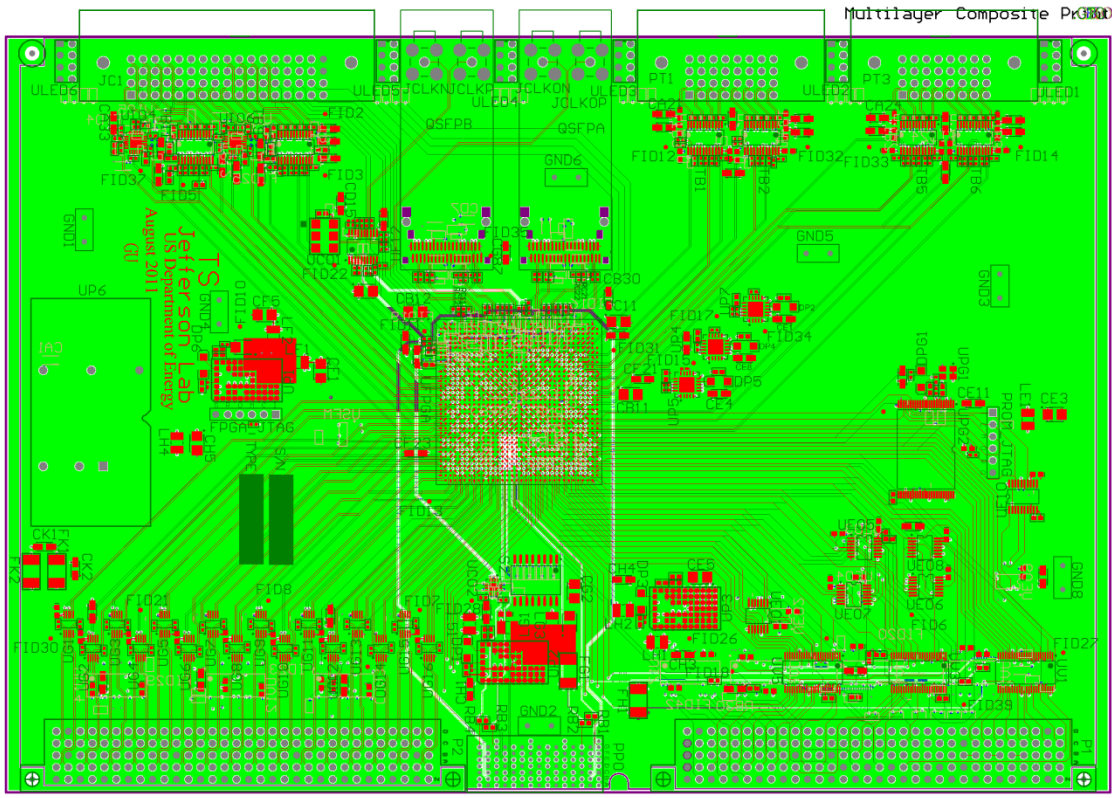

Figure 3 picture of Trigger Supervisor (TS) printed circuit board

2) TS Design

TS is designed as a VXS payload slot #18 board with a physical size of 6Ux160mm. It receives up to 32 trigger signals from the GTP via the VME P2 connector user defined pins via a backplane IO card. The signals are level shifted from LVPECL to LVDS by Micrel SY58607 differential receivers. The receivers also serve as FPGA input protection and isolation. The TS can also receive four groups (could be subdetectors) of external inputs with eight triggers per group through its front panel. These groups of external input signals are received by Maxim MAX8602 discriminator chips, so the inputs are compatible with almost any differential signal levels. To be compatible with earlier experiment setup and facilitate the DAQ test, there are sixteen generic inputs (could be trigger, busy or inhibit, etc), and twenty-two generic outputs for monitoring. There are also 24 outputs going directly to the six quad-pack LEDs. SMA connectors are mounted on the front panel for the optional clock input and output.

As a VXS payload card, it is compatible with VME64x. It has VME A24D32 registers for board setup and monitoring. It supports A32D32, block and 2ESST data readout. It can even be configured as a VME master board.

The trigger, clock and synchronization signals are transmitted via the VXS P0 connector using the high speed differential paired signals to the SD in the global trigger distribution crate for fan out. Figure 4 is the functional diagram of the TS.

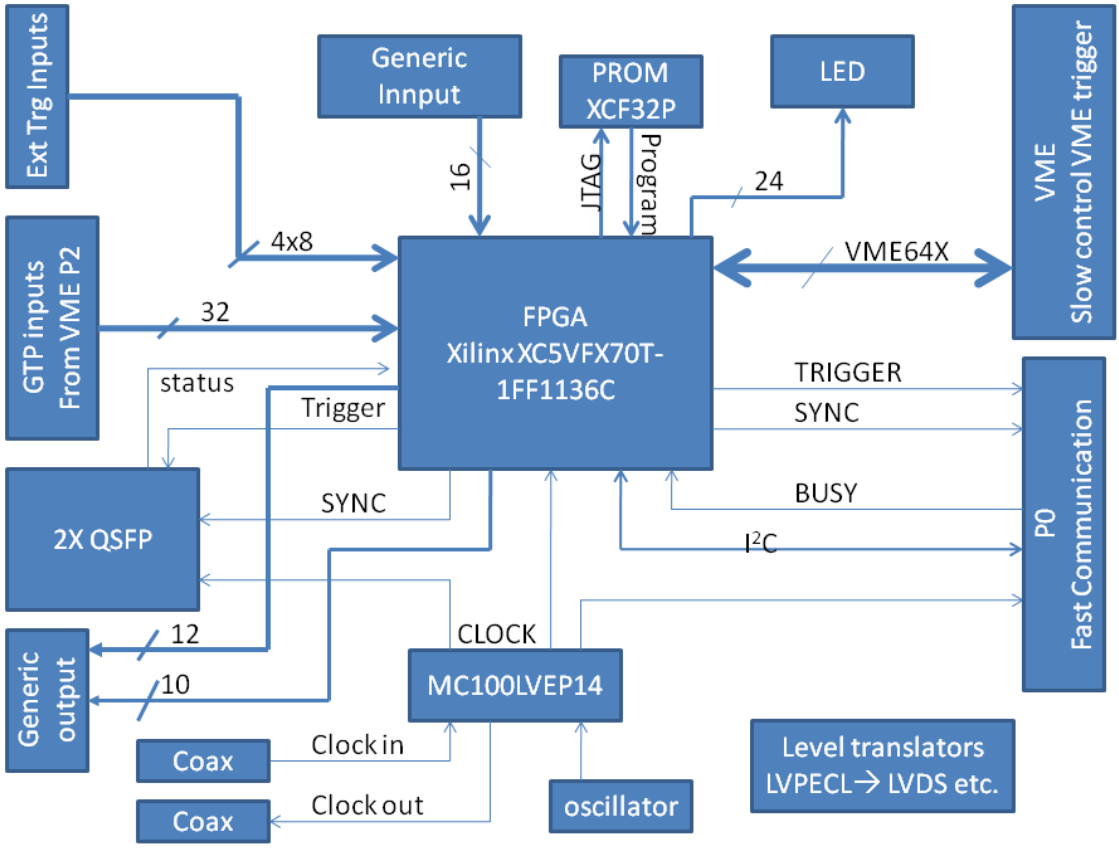

Figure 4 TS functional diagram

The TS can pre-scale and inhibit the trigger inputs to synchronize the DAQ. It can also generate triggers by VME command for system tests. The trigger and trigger information are combined into a 16-bit trigger word. This trigger word is serialized and sent to the SD in the trigger/clock distribution crate. This trigger word is fanned out by SD and TD, and received and decoded by the TI. The 16-bit trigger words are serialized by the FPGA's built in Multi-gigabit Transceivers (MGT) at 62.5MHz, that is, every 16ns. The trigger is generated on 250MHz clock and has a time resolution of 4ns. The trigger time information is sent as part of the trigger word. Table 1 is the trigger word definition:

Table 1 Trigger word definition

Bit 15	Bit 14	Bit 13	Bit12-11	Bit10-0	comment
parity	1	0	Trigger time in the 16ns window	Trigger type	triggered

parity	0	1	Trigger command	VME command
parity	0	0	TS timer	TI sync check
parity	1	1	Trigger content	Additional trigger information

An On-Semi MC100LVEP14 differential clock driver is used for clock fanout. The TS can receive an external input as the main clock source. The external clock input can be a clock generator, or the CEBAF synchronized clock. It can also use its on-board oscillator as the main clock. The source is selected by a hardware switch to be flexible, and less prone to problems. The clock is fanned out to the FPGA, front panel outputs and VXS P0 backplane. The P0 backplane clock is received by the SD and further fanned out to the TD, then to the TI and the whole system. When the system run on the accelerator synchronized clock, the TS clock could be used as TDC time zero.

The TS FPGA built in Digital Clock Manager (DCM) is used to generate the 125MHz and 62.5MHz lower speed clocks for trigger word serialization. The generated clocks are also used to keep the system synchronized.

Another signal distributed by the TS is the SYNC. The SYNC is an encoded four bits serialized command transferred at 250Mbps. Normally, the SYNC stays at logic high (or '1'). When transferring a SYNC command, the SYNC goes to logic low for one bit, then followed by the 4-bit command code. After the 4-bit SYNC command, the SYNC goes to logic high again. There is a minimum of four '1's before the next SYNC command. To facilitate the AC coupled fiber optical transceivers, the SYNC is Manchester encoded on TS, and Manchester decoded on the TI, to ensure the DC balance on the fibre media. Table 2 shows some SYNC command codes.

Table 2 SYNC command codes

4-bit SYNC code	SYNC action
0000 or 1111	Invalid codes
1101	Front end crate reset
0101	Trigger start/trigger link enable, trigger FIFO read counter reset
0111	Trigger stop/trigger link disable, and trigger FIFO write counter reset
0010	System clock resynchronization

0001	TI VME clock DCM reset
0100	Reset the TI GTP status register
Others	To be assigned

3) TS FPGA Design

The main function of the TS FPGA is trigger and sync generation to synchronize the DAQ system. Figure 5 is the diagram of the trigger word generation in FPGA.

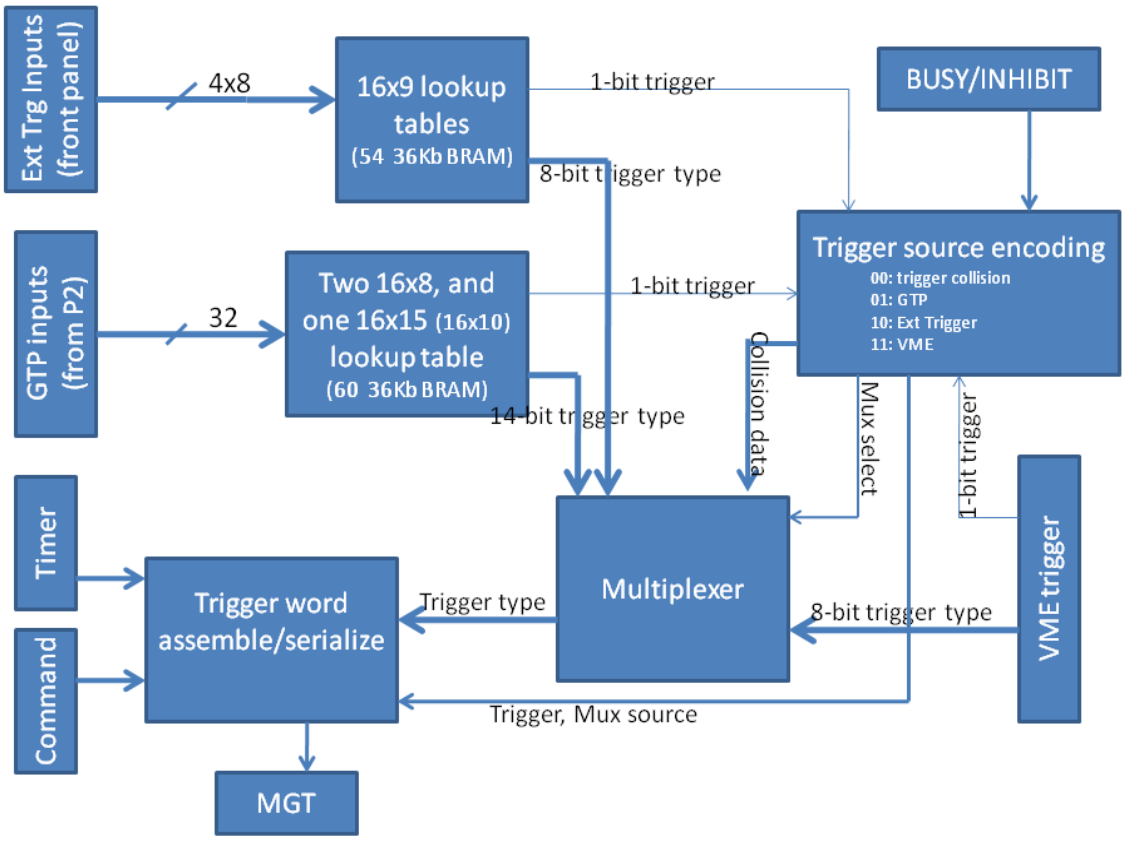

Figure 5 Functional diagram of TS trigger word generation inside the FPGA

An 8-bit trigger type word is generated from 32 trigger inputs by a two level 16-bit address and 8-bit output look up tables as shown in the FPGA diagram. The Look up table is implemented in the FPGA Block RAM. The total Block RAM used is about four Mega bits, which can fit in the XC5VFX70T FPGA comfortably. The various trigger sources are controlled by the trigger throttling logic, and the multiplexed trigger types from different sources are assembled as the 16-bit trigger words. These trigger words are serialized by the FPGA builtin MGT modules, and sent out of the FPGA and the TS every 16ns.

The 4-bit SYNC command is serialized and transferred at the speed of 250 Mbps. The 4-bit command uses a time window of 16ns too. The SYNC command can be adjusted, so the phase of 4-bit command has a fixed phase delay relative to the 62.5MHz clock used for the trigger word transfer. This phase relation is used to synchronize the slower clocks on the TI to the TS' 62.5 MHz clock.

In addition to the trigger word and SYN signal generation, the TS FPGA has two VME to I^2C engines and two VME to JTAG engines. Each of the I^2C engines is connected to one switch slot in the VXS crate, to serve as a bridge between the VME controller and the switch slot board. The JTAG engines connect to the FPGA JTAG port and PROM JTAG port. The ports can be used to load the PROM, readout the chip identification codes and user programmable code. The chip ID code is a unique code to identify the hardware device, while the user programmable code is programmed by the firmware developer. The TS PROM user code includes the TS serial number, and TS identification information. The TS FPGA user code includes the firmware revision information.

4) TS FPGA programming

The TS FPGA is Xilinx XC5VFX70T-1136, which needs about 27 Mbit of uncompressed data to configure the FPGA. A XCF32P PROM is used in serial mode to configure the FPGA and store the configure file when the power is out. When the FPGA configuration bits are compressed, the PROM can hold two versions of the firmware. This two versions design makes switching the TS operation modes very easily.

The PROM can be loaded remotely by VME command. A user defined address modifier (AM) code 0x19 is used to load the XCF32P PROM by a discrete logic engine for VME to JTAG decoding. This loading does not depend on the FPGA and works on a bare board from the assembly house. This process loads one bit of PROM data per VME transfer. To increase the efficiency of VME transfer, the second VME to JTAG engine is implemented inside the FPGA. With the FPGA JTAG engine, 32-bits are loaded into the PROM per VME command. This process is much more efficient than that of the discrete logic engine, but it works only when the FPGA is programmed and working.

B. *Signal Distribution (SD) board:*

SD is designed as VXS switch slot#B (as physical slot#12 in the 21-slot VXS crate) module with physical size of 6Ux160mm. Figure 6 is a picture of the SD card.

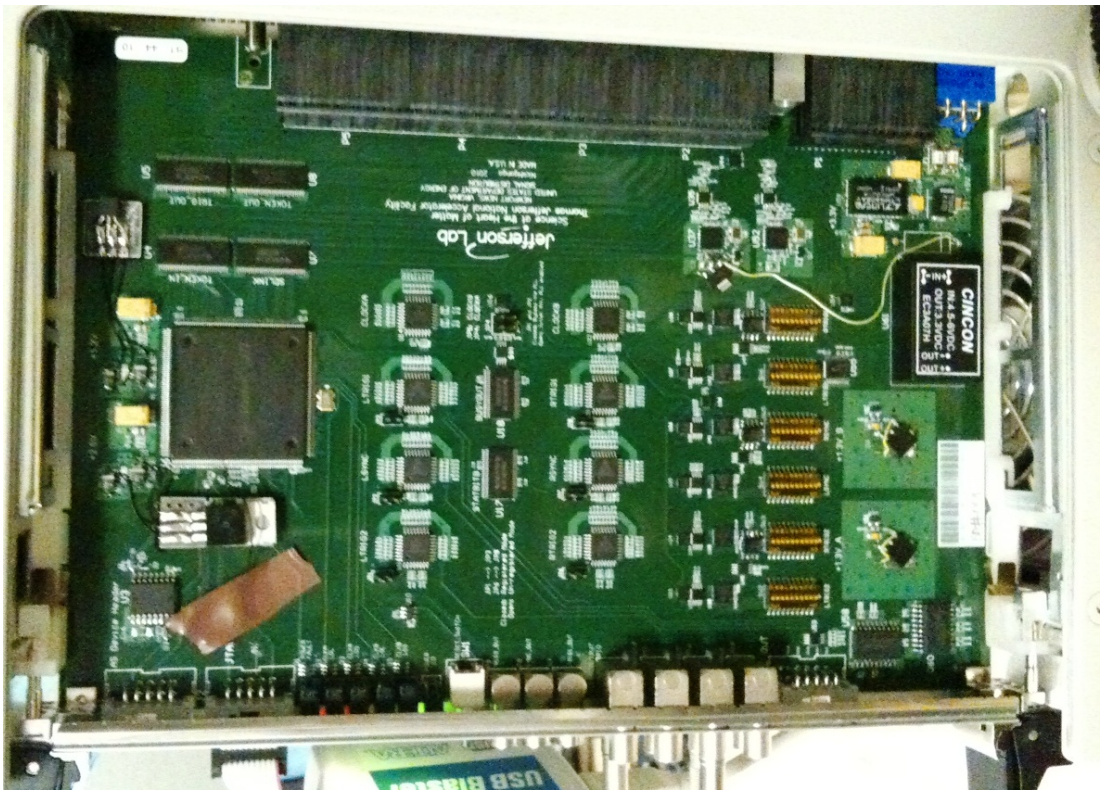

Figure 6 The Signal Distribution Module

The SD card receives Trigger, Clock and SYNC signals from the VXS payload slot#18, and fans out the signals to sixteen VXS payload slots, that is, Payload slot#1 to slot#16 through VXS P0 connectors using high speed differential signals. In the global trigger/clock distribution crate, the payload slot#18 hosts TS board, and payload slot#1 to slot#16 host TD boards. In the front end crates, the slot#18 hosts a TI board, and slot#1 to slot#16 host front end electronics boards(Flash ADC, TDC, etc.)

The SD also receives the BUSY status signals from payload slot#1 to payload slot#16 boards, and merges the BUSY signals and sends to the payload slot#18 boards. This BUSY status is used to throttle the trigger sent from TS to keep the DAQ system synchronized.

The SD has the option to clean up the clock jitter using SiliconLab SL5538 PLL component. The jitter cleaned output clock can also be phase delayed. This gives the option of aligning the front end crate clock phases. Figure 12 shows the clock jitter before and after the cleanup. After the cleanup, the clock jitter is about 1ps, which is close to the measuring limit of our equipments.

C. Trigger Distribution (TD) board:

The TD is a VXS payload module with a physical size of 6Ux160mm. Its main function is to fan out the trigger, clock and SYNC signals and to collect the front end crate status information using the optical fibres. Figure 7 is a picture of the TD board.

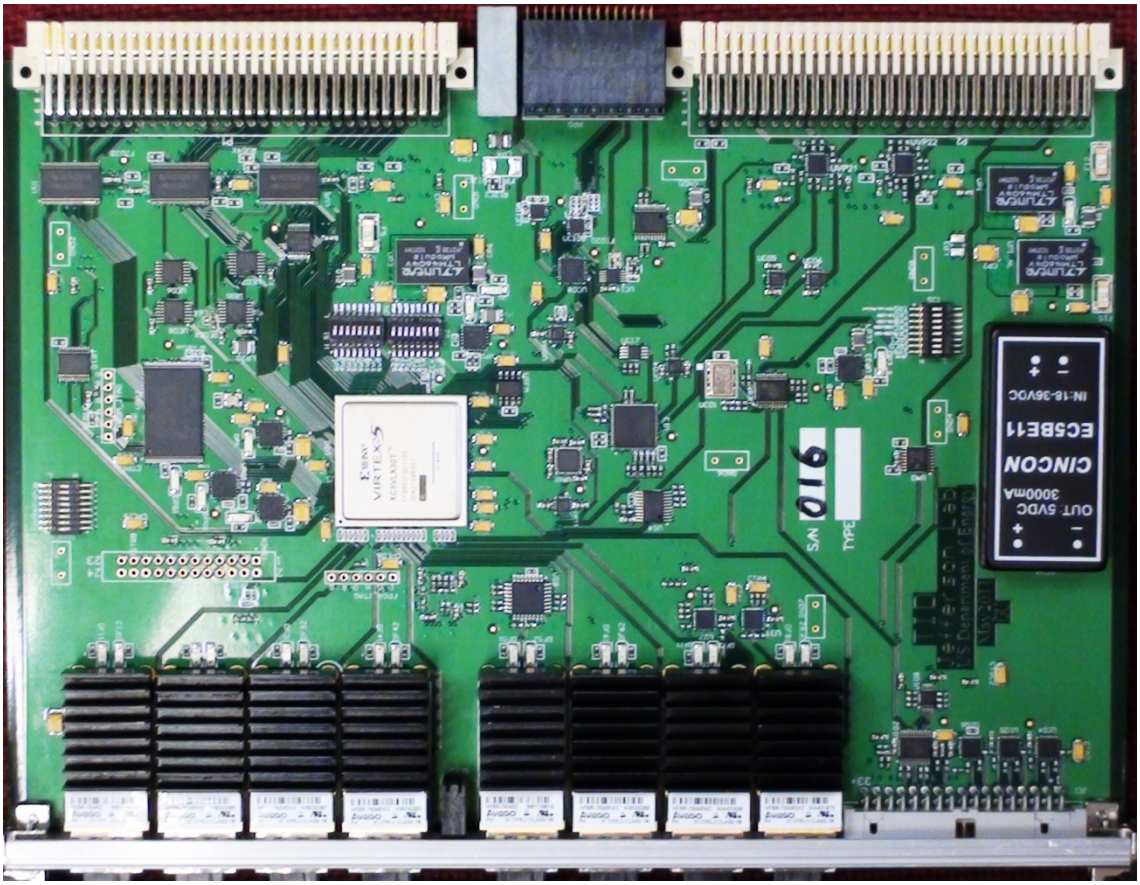

Figure 7 Trigger Distribution (TD) board.

The TD receives the trigger, clock and SYNC signals through the P0 connector from TS via SD fan out. The trigger signal is re-sampled using the Analog Devices' ADN2805 component. The trigger, clock and SYNC signals are fanned out to eight optical transceivers (Avago HFBR-7924). Each optical transceiver drives a set of fibers, and connects to one TI board in the front end crate.

The TD also receives the status from eight TI boards through the optical transceivers. The status words are deserialized by the FPGA builtin MGT modules. The status words include the front end crate (the crate that TI resides) BUSY, readout acknowledge, trigger received, and some other status. The TD merges the BUSY signals from eight TI boards, and sends to the SD, then the SD sends the BUSY to the TS. The TD can assert the BUSY if the number of events buffered at the front-end crate, which is the difference between the number of triggers it fans out and the number of readout the front end crate performed, is over a preset limit. The logic is

used to limit the number of events buffered on the front end electronics, or the buffer usage on the front end electronics. The special case is the event locking readout mode when the preset limit is one.

The TD board uses a Xilinx XC5VLX30T-665 FPGA. The FPGA needs about 9 Mbit of uncompressed data to configure the FPGA. A XCF32P PROM is used to configure the FPGA. When the FPGA bits are not compressed, the PROM can hold two versions of the FPGA firmware, and the FPGA can be programmed in parallel mode or serial mode. When the FPGA program bits are compressed, the PROM can hold four versions of the firmware. This multiple versions design makes switching the TD operation mode very easily.

The PROM can be loaded remotely by VME command. The mechanism is the same as that implemented on the TS. For the details, refer to the TS design description. Though the TD and TS are residing in the same crate, the TD and TS are in different slots and they have their own geographic addresses as defined by the VME64x protocol, there will be no confusion between TS and TD in the VME operation.

D. *Trigger Interface (TI) board*

1) TI Overview

TI is designed as a VXS payload slot#18 board with a physical size of 6Ux160mm. It receives the trigger, clock, and SYNC signals from TD. It decodes the trigger and SYNC, and sends them to SD then to the whole front end crate. Each front end crate has one TI. To optimize the system design, the TI shares the same PCB with the TD, but the components are populated differently. Figure 8 shows a picture of the TI. The TI and TD are using the same FPGA, Xilinx XC5VLX30T, though their firmware is different.

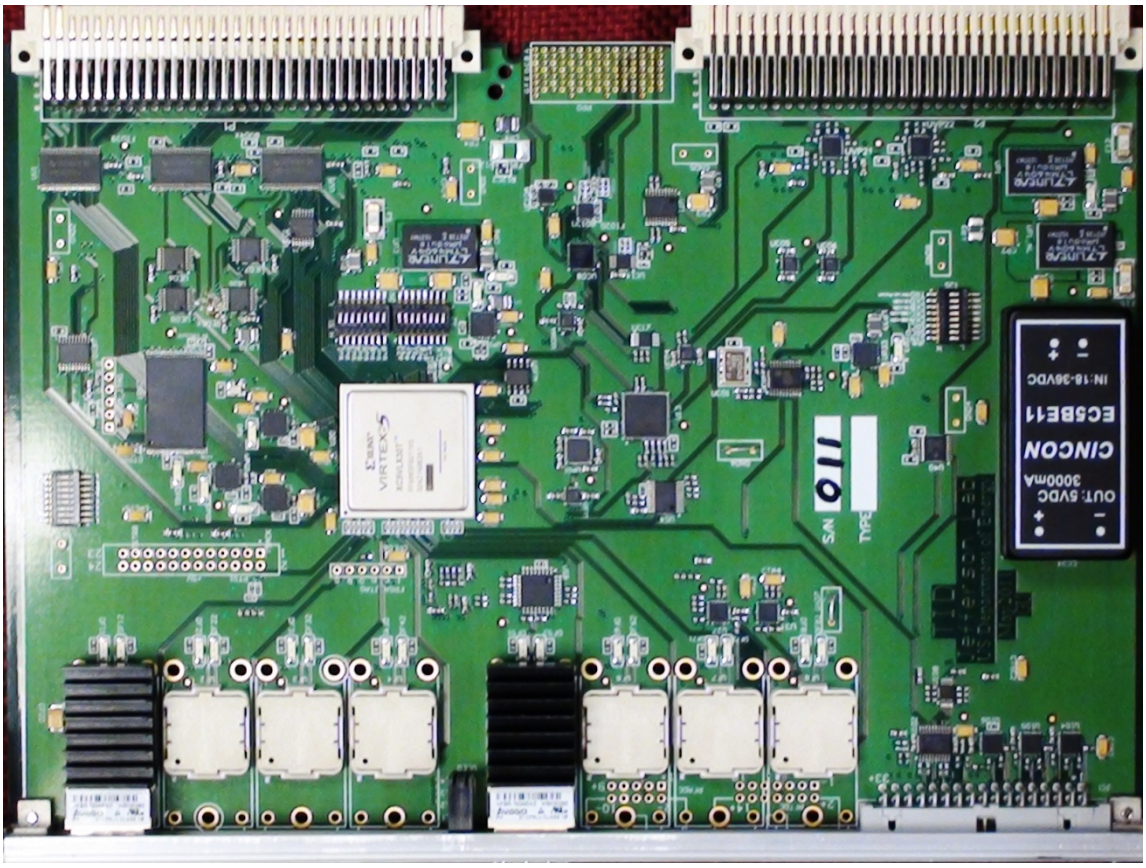

Figure 8 Trigger Interface card. The TI shares the same PCB design as TD, but the components are populated differently from the TD.

In addition to its basic functions, the TI has to be flexible enough to setup a small system for system commissioning without the TS. The shared PCB design makes this possible.

2) TI Design

The Avago's HFBR-7924 four channel optical transceiver is used on TI to receive the fiber signals from TD. There are two optical receivers on each TI. One is used for global trigger, while the other could be used for subsystem trigger. By connecting some TI boards to the same subsystem TS, the TI can be grouped together as a subsystem. The figure 9 shows the diagram of the TI functions.

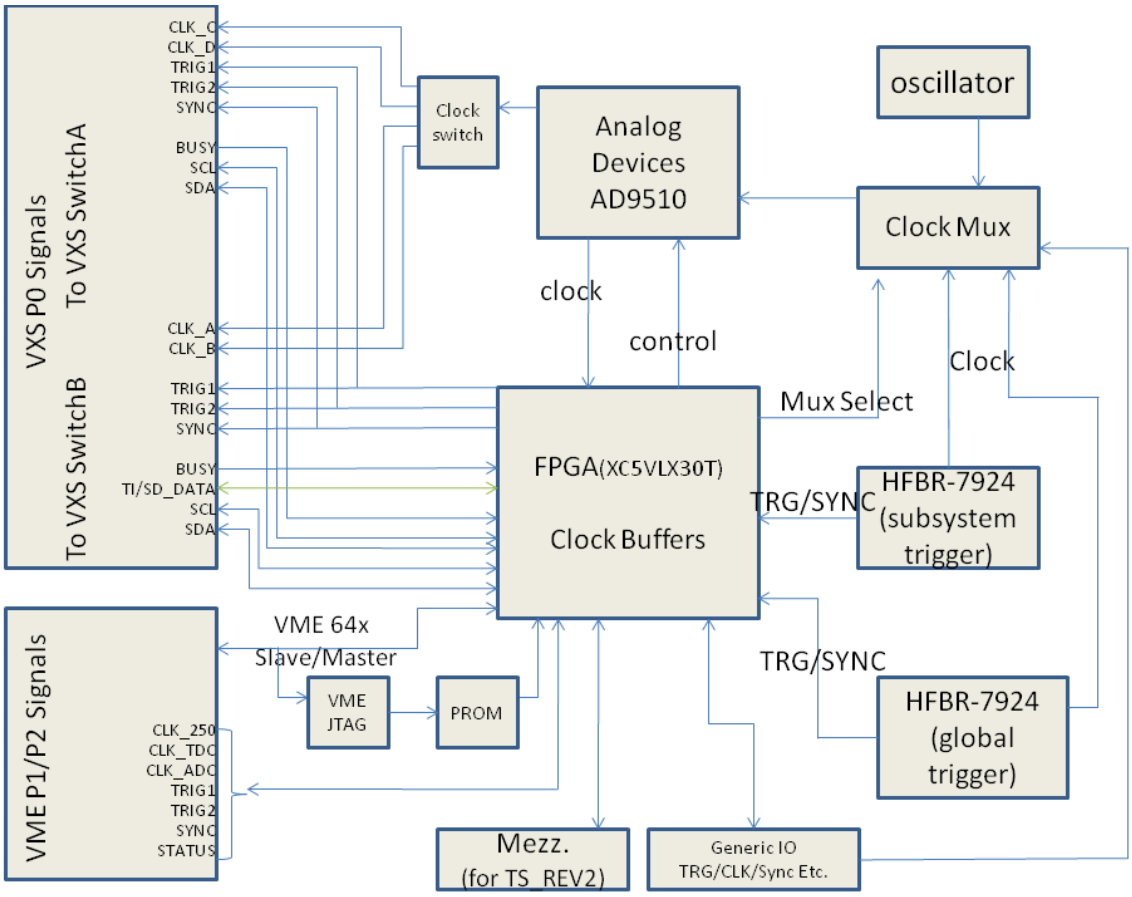

Figure 9 Trigger Interface card functional diagram

Analog Devices' AD9510 is used for clock distribution and lower speed clock generation. SYNC command is used to reset the AD9510 so the AD9510 clock output phase is determined by the timing of SYNC signal. As the SYNC is encoded in phase with the slower clock on the TS, the clock sync command can synchronize the TI slower clock with the TS slower clock. This means that all the slower clocks (derived from the 250MHz main clock) on TI boards are in phase with each other, which is important for the TI to decode the trigger in the 4ns precision and trigger synchronization across different front end crates.

3) TI FPGA and TI Data

One Xilinx XC5VLX30T FPGA is used on the TI board. The FPGA has three main functional blocks: VME interface, Trigger control and event assembly, and Sync control and BUSY monitoring. Each part will be briefly described in the following paragraphs.

The VME interface is responsible for the slow control of the TI and the switch slots boards and the TI data readout. As there is no VME bus access to the switch slot in the VXS crate, a VME to I^2C engine is implemented on the TI for each switch slot. Two VME to JTAG engines are implemented to connect to the FPGA JTAG port and PROM JTAG port. Through the JTAG ports, the board type and firmware versions can

be verified by reading out the chip code and user code. The TI also initiates the front end crate data readout through VME bus. The TI data is readout through VME. The data can be readout in simple single A32D32 VME transfer, block transfer mode, or 2eSST mode.

Using the Xilinx FPGA's built in MGT transceivers, the trigger word is deserialized. The trigger signal and trigger timing information are extracted. The trigger signal is sent out to the front end electronics in the crate using P0 connector and SD board. Meanwhile, the TI can assemble its own event data based on the trigger received. Upon receiving trigger signal, it will initiate ROC readout by either asserting the VME Interrupt Request, or setting a polling register. After the ROC finishes the crate readout, the ROC will acknowledge to the TI that the readout has finished. The TI event data includes the trigger number (or event number), trigger time stamp, and trigger type information. The TI data will be used online for detector event assembly, and event synchronization check.

The third function of the FPGA is the SYNC control and BUSY monitoring. Using the IODELAY of the FPGA, it can automatically align the SYNC signal phase to the 250 MHz main clock. By looping back from the TD, the fiber latency can be measured with a precision of less than 1 ns. The SYNC will be delayed to compensate for the fiber latency, so all the TIs will receive the SYNC command at the same time with the exception of clock skews. The TI will decode the SYNC command. It sends the resets (one of the decoded SYNC commands) to the other modules in the crate through SD via P0 backplane. The TI combines the BUSY from SD, which is the merged BUSY signals from front end modules, and the BUSY status of itself. Together with other TI status, TI sends the BUSY through MGT to the TD through the optical fiber link.

III. TRIGGER CLOCK DISTRIBUTION ISSUES

A. Trigger synchronization

The trigger signal and trigger information (trigger type, trigger timing etc) are serialized from the TS, the serialized trigger is fanned out by the SD and TD and deserialized by the TI. The latency (between TS and TI) is different for different TI boards, as the fiber lengths are different and the deserializer has different latency too. The TI needs be synchronized, so all the TI boards send the trigger at the same time to the front end data acquisition board. In this way, it can be sure that the data from different electronics are from the same physics event. The trigger synchronization is the process to make sure that all the TI boards send the trigger out to the front end modules at the same time.

To synchronize the trigger signals, both the fibre latency and the deserialzer latency need be compensated. Figure 11 shows the diagram of compensated trigger distribution.

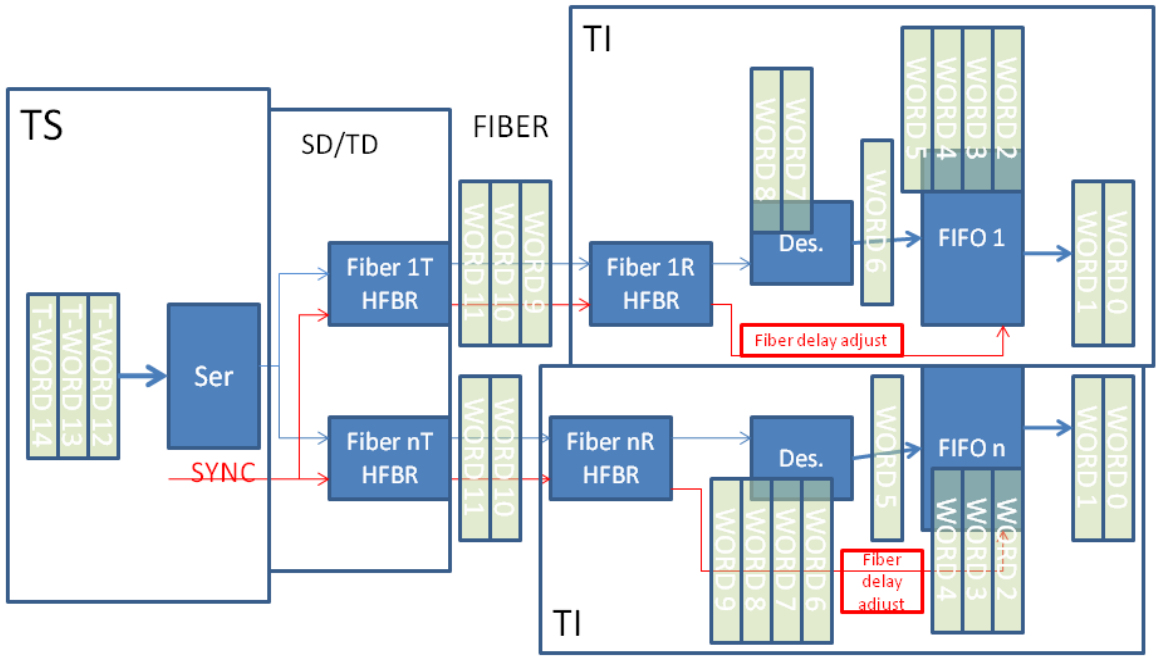

Figure 10 Trigger synchronization between TIs

The fixed latency SYNC signal is delayed on the TI to compensate for the fiber propagation delay, that is the TI with longer fiber will have a shorter delay on the TI. The SYNC signal is automatically synchronized to the global 250MHz clock. The synchronized SYNC signals are used to synchronize the triggers as described in the above figure. Each function in the trigger synchronization will be briefly described next.

1) Trigger serializer/deserializer

The trigger signal and trigger information (trigger type, trigger timing etc) are serialized at TS and deserialized at TI using the Xilinx virtex-5 FPGA MGT modules. As the TS and TI are using the same base 250MHz clock, the elastic buffers inside the MGT are not necessary, so the serializer/deserializer latency can be kept at their minimum. The MGT phase alignment is used to bypass the elastic buffers. The MGT delay on the TS is not a problem for trigger synchronization as it is the sole source.

2) Fiber latency measurement

There are twelve fibres in each bundle. Eight fibres (four pairs) are connected to the optical transceivers (Avago HFBR7924), while the other four are not used. Out of the four pairs, one pair is used for trigger and status, one pair is used for clock, and one pair is used for SYNC signal. The forth pair is used to measure the fiber latency. When measuring the latency, the TI sends a test signal to the TD through one of the pair, the TD

receives the test signal, and loop back to the TI through the other fibre of the pair. The TI measures the delay between the test pulse and the looped back test pulse using the FPGA counter and the carry chain[5,delay measurement]. As the fibre skew is pretty small, this measurement result can be used as the latency for the fibre that carries the SYNC signals.

3) Sync latency compensation

The test pulse loop back time is twice the fibre latency. This measurement result can be saved in the TI, and used to automatically compensate for the SYNC delay in steps of the 250 MHz clock period. Using the Xilinx FPGA IODELAY feature, the SYNC can be automatically phase aligned to the system clock.

4) Trigger latency compensation

If the clock phase is not adjusted, there will be a maximum of 4ns skew among the clocks on the TI boards. This phase can be adjusted by SD if the skew is critical to the system. As the trigger and sync are phase aligned with the clock, there will be a maximum of 4ns phase differences for the trigger signals among TI boards if the clock phase is not adjusted.

B. Clock distribution performance

1) Same clock for the whole system

The TS supply the clock source for the whole system. The slower clocks are derived from the TS fanned out clock. Figure 12 shows the clock jitters as received by the front end electronics distributed by the SD boards on the front end crate. This shows that the system has a very high quality clock, that is, the front end electronics receives a clock of jitter of about 1ps.

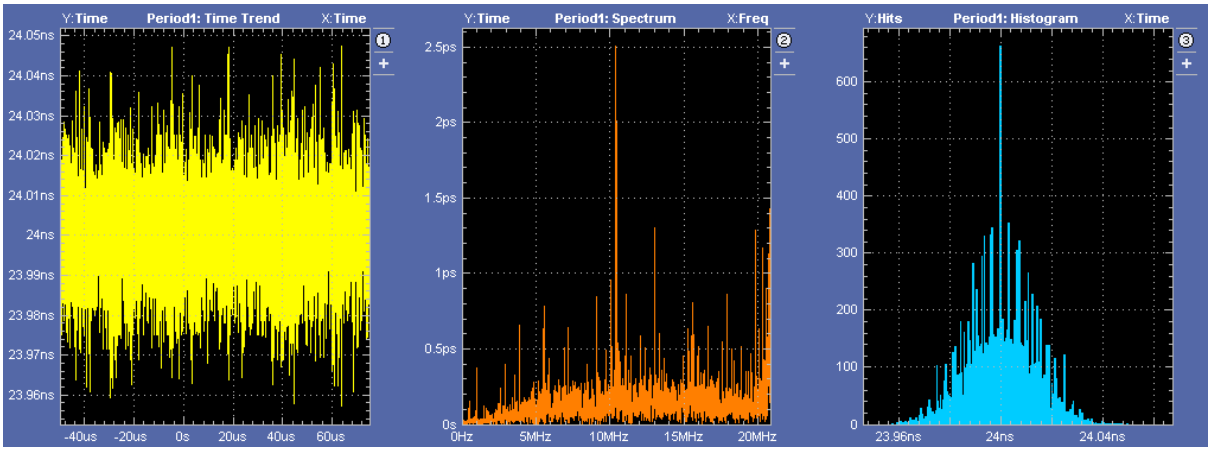

Figure 11 Distributed clock jitters as seen on front end crate. 2ps before SD clean up, and 1 ps after SD clean up

C. DAQ synchronization (trigger throttling)

1) Why we need this

Because of the finite memory size and the randomness of the trigger, it is possible that the memory get over welcomed somewhere in the DAQ system, which could cause problems in the system. The trigger distribution throttling mechanism is used to prevent the possible memory overflows, and to keep the DAQ synchronized. Figure 13 shows the DAQ synchronization logic implemented. Each of the components will be described in the following sections in detail.

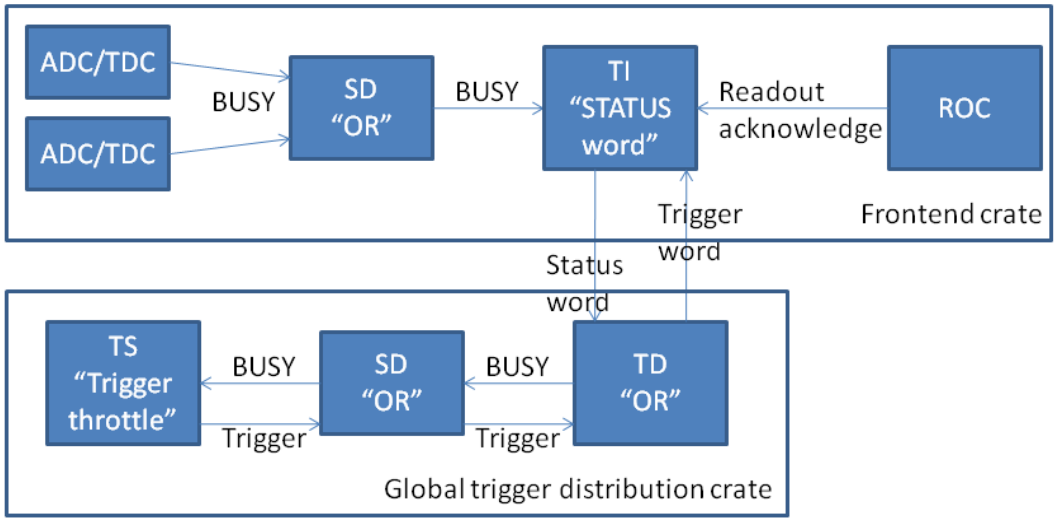

Figure 12 DAQ synchronization

2) Busy signals

The BUSY signals are the primary feedback for the DAQ synchronization. The front end DAQ electronics receives the trigger signal, and find the matching data and store the data in the memory to be readout later. The DAQ is synchronized on the trigger, that is, each trigger is one physical event. If the front end electronics memory is full (or close to full), it will assert the BUSY signal to inform the trigger distribution system that possible DAQ out of sync could occur if more triggers come. This BUSY signal from front end board can be accumulated on the SD, and send back to TI. The TI sends the BUSY signal back to the TD through fibers. The TD will accumulate the BUSY from TI boards, and send to the SD in global trigger distribution crate. The SD in the distribution crate accumulates the BUSY from TD boards, and send to the TS. When TS receives the BUSY, it will throttle the trigger to prevent the memory overflow in the front end electronics. After data

readout in the front end, the BUSY will abate. After the BUSY disserted on the TS, TS will resume trigger again. The TS will record the BUSY time, as efficiency monitoring.

3) Event limit setting

In addition to the BUSY feedback, the system can set a limit on the trigger buffered at the front end. This is achieved by the trigger acknowledge and readout acknowledge by the TI boards.

After the trigger (event) is readout, the Read Out Controller (ROC) will set an acknowledge signal to the TI to indicate that one event is read. The TI sends this acknowledge signal back to the TD through the same fiber for the BUSY, which is encoded and serialized. The TD keeps track of the number of trigger sent to the TI, and the number of trigger acknowledged by the TI. If the difference is over a preset limit, this means that there are a certain number of triggeres are buffered on the front end DAQ electronics, the TD will assert the BUSY. Through the SD, the TS receives the BUSY, and the TS will throttles the trigger and disable further trigger fan out. After front end readout and trigger acknowledge, the difference will re-treat, and the BUSY will abate on the TD. After TS senses the desertion of BUSY from TD, it will fan out the trigger again. The TS record the BUSY time the same way as the BUSY asserted by the front end electronics. If the preset limit is 1, this is the event locking mode. That is no second trigger is sent out before the first trigger is readout. If the preset number is infinite (in practice, a very large number), the DAQ will be working at pipeline mode with trigger throttling by the front end electronics BUSY only.

If event blocking is used, that is, a preset number of triggers is treated as a block in the DAQ readout, the ROC will acknowledge on the block based readout, not individual trigger. In this case, the TD will count the number of blocks sent to the TI, and the number of blocks acknowledged by the TI. The TD will set the BUSY if the difference is over the preset number. If the number of the trigger per block is set to 1, each block is one trigger. This special case is the same as that mentioned in the previous paragraph.

4) Sync event (special event)

The TS can distribute a special trigger, SYNCEVENT. After fanning out this event, the TS will be in a waiting mode, and inhibits further triggers. Upon receiving this trigger, the TI will inform the ROC in the crate of the special event, and set the BUSY status. The BUSY will propagate back to the TS to reset the TS inhibit. As the BUSY is set, there is still no further trigger. After the normal front end crate readout, the ROC will dump all the front end modules memory buffers, and make sure that all the data buffers are empty, and ready for further triggers. Then the ROC will set an acknowledge signal to the TI to indicate that the front end crate is

ready for triggers. The TI will negate the BUSY. After all the BUSY are abated from TIs, the TS will fan out triggers again. The SYNC event is a pre-emptive action for DAQ synchronization.

D. Subdetector partitioning

1) Partitioning using the TS trigger type

(leave to Ed.) By encoding a special code on the TS, the TI will selectively decode the triggers. Different TI boards can decode and fan out triggers differently. This requires different firmware or firmware setting on each TI, but should not be hard to implement provided that the TS (and the software) is capable to deal with multiple requests, especially during system commissioning.

2) Partitioning using the Subsystem trigger supervisor

The shared TI and TD PCB board can be configured and firmware programmed as a subsystem supervisor board. It behaves like a trigger supervisor with optical fiber fanout like a TD. Each subsystem trigger supervisor board can drive up to eight TI boards. These eight TI boards are grouped as a sub-system. The TI uses the HFBR#5 as subsystem trigger input and SYNC input. As the whole system is working on the same clock, there is no need to use a sub-system clock. The sub-system partition can co-exist with the global system.

E. Subsystem commissioning

Because of the flexibility of the TI/TD PCB design, the PCB can be configured as any combination of the TI, TD and TS functionalities. This is very useful in subdetector testing and commissioning. Figure 14 is a sample configure diagram for nine crate testing/commissioning.

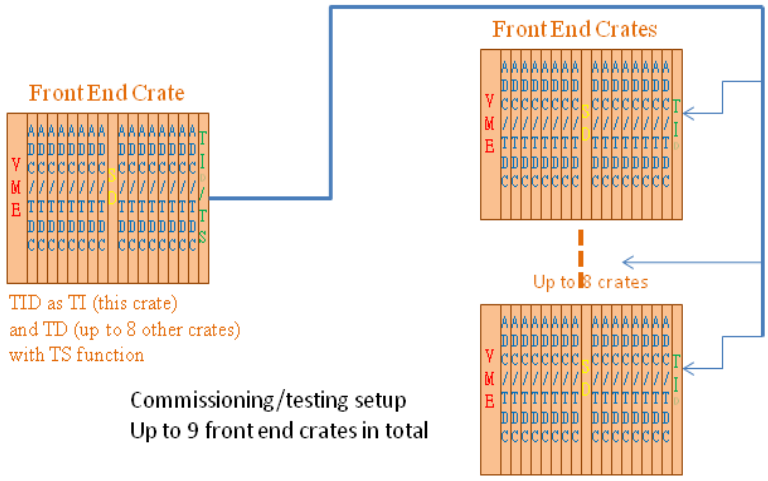

Figure 13 Subsystem testing/commissioning for up to nine Front End Crates

The First crates has the PCB configured as a multi-purpose boards, which we call it TIMaster. The TIMaster receives external triggers (either front panel inputs, or VME generated triggers) and generate triggers for the set up. It generates the system clock (250MHz) by either the on-board oscillator or an external clock inputs. It generates the SYNC commands from the VME controls. It sends out the trigger/clock/SYNC signals like a TI through the P0 backplane to the crate, and it sends out trigger/clock/SYNC signals to another eight TIs like a TD. The BUSY signals are merged by the TIMaster, and used to inhibit the triggers to control the DAQ flow. The ROC readout acknowledges are also collected by the TIMaster to control the DAQ process. The other eight crates are standard front end crates with TI board in standard configurations.

A system with one TIMaster front end crate and one standard TI front end crates are tested in the lab, and running for more than six months.

IV. Status

A. *Prototype System Integration*

A prototype of the trigger and clock distribution system was setup and tested. The distribution system works. Figure 15 is a picture of the test setup.

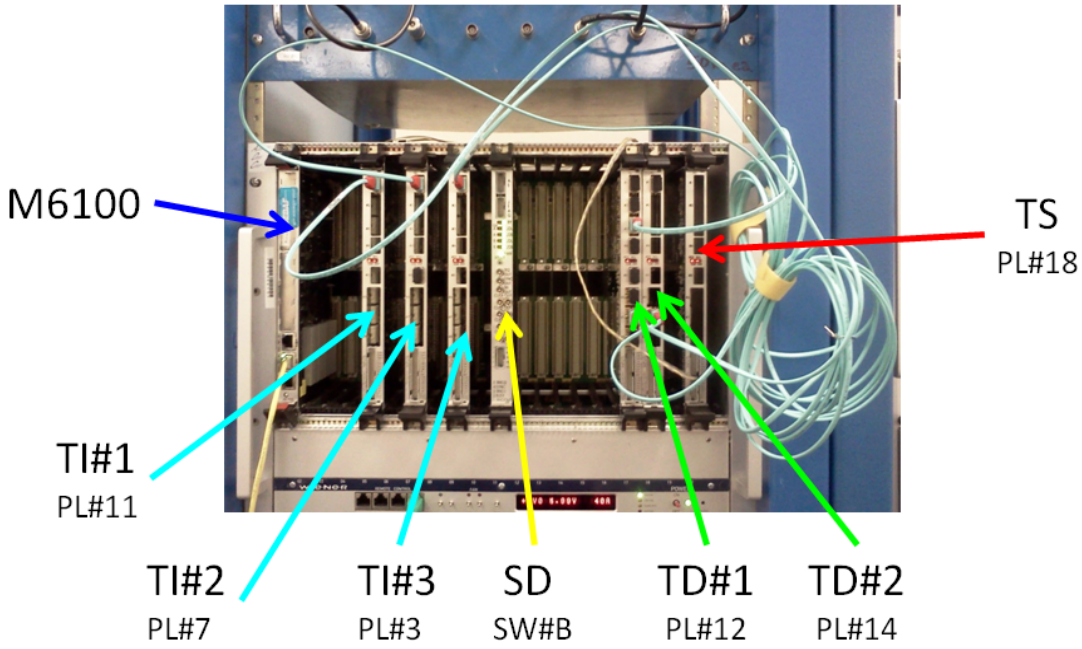

Figure 14 Setup for the trigger and clock distribution

In this setup, one prototype TS (the TID programmed as a TS) board, three preproduction TI boards, two preproduction TD, one preproduction SD and one production VXS crate are used. The TS sends trigger and

clock to the SD, and the SD fanout them to the TDs in the distribution crate. Three fibers connect two TDs to the three TI boards in the same crate. The drivers for TI board P0 connector are disabled, so the TI can be plugged in the same crate without signal conflict. This setup can represent the full trigger/clock distribution system. There should not be any problem to use 16 TDs if two TDs are fine, and there should be new problems for the TD to fan out to eight TIs.

The TI boards are synchronized. The trigger and clock distribution are synchronized. The trigger throttling is working. The prototype setup is stable. We do not expect any problem for the full trigger/clock distribution system.

B. Hardware status

The TI, TD, and SD preproduction boards are fully tested, and the production will be finished by early 2012. The TS prototype is fully tested, and satisfies the design requirement. The production will be finished by early 2013. There will be no preproduction stage for the TS as the small quantity required in the system. The full system will be installed in 2013 in the experimental halls, and will be ready for 12 GeV upgrade experiments by 2015.

The trigger and clock distribution scheme is initiated by the HallD experiment, but the use of the distribution scheme is not limited to that Hall. The scheme can be used in other three CEBAF experiments, and even beyond CFBAF experiments.

V. REFERENCES

[1] GLUEX collaboration, the gluex experiment

[2] CEBAF references

[3] Trigger Supervisor, technical note

[4] Trigger Distribution board, technical note

[5] Trigger Interface board, technical note

[6] Signal Distribution board, technical note

[7] VXS crate, and VXS specification

[8] Cuvas etal, trigger system description

[9] Heyes etal, DAQ system description

VI. GLOSSARY

ADC: Analogous to Digital Converter.

TDC: Time to Digital Converter.

VME: Versa Module European. ANSI/IEEE 1014-1987

VXS: VME switched Serial. VITA41.0

TI: Trigger Interface

TD: Trigger Distribution

TS: Trigger Supervisor

SD: Signal Distribution

GTP: Global Trigger Processor

CTP: Crate Trigger Processor

ROC: ReadOut Controller

DAQ: Data Acquisition

GLUEX: Gluon Excite experiment

FPGA: Field Programmable Gate Array

PROM: Programmable Read Only Memory

LVPECL: Low Voltage Positive Emmission Coupling Logic signals

LVDS: Low Voltage Differential Signals

MGT: Multiple Gigibit Transceiver

MHz: Million Hertz

ns: Nano-second, or one billionth of a second

ps: Pico-second, or one trillionth of a second

Mbps: Million bits per second

VII. FIGURE CAPTIONS