



Nuclear Physics Division
Data Acquisition Group

Description and Technical Information for the VME Trigger Distribution (TD) Module

J. William Gu (jgu@jlab.org)

June 14, 2016

Table of Contents

Section	Title	Page
1	Introduction	3
2	Purpose of TID Module	4
3	Function Description	4
4	Specifications	7
5	TID operation	9
6	Programming Requirements	10
7	VXS P0 and VME P2 Row-C Pin outs	17
8	Examples of individual test	17
9	Software setup for TID	18
10	Citation	18
Appendix A	Schematics	20
Appendix B	Fabrication Drawing	38
Appendix C	Bill of Materials	41
Appendix D	Glossory	47
Appendix E	TID data format	48
Appendix F	Revision history	49

1 Introduction

The Trigger Interface Distribution (TD) module is being designed for the Jefferson Lab 12GeV upgrade, mainly for HallD[(Collaboration G. , 2009)] and HallB[(Collaboration C. , 2009)], with other experimental Halls [(experiments, 1990)] compatibility. This module is responsible for fanning out a low-jitter system clock, fixed latency trigger signals, and fixed latency SYNC signals to the Trigger Interface (TI) modules for the Front-end data acquisition crates through optic fibers. The modules also merge the front-end data acquisition crate status and generate a BUSY signal to request the Trigger Supervisor (TS) to pause the trigger. Figure 1a shows the placement of the TD modules in the global trigger distribution scheme in experiment setup. Figure 1b shows the crate level diagram

Figure 1a:

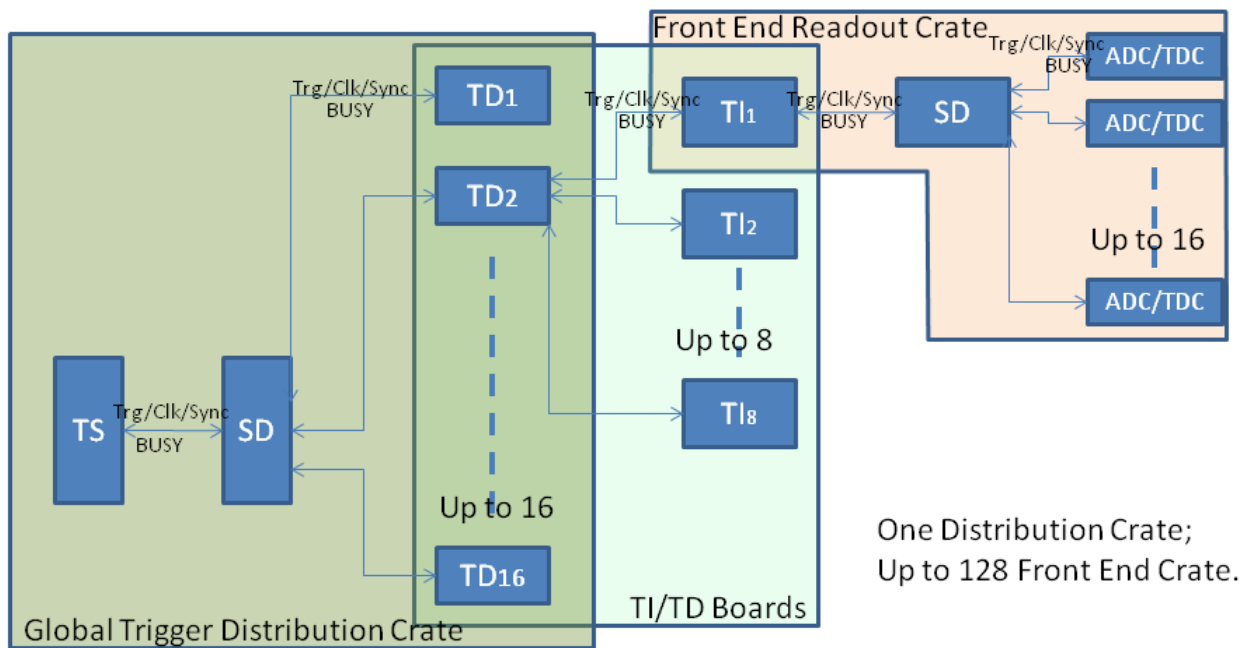
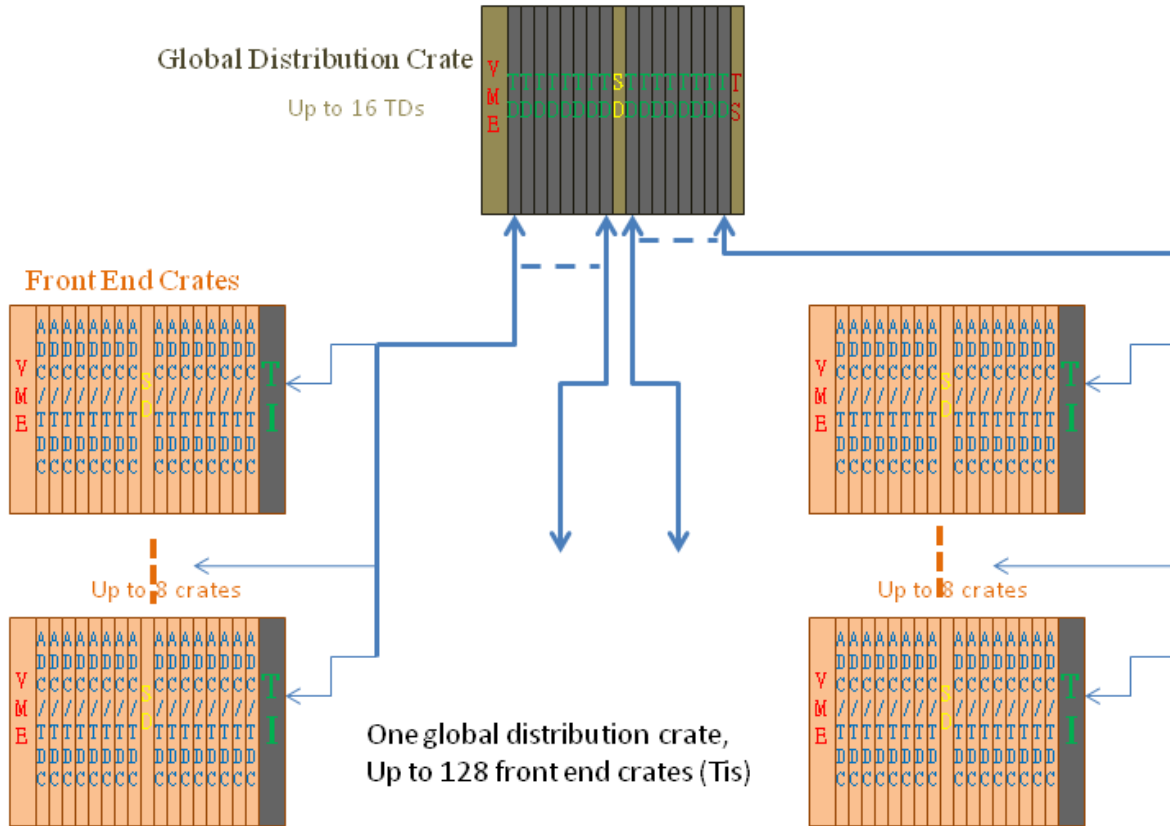


Figure 1b:



The TD modules sit in the Global Trigger/Clock Distribution Crate [(Chris, Hall_D trigger layout, 2009)] to fan out trigger/Clock/Sync to the front-end crates.

2 Purpose of the module

The TD module receives trigger/clock/Sync signals from the SD and fans out the signals for up to eight crates in the front-end data acquisition system. The global trigger distribution crate is designed to house up to 16 TD modules, which provides trigger/Clock/Sync for up to 128 crates. The TD distributes the following signals to each front-end crates: global system clock, trigger words, and Sync, a custom serial link to establish a fixed latency from the trigger Supervisor to front end crates. In addition, the TD will receive status information from each crate that will be used to generate a ‘busy’ signal and also track various status registers of the front-end crates.

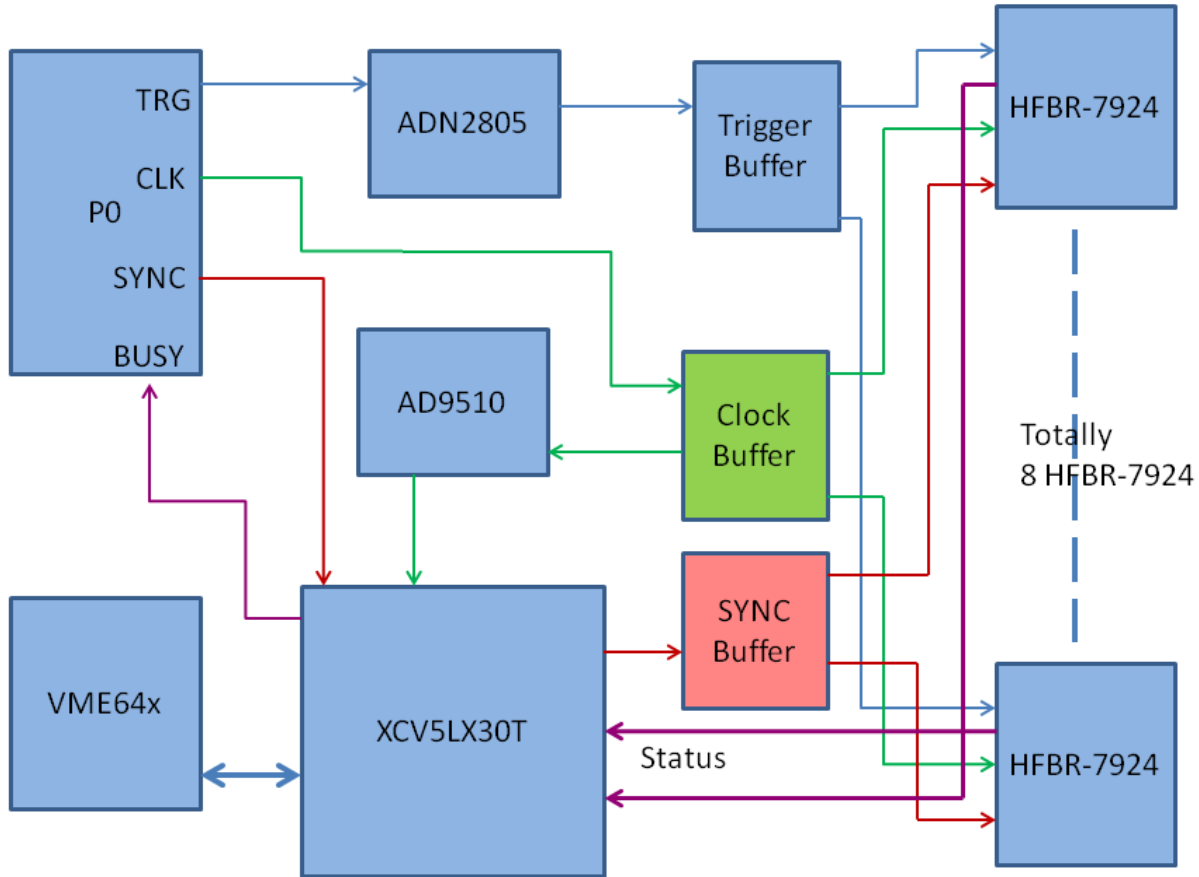
3 Functional Descriptions

3.1 General description

Figure 2 shows the block diagram of the TD module, indicating the major components used in the design. The HFBR-7924 is the multi-channel (4 Rx, 4 Tx) fiber link that the TD fans out a low-jitter (<3ps RMS) 250MHz global pipeline clock, serialized 16bit trigger words, and a fixed latency sync signal used in producing a fixed latency trigger. The AD9510 is the main clock driver and gets synchronized lower frequency clocks. The Xilinx XC5VLX30T is used to encode/decode the SYNC data, to interface with the VME, to monitor (combine)

the front end crates status. The P0 is compatible with the VXS payload slots, which matches with SD positioned in switch slots.

Figure 2: Trigger Distribution board Block Diagram



3.2 Fiber links

The HFBR-7924 is the multi-channel (4 Rx, 4 Tx) fiber optic link for the TD. All the eight HFBR-7924 transceivers will be installed, so each can support up to eight front-end data acquisition crates. The HFBR_7924 is chosen over the HFBR-7934, because the HFBR-7924 is about \$100 cheaper per piece, and there is no visible performance degradation comparing with HFBR-7934. [GU, 2010].

The first pair (Tx/Rx) is used to transfer trigger words from TD to TI, and status from TI to TD. The second pair is used to transmit the 250MHz clock from TD to TI. The third pair is used to transmit the SYNC from TD to TI. The TI to TD links on second pair and third pair are not used. The fourth pair (Tx/Rx) is looped back on the TD for fiber length (latency) measurement.

3.3: Clock Distribution

To minimize the added jitter on the clock, the clock from P0 are directly buffered and driven to the optic transceivers. One of the buffer output was sent to the AD9510, and supply the on-board clock.

3.4 Trigger distribution:

The Serialized (by TS) trigger word was re-sampled by ADN2805, a 1.25 Gbps Clock and Data Recovery IC. The re-sampled data was fanned out to the optic transceivers. The TD does not decode the serialized trigger word.

There are two ways for the TD to get the trigger signal. The first is to use the VME P2 connector. In this case, a twisted pair cable is connected from the TS backplane IO card to the TD P2 connector. The second is to use the 'trigger2' line on the P0 connector. The TS sends the trigger pulse to P0 'Trigger2' line, and the TD receives the 'TRIGGER2' via SD fan out.

3.5: Fixed Latency SYNC

The SYNC signal is a 250Mbps serial line operating in synchronous mode. This serial link allows a 4bit command to be sent at chosen 4ns points in time. SYNC is synchronized to the master clock CLK250 and is sampled every 4ns cycle. The line is considered to be idle when more than 4 samples in a row are read '1'. A command is sent between idle times by sending first a '0' followed by the 4bits that comprise the command, LSB first. After the command has been sent a final '1' is sent so that the line will return back to the IDLE state. The encoding portion of this serial protocol is performed on the TS. The encoded SYNC signal is first received by the FPGA after phase alignment. The SYNC is decoded in the FPGA. One of the decoded SYNC is re-encoded, and sent to a buffer/fanout to all the eight optic transceivers. The decoded SYNC is further decoded in the FPGA for use on TD itself.

3.6 VME interface

The TD is a VXS payload slot board. It is compatible with VME64x backplane. Normally, it is a VME slave board, with interrupt capability.

The TD can also be a master VME board. It supports single level bus request (BR3, level 3) only, as we do not expect many boards to be a VME master in the crate.

For simplicity, three kinds of VME address modifier codes are implemented. (1), User defined address modifier. (0x19, 0x1A, 0x1C and 0x1D) This is similar to the A24 address modifier. It is used to load the PROM by the emergency logic. (2), Standard A24 address modifier. This is used to readout the registers on the FPGA, slow controls of the TID peripherals, and to request data from other boards in the crate when in master mode. (3), A32 BLT data transfer. This is used to transfer data to the ROC (Read Out Controller). This is implemented the same as other ADC/TDC board, so the ROC needs only one read to get all the front end boards' data out for higher efficiency.

3.7: The Xilinx PROM programming.

The Xilinx XCF32P PROM is used to program the FPGA. It can save two different versions of the FPGA (XC5VLX30T) firmware when used in non-compression mode. It can save four different versions of the firmware when bit stream compression is used, in which case, only the slave serial and slave SelectMAP modes are supported. The PROM is programmed using VME with emergency logic decoding. It can be addressed in the VME64x crates by its geographical address. If it is in the crate without geographical address, only one TID in the crate should be addressed as geographical slot#0. To avoid conflict with other VME addressing, the user-defined address modifiers are used for the PROM loading. The emergency logic supports A24 user defined address modifier codes: 0x19, 0x1A, 0x1D and 0x1E (Similar to 0x39, 0x3A, 0x3D and 0x3E). Out of the data, bit[1] is used for TDI, bit[0] is used for TMS, and all the other bits are unused. This approach is fully tested in CMS on LHC. The emergency loading is tested. With M6100 controller, the 32 Mbit PROM (XC32P) can be loaded in less than five minutes. The emergency loading provides VME remote firmware re-loading and broadcast firmware loading even if the FPGA is not working. One 33 MHz (25MHz on earlier revision of TID) on-board oscillator is used to program the FPGA in slave mode, and used by the FPGA for slow control, for example, the VME to AD9510 serial control engine.

The PROM can also be programmed by the on-board JTAG connector and VME-JTAG engine (after the FPGA is programmed and working) in the FPGA. The JTAG engine in the FPGA provides VME remote firmware loading when the FPGA is working with more efficient VME data transfer (32 bits versus 1 bit).

3.8: Status passing

The TD can merge the status together and pass on to SD then to TS. Specifically, the TD receives the status from eight TI boards. There are three ways that the TD monitor the TI (or front end crate) status:

First, the TD extracts the TI busy information, and do a logical OR as the overall BUSY;

Second, the TD extracts the trigger acknowledge, and compare with the number of the trigger pulse it sends to the TI to check for missing triggers. If the trigger is missing, the TD will raise a BUSY flag too.

Third, the TD extract the TI read out acknowledge, and compare with the number of data blocks the trigger generates. This can be used to indicate the data buffer level on the front end electronics. If the buffer level is too high, the TD can assert BUSY, and stop further trigger going down to TI, hence prevent the front end electronics data buffer overflow.

3.9: Serial data communication with SD

The TD can send data to the SD via a 250Mbps link, (it is possible to increase it to 500 Mbps using DDR techniques). This is implemented using the Xilinx SelectIO standard differential IO pin pair. In this case, the SD can be implemented as a data concentrator card to collect data from the all the TD boards in the crate. This is another data readout path in addition to the standard VME readout. The maximum data rate is 50 MB/sec per slot. The full crate can reach up to 900 MB/sec assuming all 18 payload slots are used.

The SD can also send data, or simply another pulse to TD using this link. The direction of the data link depends on the firmware (TD and SD) implementation.

4. Specification Sheet

4.1 Mechanical

- Single width VITA 41 Payload Module. It is positioned in the PP01 to PP16 in global clock/trigger distribution crate

4.2 High speed serial P0 and P2 inputs:

- Trigger pulse from TS via P0;
- BUSY ECL signals on P2 used as trigger pulse from TS;
- Clock, trigger and sync signals from SD

4.3 High speed serial P0 and P2 outputs:

- BUSY to SD on P0
- 250/500 Mbps data (LVDS) to SD at per event basis

4.4 Front panel inputs and outputs:

- Eight HFBR-7924 transceivers for TD in distribution crate.
- 34-pin connector for some generic IO:
 - Pin1/2: Board busy
 - Pin3/4: readout trigger
 - Pin5/6, 7/8, 9/10 and 11/12: FPGA internal debug signals
 - Pin 13/14: SyncResetReqst output to TS (OR of SyncResetReqst from TI)
 - Pin 15/16: Prompt trigger
 - Pin 17/34: trigger inhibit (not implemented yet)

4.5 Fiber channel signals:

- SYNC Fixed Latency Link
 - 250Mbps Serial Communication
 - Manchester Encoded
 - SYNC to CLK skew variation adjusted at FPGA receiver.
- TRIGLINKTX/TRIGLINKRX
 - 1.25Gbps Trigger Word Line
 - Provides 16bit parallel data every 16ns
 - A BUSY status word in the opposite direction.
- CLK
 - 250MHz Clock <3ps RMS Jitter

4.6 Indicators: Front Panel:

- Bit 1 (close to the PCB): FPGA programmed and the clock (DCM locked) is ready;
- Bit 2: VME DTACK, VME activity;
- Bit 3: Trigger_1 is sent out;
- Bit 4: HFBR MGT Rx error;

On board:

- Power OK near each regulator or DC-DC converter;
- FPGA program DONE;
- Fiber optical transmitter FAULT and receiver SIGNAL_DETECTED near each HFBR-7924 module.

4.7 Programming:

- VME to JTAG A24D32 with user defined AM (Address Modifier) for remote loading with redundant On board JTAG connector;
- Custom VME to JTAG engine implemented in the FPGA using A24D32 for firmware loading;
- Up to four revisions of the firmware can be stored in the PROM simultaneously.

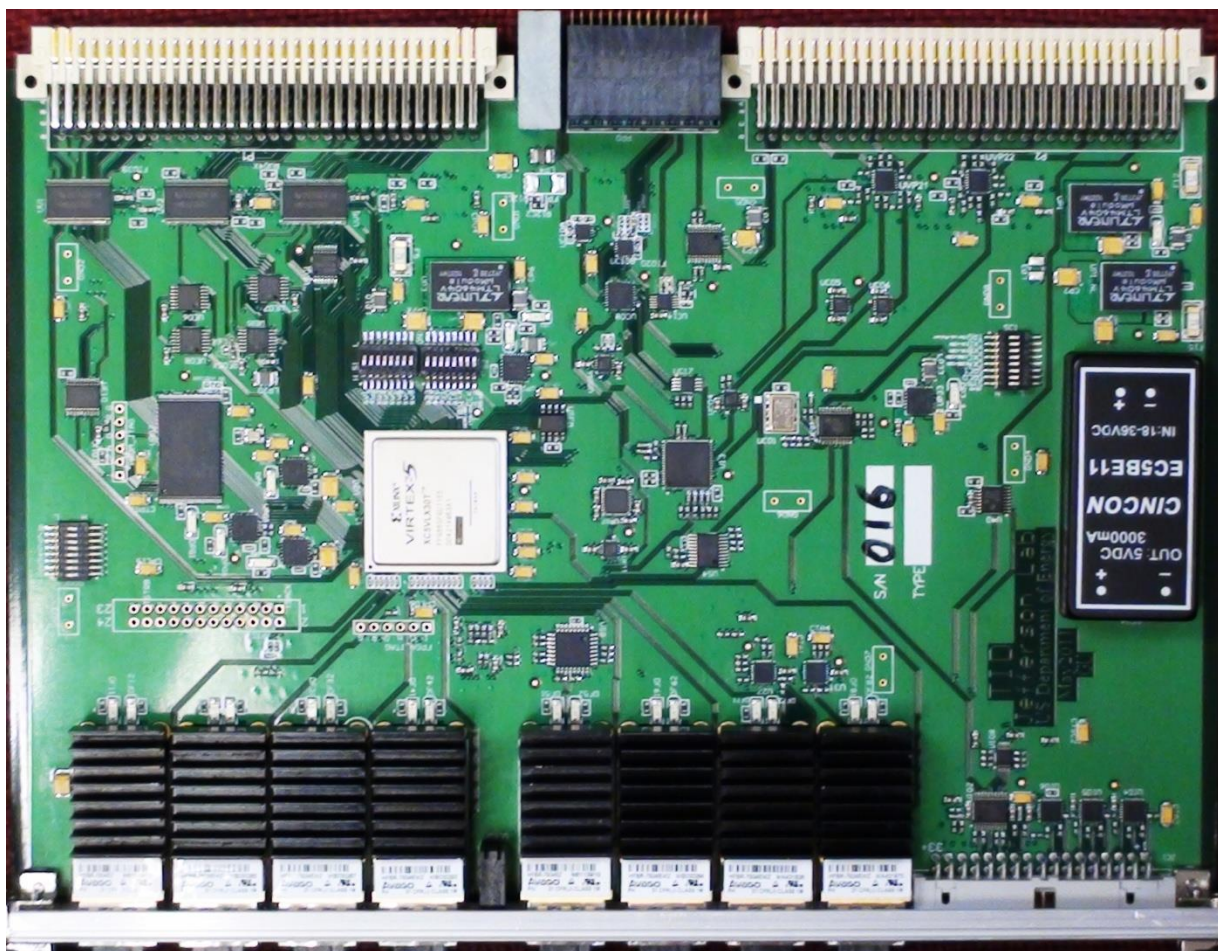
4.8 Power requirements:

- +5v @ 3 Amps; -12V @ 0.25 Amp; +12V @0.25 Amp +3.3V@2A (From Backplane)
- Local regulators for other required voltages: +1.0V, +1.2V, +1.8V, +2.5V, +3.3V, and -5V.

4.9 Environment:

- Forced air cooling: Weiner standard VME64x/VXS
- Commercial grade components (0-75 Celsius)

Figure 3 shows a picture of the TD board:



5 TD operation procedures:

The TD needs be properly set, and plugged into the proper crate and slot. Damage may happen to the TD, the crate, or other PCBs in the crate if the right procedure is not followed.

5.1 TD Power supply:

The TD use +3.3V directly from VME64x crate. It can also generate its own +3.3V supply by a DC-DC converter. Another dedicated +3.3V DC-DC converter can be used to power the optical transceivers (HFBR-7924). The HFBR_7924 can also be powered by the main +3.3V supply for the board. Proper settings are needed to avoid damage to the board or backplane.

If the dedicated +3.3V DC-DC converter is to be used to power the HFBR-7924:

- (1). Make sure that the DC-DC converter LTM4604, UP01, is stuffed.
- (2). Inductor, LP3 is removed.

If the TID main +3.3V power is used to power the HFBR-7924:

- (1). Make sure that either UP1_NL is NOT stuffed,
- (2). Inductor LP3 is stuffed.

If the VME64x crate +3.3V power is used for the TID:

- (1). The fuse, FP1 is stuffed;
- (2). The DC-DC converter UP1 is removed.

If the VME64x crate +3.3V power is not used for the TID:

- (1). The fuse, FP1 is removed;

(2). The UP1 is stuffed.

5.2 Hardware setting (Switch etc.):

The TD receives signals from P0 connector, and fan out to the optic transceivers. There are four 8-bit switches on the TID, and marked as: S1, S2 (VME address space setting switches), SC01 (TID mode setting) and SC1 (TID clock setting). Some switches are LVTTTL, some are LVPECL. When the switch is ON, the switch is LOW, (0V for LVTTTL, and 1.4V for LVPECL); when the switch is OFF, the switch is HIGH, (3.3V for LVTTTL, and 2.5V for LVPECL). Here are the details of the switch setting:

5.2.1. SC1 setting:

- Bit1: LVPECL, open=high, trigger_1 source selection. When low, the trigger_1 source is FPGA MGT_112 output (serialized trigger data); when high, the trigger_1 source is standard FPGA differential output (pulse);
- Bit8: LVPECL, open=high, TID connectors' sync signal source selection. When low, Sync_reset is selected; when high, Manchester encoded SYNC signal is selected.

5.2.2 SC01 setting:

- Bit[2:1]: LVTTTL, open=high. Firmware revision selection. When Bit2=0&Bit1=0, select firmware Rev0; when Bit2=0&Bit1=1, select firmware Rev1; when Bit2=1&Bit1=0, select firmware Rev2; when Bit2=1&Bit1=1, select firmware Rev3. If the program bits are not compressed, the PROM XCV32P can only fit two revisions of the firmware.

5.2.3 S1 setting:

- Bit[1:3]: These three bits are used to control the OUTPUT(5:2) of the front panel 34-pin connector. The switches are used to multiplex the eight FPGA internal monitoring sources (32 signals) on the four output pins.
- Bit[4]: Add an extra word if the total number of words in a block is odd. '1' to enable, '0' to disable;
- Bit[8]: keep high, for TID_rev1, this pin is used as IACK input to the FPGA;
- Bit[8:7]: keep high, for TID_rev2, these two pins are used as clock source selection output from the FPGA;
- Bit[5:6]: not used.

5.2.4 S2 setting:

- Bit[1:5]=A[23:19], VME address space in A32 or A24 mode. Be careful about the bit order. When in VME64x crate, these addresses should be set the same as its geographical address.
- Bit6: LVPECL, open=high. The HFBR#1, #2, #3 and #4 trigger source selection. When low, the source is P0 (from SD), when high, the source is FPGA GTP_116.
- Bit7: LVPECL, open=high. The HFBR#1_8 fan out clock source selection. When low, the fan out source is P0 (from SD), when high, the source is on-board clock manager AD9510. This should be consistent with the bit(4:3) of SC01 switch setting.
- Bit8: LVPECL, open=high. The HFBR#5, #6, #7 and #8 trigger source selection. When low, the source is P0 (from SD), when high, the source is FPGA GTP_114.

5.3 Software setting:

After the board is properly set, and plugged in the right slot, some software setting needs be applied for the board to work. Some parts of the board needs be powered down to reduce the power consumption. The FPGA GTP transceivers will be automatically powered depending on the mode setting (TI/TD).

6. VME Programming Requirements (This part will be updated as the firmware develops)

There are three categories of Address Modifier codes are supported on the TID: the user-defined codes (A24) for emergency firmware loading; Standard A24 for FPGA register read/write and slow control; A32 block transfer for VME data readout.

6.1 VME to JTAG emergency loading:

The AM[5:0] user defined codes are used for this logic. This works even before the FPGA is programmed and working. It is almost the same as A24D32 mode. The valid AM codes are: 0x19, 0x1A, 0x1D and 0x1E. These AM codes are user defined, and similar to the AM codes 0x39, 0x3A, 0x3D and 0x3E.

The valid address bits are A[31:24] do not care; A[23:19]=GA[4:0] for VME64x crates, or A[23:19]=0 for non-VME64x crates; A[18:2]=b'0001111111111111.

Data bit[1] is TDI; data bit[0] is TMS.

For example, if the board is in slot#5 (that is $\sim GA(4:0) = 11010$), you need write to A(23:0)=0x28fffc. If data(1:0)=00, both TMS and TDI will be low; if data(1:0)=01, TMS is high, TDI is low; if data(1:0)=10, TMS is low, TDI is high; if data(1:0)=11, both TDI and TMS are high. The normal A24 address should try to avoid this address (0x0fffc).

A more advanced example: Instruction register shift (8-bit, shift in 0x5a) starting from/end up at the 'reset idle' mode: 14 consecutive writes to the address 0x28fffc with AM=0x19, 1a, 1d or 1e, the data are 1, 1, 0, 0, 0, 2, 0, 2, 2, 0, 2, 1, 1, 0 respectively.

Data	1	1	0	0	0	2	0	2	2	0	2	1	1	0
TMS	H	H	L	L	L	L	L	L	L	L	L	H	H	L
TDI	0x	0x	0x	0x	0	1	0	1	1	0	1	0	0x	0x

- “TMS H” means logic High, “TMS L” means logic Low, “TDI 0” means 0 or Low, “TDI 1” means 1 or High, and “TDI 0x” means DO NOT CARE by the JTAG, but the set value is 0.

6.2 Configuration Registers:

A24D32 are used for register read/write. Similar to the emergency loading logic, the base address is determined by the Geographic Address in VME64x crate, and external switch for non-VME64x crate. That is, A[23:19]=GA[4:0], or SW[5:1].

➤ Address offset: 0x00000: Board ID:

Bit 7-0 (R/W): Crate ID; Reset default 0x00;

Bit 12-8 (R): A24 address, higher 5 bits; Reset default 000

Bit 13 (R): ‘1’: TD is in running mode, it is GA parity bit for TI;

Bit 15-14 (R): ‘10’: TD is in running mode (no more register changes), others: TD not in running mode;

Bit 23-16 (R): Board revision, 00: prototype, 01: production

Bit 31-24 (R): Board type, 0x71: TI, 0x75: TS, 0x7D: TD.

➤ Address offset: 0x00004: Optic transceiver enable:

Bit 7-0 (R/W): on TI: HFBR#8, #7, ... #1 Enable, Reset default 0xFF all enabled.

Bit 0: ‘1’ enable HFBR#1, ‘0’ disable HFBR#1; (‘disable’ means ‘power down’)

Bit 1: ‘1’ enable HFBR#2, ‘0’ disable HFBR#2;

Bit 2: ‘1’ enable HFBR#3, ‘0’ disable HFBR#3;

Bit 3: '1' enable HFBR#4, '0' disable HFBR#4;
 Bit 4: '1' enable HFBR#5, '0' disable HFBR#5;
 Bit 5: '1' enable HFBR#6, '0' disable HFBR#6;
 Bit 6: '1' enable HFBR#7, '0' disable HFBR#7;
 Bit 7: '1' enable HFBR#8, '0' disable HFBR#8;

Bit 7-0 (R/W): for TD with AFBR-79EIDZ optic transceivers, these bits are used to enable the I2C interface. '0': to enable (select), '1' to disable (by pass).

Bit 8 (R/W): Trig/Sync Output enable on P0, for TI only (not TD)

Bit 23-16 (R): HFBR#8, #7, ... #1 connected to the TI board (TI powered up)

Bit 31-24 (R): HFBR#8, #7, ... #1 connected TI has trigger inputs enabled (trigger sources are set).

➤ Address offset: 0x00008: Interrupt setting:

Bit 7-0 (R/W): Interrupt ID; Reset default 0xC8

Bit 10-8 (R/W): Interrupt level; Reset default 5;

Bit 16 (R/W): IRQ enable. Reset default: 0;

➤ Address offset: 0x0000C: Trigger delay and Pulse width:

Bit 7-0 (R/W): Trigger_1 delay, $(n+1)*4$ ns; Reset default 0x07;

Bit 15-8 (R/W): Trigger_1 Pulse width $(n+1)*4$ ns; Reset default 0x07;

Bit 23-16 (R/W): Trigger_2 delay, $(n+1)*4$ ns; Reset default 0x07;

Bit 31-24 (R/W): Trigger_2 Pulse width $(n+1)*4$ ns. Reset default 0x07;

➤ Address offset: 0x00010: A32 address space:

Bit 13-5 (R/W): Address Max; Reset default 0x1FF;

Bit 22:14 (R/W): Address Min; Reset default 0x000;

Bit 31-23 (R/W): Base Address. Reset default 0x100;

➤ Address offset: 0x00014: Block size:

Bit 7-0 (R/W): Block size. Reset default 0x01 This is used on TD only. It's read/write register but does not affect anything on TS and TI. For TI/TS, check Bit(31:16), Current/Next block levels.

The TD does not decode the serialized trigger word, so it can NOT get the block level setting from TS.

➤ Address offset: 0x00018: TI data format control: Reset default 011;

Bit 0: not used.

Bit 2-1: Event format control:

00: Shortest words per trigger;

01: The TI timing word is enabled;

10: The TI status word is enabled;

11: The TI timing word and status word are enabled;

➤ Address offset: 0x0001C: VME setting; Reset default 0x011:

Bit 0 (R/W): '1' enable Bus_Error_En, so the block read can be terminated by event block trailer;

Bit 1 (R/W): '1' en_token_in is true, '0' en_token_in is false;

Bit 2 (R/W): '1' enable 'Multi-board' readout, '0' disable 'Multi-board'; assert to enable multi-board token passing protocol;

Bit 3 (R/W): '1' enable en_A32m, '0' disable en_A32m; assert to enable common A32 multi-board addressing of module;

Bit 4 (R/W): '1' enable en_A32, '0' disable en_A32;

Bit 7 (R/W): '1' enable VME bus interrupt for module error?

Bit 8 (R/W): '1' I2C device address 0x1101xxx, '0' I2C device address 0x0000xxx;

Bit 9 (R/W): '1' token_in high, '0' token_in low;

Bit 10 (R/W): '1' first_board true, '0' first_board false;

Bit 11 (R/W): '1' last_board true, '0' last board false;

Bit 15 (R/W): '1' disable data readout buffer full

Bit 18:16 (R): "111" token

➤ Address offset: 0x00020: Trigger source register:

Bit 15-0 (R/W): Trigger source enables: Reset default 0x0000;

Bit 0: P0 trigger input; (not used?)

Bit 1:

Bit 2: Pulse trigger from P0 TRIGGER2 line. (TS→SD→TD)

Bit 3: Front panel trigger input;

Bit 4: VME trigger;

Bit 5: Front Panel Trigger Codes (as Supervisor) inputs; (not used?)

Bit 7: Random trigger;

Bit 9: VME P2 BUSY is used as pulse trigger input (from TS). Need jump wires.

Bit 10: SubTS trigger enable;

Bit 12: Enable SubTS#1 generation on TS, enable SubTS#1 trigger on TS, TD and TI;

Bit 13: Enable SubTS#2 generation on TS, enable SubTS#2 trigger on TS, TD and TI;

Bit 14: Enable SubTS#3 generation on TS, enable SubTS#3 trigger on TS, TD and TI;

Bit 15: Enable SubTS#4 generation on TS, enable SubTS#4 trigger on TS, TD and TI;

Bit 31-16 (R): Trigger source monitor.

➤ Address offset: 0x00024: Sync Source register:

Bit 7-0 (R/W): Sync Source enables: Reset default 0x02;

Bit 0: P0 sync input;

Bit 3: Front panel sync input;

Bit 4: TS loopback SYNC enable

Bit 31-16 (R): Sync source monitoring.

➤ Address offset: 0x00028: Busy source registers:

Bit 15-0 (R/W): Busy source enables:

Bit 2: '1' enable the VME P2 BUSY input, '0' disable;

Bit 6: '1' enable the waiting for trigger acknowledge (set BUSY between trigger and acknowledge).

Bit 7: '1' enable TS feed_back BUSY, '0' disable the busy. (useful in TM mode)

Bit 15-8: HFBR #8-#1 BUSY enables: '1' enable the HFBR BUSY input, '0' disable;

Bit 31-16 (R): BUSY source monitoring.

Bit 22: OR of the 'trigger not_acknowledge' from enabled TI boards.

➤ Address offset: 0x0002C: additional Busy monitor:

Bit 7:0 (R/W): bit (1:0): clock source selection; bit(5:4): mixed the inputs of FP with GTP for TS.

Bit 23-16 (R): TI#n (HFBR#n) BUSY;

Bit 15 (R): TD is BUSY. This BUSY is for TD when, mainly, FIFO is full;

➤ Address offset: 0x00030: Trigger prescale:

Bit 15-0 (R/W): Trigger prescale factor (Bit(15:0)+1). This is useful when the TD is configured as SubTS.

➤ Address offset: 0x00034: Trigger block inhibit:

Bit 7-0 (R/W): TS trigger inhibit threshold (in the unit of event blocks); Reset default 0x01;

Bit 23-8 (R): Number of blocks in the DAQ ready to be readout.

(on TI, Bit 23-16 (R): Number of events before the a block is formed.)

Bit 27-24 (R): Number of missing block acknowledge;

When the TI is used in SBS, Bit(27) is the OR of number of IRQ waiting; Bit 26-24 is the number of events which have Fastbus TDC data or ADC data.

Bit 28 (R): if '1', the RUN is stopped because the block number (readout) has reached. (set by 0xFC)

Bit 29 (R): if '1', the event block is being filled by FillTrg;

Bit 30 (R): SyncReset Request set. If '1', SyncReset is required. To be issued by TImaster/TS.

Bit 31 (R): SyncEvent received, and the system is BUSY. Waiting for ROC to clear the frontend data.

➤ Address offset: 0x00038: Trigger rules:

Bit 7-0 (R/W): No more than 1 Trigger in (Bit(6:0)*(16/500 ns)); Bit7 determines 16ns or 500ns step.
Reset default 0x03;

Bit 15-8 (R/W): no more than 2 trigger in (Bit(14:8)*(16/500ns)); Bit15 determines 16ns or 500ns step.
Reset default 0x03;

Bit 23-16 (R/W): no more than 3 triggers in (Bit(22:16)*(16/500 ns)); Bit23 determines 16ns or 500ns step.
Reset default 0x03;

Bit 31-24 (R/W): no more than 4 triggers in (Bit(30:24)*(16/500 ns)). Bit31 determines 16ns or 500ns step.
Reset default 0x03;

➤ Address offset: 0x0003C: Trigger coincidence window:

Bit 7-0 (R/W): Trigger input coincidence window; Reset default 0x01;

Bit15-8 (R/W): Trigger inhibit window (extra to bit(7:0)). Reset default 0x00;

These two parameters are used to determine the event resolution

Bit24-16 (R/W): Set the delay between TRIGGER2 and the (TRIGGER2 generated) TRIGGER1. The delay is in 4ns step with an offset (minimum setting) of ~2.6us;

➤ Address offset: 0x00040: MGT status(31:0) not used

➤ Address offset: 0x00044: Front panel trigger input enable (in TDp firmware):

Bit 5-0 (R/W): Front panel trigger input enable (TScore). Reset default 0x00000000;

➤ Address offset: 0x48: MGT status (63:32) not used

Bit 31-0 (R): TI MGT status (63:32)

- Address offset: 0x0004C: Blocks for VME interrupt:
 - Bit 3-0 (R/W): 4-bit output to the front panel generic output connector;
 - Bit 7-4 (R): Set to “0000”;
 - Bit 15-8: Number of blocks in readout;
 - Bit 23-16 (R): Number of data blocks ready for VME interrupt.
 - Bit 31-24 (R): on TI/TD: Number of events of a partial block (or, before the block is formed)
On TS: bit(15:8) of the number of data blocks ready for VME interrupt.
- Address offset: 0x00050: SyncDelay setting (TIp firmware):
 - Bit 7-0 (R): on TI: SYNC phase of HFBR#1 input;
 - Bit 15-8 (R/W): HFBR#1 SYNC input delay; Reset default 0x00;
 - Bit 23-16 (R/W): TM (internal loopback) SYNC delay; Reset default 0x00;
 - Bit 23-16 (R): on TI: SYNC phase of HFBR#5 input;
 - Bit(31:24 (R/W): HFBR#5 SYNC input delay. Reset default 0x00;
- Address offset: 0x00054: RocAckRead(31:0):
 - Bit 7-0 (R): Number of ROC#1 readout acknowledge; (Each TI can support upto 8 ROCs)
 - Bit 15-8 (R): Number of ROC#2 readout acknowledge;
 - Bit 23-16 (R): Number of ROC#3 readout acknowledge;
 - Bit 31-24 (R): Number of ROC#4 readout acknowledge;
- Address offset: 0x00058: RocAckRead(63:32):
 - Bit 7-0 (R): Number of ROC#5 readout acknowledge;
 - Bit 15-8 (R): Number of ROC#6 readout acknowledge;
 - Bit 23-16 (R): Number of ROC#7 readout acknowledge;
 - Bit 31-24 (R): Number of ROC#8 readout acknowledge;
- Address offset: 0x00064: Front panel generic trigger input prescale (TIp firmware):
 - Bit 3-0 (R/W): FP Generic trigger input #1;
 - Bit 7-4 (R/W): FP Generic trigger input #2;
 - Bit 11-8 (R/W): FP Generic trigger input #3;
 - Bit 15-12 (R/W): FP Generic trigger input #4;
 - Bit 19-16 (R/W): FP Generic trigger input #5;
 - Bit 23-20 (R/W): FP Generic trigger input #6;
- Address offset: 0x00074: VME event type setting (TIp firmware):
 - Bit 23-16 (R/W): VME periodic VME event type, default 0xFD;
 - Bit 31-24 (R/W): VME pseudo random trigger event type, default 0xFE.
- Address offset: 0x00078: VME Sync Load
 - Bit 7-4 == Bit 3-0 (R/W): 4-bit sync code; Decoding of the Sync command (bit[7:0]):

0x11: VME clock DCM reset, and full reset;
 0x22: CLK250 resync (AD9510, DCM resync and MGT reset);
 0x33: AD9510 re-sync (slower clock phase adjustment), part of 0x22 function;
 0x44: Reset the MGT status_B registers;
 0x55: Trigger link enable (serial link started), FIFO read counter reset;
 0x77: Trigger link disable, trigger FIFO write counter reset;
 0xAA: reset the TI_trigger_enabled registers on TD.
 0xBB: Event number reset, and trigger input scalar reset;
 0xDD: (SyncReset), FPGA logic and counter reset, this reset does not go to SD, CTP/GTP;
 0x99: Force SyncReset high if this feature is enabled (by offset 0x24, bit 7);
 0xCC: set the SyncReset low if it is forced high by code 0x99.
 0xEE: set the SyncReset for ~4 us.
 0x66, 0x88, to be assigned;
 0x00, 0xff: reserved, not to be assigned

- Address offset: 0x0007C: VME Sync Delay. The latency before being serialized.
 Bit 6-0 (R/W): latency, in 4ns steps. Reset default 000,0111
- Address offset: 0x00080: Reset pulse width: Reset default 00,0111
 Bit 7-0 (R/W): Reset (to SW#A, SW#B and on-board) pulse width. Pulse width is $(\text{Bit}(6:0) * (4/32 \text{ ns}))$,
 Bit(7) determines the steps (4ns or 32ns);
- Address offset: 0x00084 (R/W): VME Trigger command
 Bit 15-0: VME trigger command.
 Bit (11-8): command code, 0011 for Sync event; 0x0001: trigger 1; 0x0010: trigger 2; 0x1000: set block level, or block size.
 Bit (7-0): Event type, or block level value.
- Address offset: 0x00088 (R/W): VME Random Trigger Command Register:
 Bit 3-0: Random trigger_1 rates: $500\text{KHz} / (2^{\text{Bit}(3:0)})$;
 Bit 6-4: same as Bit(2-0) for redundancy check. No match, no trigger_1;
 Bit 7: enable/disable random trigger_1; (There is NO requirement that it match with bit 3)
 Bit 11-8: Random trigger_2 rates: $500\text{KHz} / (2^{\text{Bit}(11:8)})$;
 Bit 14-12: same as Bit(10-8) for redundancy check. No match, no trigger_2.
 Bit 15: enable/disable random trigger_2;
- Address offset: 0x0008C(R/W): VME Trigger Generation:
 Bit 15-0: Number of trigger_1s to be generated; If 0xFFFF, the number of event will not be limited.
 Bit 31-16: (trigger rate control) Time between triggers. $T = (120 + 30 * \text{Bit}(30:16)) * 1024^{\text{Bit}(31)}$ ns. (Assuming that the ClkVme=33MHz or 30ns period).
- Address offset: 0x00090(R/W): VME Trigger_2 Generation:
 Bit 15-0: Number of trigger_2s to be generated;

Bit 31-16: (trigger rate control) Time between triggers. $T = (120 + 30 * \text{Bit}(30:16)) * 1024^{\text{Bit}(31)}$ ns. (Assuming that the ClkVme=33MHz or 30ns period).

- Address offset: 0x00094 (R): Number of Blocks in the DAQ system:

Bit 31-24: Number of events of a partial data block;

Bit 23-0: Number of full data blocks the TIDS has ever generated;

- Address offset: 0x00098 (R): Sync History

Bit 31-0: Sync History buffer readout. The readout will be 0 if the buffer is empty.

Bit 19: TS generated SYNC, bit(18:15): TS sync code;

Bit 14: TD loopback sync, bit(13:10): loopback code; This is the code it sends to TI, and also used on TD.

Bit(3:0)&bit(31:21) time stamp of the sync code;

Bit(9:6): Sync FIFO status: FULL, Prog_FULL, EMPTY, RegisterEMPTY

- Address offset: 0x0009C (R/W): The FPGA running mode;

Bit 7-0: TS in running mode if set to 0x5A; if other value, not in running mode. Reset default 0x00;

TI in running mode if set to 0x71. TI starts clock monitoring in 'running' mode.

TD in running mode if set to 0x7D.

- Address offset: 0x000A8 (R): Trigger live timer:

Bit 31-0 (r): board live time counter. The real time is $\text{Bit}(31:0) * 256 * 30\text{ns}$.

- Address offset: 0x000AC (R): Trigger busy (trigger dead) timer:

Bit 31-0 (r): TID busy (can not accept trigger, or trigger dead) time counter. The real time is $\text{Bit}(31:0) * 256 * 30\text{ns}$. This counter and the live time counter make up the total time counter, which is the total time since any one of the trigger sources is enabled.

- Address offset: 0x000B0 (R): MGT STATUS_A:

Bit 7-0: MGT[7:0] reset_done;

Bit 11-8: MGT PLL lock detected (two MGTs per PLL lock);

Bit 23-12 : not used yet;

Bit 31-24: Gigabit idle word on the HFBR#8, #7,...#1;

- Address offset: 0x000B4 (R): MGT STATUS_B registers:

Bit 7-0: Channel bonding sequence detected in MGT[7:0];

Bit 15-8: received data is not an 8B/10B character, or has disparity error in MGT[7:0];

Bit 23-16: RX disparity error has occurred in MGT[7:0];

Bit 31-24: Rx data not in 8B/10B table has occurred in MGT[7:0].

- Address offset: 0x000B8 (R): MGT trigger data buffer length:

Bit 9-0: TD trigger receiving FIFO length;

Bit 11-10: TD data generation FIFO FULL/Prog_FULL;

Bit 15-12: TD data readout FIFO FULL/Prog_FULL;

Bit 27: TD is in running mode if '1';

Bit 28: HFBR#1 MGT receiver error;
Bit 29: CLK250 DCM locked;
Bit 30: Clk125 DCM locked;
Bit 31: VME CLK (33MHz or 25MHz) DCM locked

➤ Address offset: 0x000BC (R): TS input trigger counter:

Bit 31-0: Number of triggers received by TS (before BUSY inhibits).

➤ Address offset: 0x000C0 (R):

Bit 7-0: Number of blocks to be readout on HFBR#1;
Bit 15-8: Number of blocks is still missing on HFBR#1
Bit 23-16: Number of blocks to be readout on HFBR#2
Bit 31-24: Number of blocks is still missing on HFBR#2

➤ Address offset: 0x000C4 (R):

Bit 7-0: Number of blocks to be readout on HFBR#3;
Bit 15-8: Number of blocks is still missing on HFBR#3;
Bit 23-16: Number of blocks to be readout on HFBR#4;
Bit 31-24: Number of blocks is still missing on HFBR#4;

➤ Address offset: 0x000C8 (R):

Bit 7-0: Number of blocks to be readout on HFBR#5;
Bit 15-8: Number of blocks is still missing on HFBR#5;
Bit 23-16: Number of blocks to be readout on HFBR#6;
Bit 31-24: Number of blocks is still missing on HFBR#6;

➤ Address offset: 0x000CC (R):

Bit 7-0: Number of blocks to be readout on HFBR#7;
Bit 15-8: Number of blocks is still missing on HFBR#7;
Bit 23-16: Number of blocks to be readout on HFBR#8;
Bit 31-24: Number of blocks is still missing on HFBR#8;

➤ Address offset: 0x000D0 (R): (was 0xD0 in TD firmware V7.1 and earlier)

Bit 4-0: A24 address used for the module (to match with A23-A19);
Bit 9-5: A24 address set by the onboard hardware switch;
Bit 14-10: GA(4:0), VME64x geographic address;
Bit 15: parity of GA(4:0);
Bit 23-16: Number of blocks to be readout on TM itself;
Bit 31-24: Number of blocks is still missing on TM itself;

➤ Address offset: 0x000D4 (R/W): Periodic Sync Event register

Bit 19-0: Number of data blocks to assert a sync event (periodic SyncEvent);
Bit 31-20: not used. When the Bit(19:0) is not zero, the Sync event is enabled.

➤ Address offset: 0x000D8 : Prompt Trigger width and Event number register

Bit 7-0 (R/W): Prompt Trigger Width, width = (bit(6:0) + 3) * 4ns;

Bit 31-16: higher 16-bit (bit 47-32) of event number counter;

- Address offset: 0x000DC (R): Event number register

Bit 31-0: lower 32-bit (bit 31-0) of event number counter.

- Address offset: 0x000EC: ROC enable, GTP_ROC_ID

Bit 7-0 (R/W): ROC 8:1 enable, the default is 00000001

Bit 18-10 (R/W): SyncResetRequest enable. For TImaster and TD, this corresponds to the eight TI slaves (bit#18:11) and the loopback (bit#10).

Bit 28-20 (R): Monitor of the SyncResetRequest corresponding to the bit#18:10.

- Address offset: 0x000F0 (R): valid for TM (or with TS function)

Bit 31-0: Number of valid code from Front Panel Async trigger inputs

- Address offset: 0x000FC (R/W): Generic enable control

Bit 23-0: Number of data blocks to end the run. This is used only when the TD is configured as a subsystem TS (like a TImaster).

- Address offset: 0x00100 (W): Reset and one-shot registers. The signal will be one ClkVme cycle. If the ClkVme is 25 MHz, the one-shot will be 40ns wide. Positive logic.

Bit 0: not used;

Bit 1: if '1', RESET signal to reset the VME_to_I2C engine;

Bit 2: if '1', RESET signal to reset the VME_to_JTAG engine;

Bit 3: if '1', RESET signal to reset the VME_to_SFM engine;

Bit 4: if '1', RESET signal to reset the VME registers (TID settings) to their default values;

Bit 7: if '1', this register will generate a BUSY reset, and Trg_Ack pulse (TS rev2 compatible).

Bit 8: if '1', Reset the CLK250/Clk200 DCM.

Bit 9: if '1', Reset the CLK125 DCM.

Bit 10: if '1', Reset the MGT (MultiGigabit Transceiver,) inside the FPGA.

Bit 11: if '1', Auto alignment of SYNC phase from HFBR#1; auto align P0 sync input for TD.

Bit 12: if '1', TI: Auto alignment of SYNC phase from HFBR#5;

TS: reset the BRAM loading address to 0 (very beginning).

Bit 13: if '1', Auto alignment of fiber latency measurement signals;

Bit 14: if '1', Reset the IODELAY;

Bit 15: if '1', Measure the fiber latency

Bit 16: if '1', this register will generate a 'TAKE_TOKEN'

Bit 17: if '1', the available number of data blocks will decrease by 1,

Bit 20: if '1', generate a SyncEvent (forced SyncEvent). This can be used as end_of_run etc.

Bit 21: if '1', clock reset for the ClkVme, and all other clocks (similar to Sync_code 0x11), Be cautious.

Bit 22: if '1', MGT Rx_CDR reset, which also includes RxReset.

Bit 23: if '1', generate Sync_Reset_Request.

Bit 24: if '1', all the trigger input scalars are latched (ready for read out); also latch the live/busy timer counters;

Bit 25: if '1', all the trigger input scalars are reset. (Bit 24 and Bit 25 can be set simultaneously)

- Address offset: 0x00104 (R/W): FP input trigger (TS Code) delay (in 4 ns steps):
 - Bit 8-0: TScore#1 trigger input delay (Channel#1);
 - Bit 18-10: TScore#2 trigger input delay (Channel#2);
 - Bit 28-20: TScore#3 trigger input delay (Channel#3);
- Address offset: 0x00108 (R/W): FP input trigger (TS Code) delay (in 4 ns steps):
 - Bit 8-0: TScore#4 trigger input delay (Channel#4);
 - Bit 18-10: TScore#5 trigger input delay (Channel#5);
 - Bit 28-20: TScore#6 trigger input delay (Channel#6);
- Address offset: 0x00128 (R): Front Panel Busy input scalar:
 - Bit 31-0: Busy scalar caused by the front panel input;
- Address offset: 0x138 (R/W): Extra hold off after trigger rule (minimum busy width)
 - Bit 31: '1' to enable the minimum busy width for trigger rule#4;
 - Bit(30:24): Minimum busy width for rule#4. $\text{MinimumWidth} = \text{bit}(30:24) * \text{Tclock}$. $\text{Tclock} = 480\text{ns}$ if bit#31 of Reg#1C is set to '0'; $\text{Tclock} = 480 * 32\text{ns}$ if bit#31 of Reg 0x1C is set to '1';
 - Bit 23: '1' to enable the minimum busy width for trigger rule#3;
 - Bit(22:16): Minimum busy width for rule#3. $\text{MinimumWidth} = \text{bit}(22:16) * \text{Tclock}$. $\text{Tclock} = 480\text{ns}$ if bit#31 of Reg#1C is set to '0'; $\text{Tclock} = 480 * 32\text{ns}$ if bit#31 of Reg 0x1C is set to '1';
 - Bit 15: '1' to enable the minimum busy width for trigger rule#2;
 - Bit(14:8): Minimum busy width for rule#2. $\text{MinimumWidth} = \text{bit}(14:8) * 16\text{ns}$. The maximum width setting is $\sim 2\mu\text{s}$.
 - Bit 7-0: Minimum busy width for trigger rule#1, not used, and no need for this.
- Address offset: 0x00140-0x0017C (W): Trigger table loading (it was 0x8C0-8FC)
 - Bit 31-0: Data to be loaded into event lookup table, totally 64 bytes, or 16 4-byte words;
 - Address bits(5-2) are used to load 16 32-bit words;
 - 6-bit read addressing with 8-bit trigger type (byte wide)
- Address offset: 0x00180 (R): FP input trigger scalar for #1:
 - Bit 31-0: 32-bit scalar, number of input#1 counter
- Address offset: 0x00184 (R): FP input trigger scalar for #2:
 - Bit 31-0: 32-bit scalar, number of FP input#2 counter
- Address offset: 0x00188 (R): FP input trigger scalar for #3:
 - Bit 31-0: 32-bit scalar, number of FP input#3 counter
- Address offset: 0x0018C (R): FP input trigger scalar for #4:
 - Bit 31-0: 32-bit scalar, number of FP input#4 counter
- Address offset: 0x00190 (R): FP input trigger scalar for #5:

Bit 31-0: 32-bit scalar, number of FP input#5 counter

- Address offset: 0x00194 (R): FP input trigger scalar for #6:

Bit 31-0: 32-bit scalar, number of FP input#6 counter

- Address offset: 0x0019C (R): TD loopback readout busy counter.

Bit 31-0: 32-bit Busy timer of TD readout (same steps as live/busy timer).

- Address offset: 0x001A0 (R): TI#1 readout busy counter

Bit 31-0: 32-bit Busy timer of TI#1 (same steps as live/busy timer).

- Address offset: 0x001A4 (R): TI#2 readout busy counter

Bit 31-0: 32-bit Busy timer of TI#2 (same steps as live/busy timer).

- Address offset: 0x001A8 (R): TI#3 readout busy counter

Bit 31-0: 32-bit Busy timer of TI#3 (same steps as live/busy timer).

- Address offset: 0x001AC (R): TI#4 readout busy counter

Bit 31-0: 32-bit Busy timer of TI#4 (same steps as live/busy timer).

- Address offset: 0x001B0 (R): TI#5 readout busy counter

Bit 31-0: 32-bit Busy timer of TI#5 (same steps as live/busy timer).

- Address offset: 0x001B4 (R): TI#6 readout busy counter

Bit 31-0: 32-bit Busy timer of TI#6 (same steps as live/busy timer).

- Address offset: 0x001B8 (R): TI#7 readout busy counter

Bit 31-0: 32-bit Busy timer of TI#7 (same steps as live/busy timer).

- Address offset: 0x001BC (R): TI#8 readout busy counter

Bit 31-0: 32-bit Busy timer of TI#8 (same steps as live/busy timer).

- Address offset: 0x001D0 (R): optic transceiver HFBR#1 TI ID

Bit 7-0: Trigger Source Enable of the TI connected to fiber#1;

Bit 15-8: Crate ID of the TI connected to fiber#1.

Bit 23-16: Block level set on TI connected to fiber#1.

- Address offset: 0x001D4 (R): optic transceiver HFBR#2 TI ID

Bit 7-0: Trigger Source Enable of the TI connected to fiber#2;

Bit 15-8: Crate ID of the TI connected to fiber#2.

Bit 23-16: Block level set on TI connected to fiber#2.

- Address offset: 0x001D8 (R): optic transceiver HFBR#3 TI ID

Bit 7-0: Trigger Source Enable of the TI connected to fiber#3;

Bit 15-8: Crate ID of the TI connected to fiber#3.

Bit 23-16: Block level set on TI connected to fiber#3.

- Address offset: 0x001DC (R): optic transceiver HFBR#4 TI ID

Bit 7-0: Trigger Source Enable of the TI connected to fiber#4;

Bit 15-8: Crate ID of the TI connected to fiber#4.

Bit 23-16: Block level set on TI connected to fiber#4.

- Address offset: 0x001E0 (R): optic transceiver HFBR#5 TI ID

Bit 7-0: Trigger Source Enable of the TI connected to fiber#5;

Bit 15-8: Crate ID of the TI connected to fiber#5.

Bit 23-16: Block level set on TI connected to fiber#5.

- Address offset: 0x001E4 (R): optic transceiver HFBR#6 TI ID

Bit 7-0: Trigger Source Enable of the TI connected to fiber#6;

Bit 15-8: Crate ID of the TI connected to fiber#6.

Bit 23-16: Block level set on TI connected to fiber#6

- Address offset: 0x001E8 (R): optic transceiver HFBR#7 TI ID

Bit 7-0: Trigger Source Enable of the TI connected to fiber#7;

Bit 15-8: Crate ID of the TI connected to fiber#7.

Bit 23-16: Block level set on TI connected to fiber#7.

- Address offset: 0x001EC (R): optic transceiver HFBR#8 TI ID

Bit 7-0: Trigger Source Enable of the TI connected to fiber#8;

Bit 15-8: Crate ID of the TI connected to fiber#8.

Bit 23-16: Block level set on TI connected to fiber#8.

- Address offset: 0x001F0 (R): The TI master (itself) ID (in master mode)

Bit 7-0: Trigger Source Enable of the TI itself, should be the same as bit7-0 of register 0x20;

Bit 15-8: Crate ID of the TI itself, should be the same as bit7-0 of register 0x00.

- Address offset: 0x0DCxx (0xDC00 – 0xDDFC) (W): SysMon register

Bit 31-16: to be ignored.

Bit 15-0: 16-bit register of Virtex-5 FPGA System Monitor data interface.

Address 0xDC00 – 0xDCFC: read only registers,

Address 0xDD00 – 0xDDFC: Read and write registers.

6.3 VME to Serial engines:

A24D32 are used for VME to serial engines. The engines include: VME to JTAG engine for the FPGA, VME to JTAG engine for the PROM, and VME to I2C engine for the TIDqsfq QSFP transceivers.

Address offset: 0x1XXXX: JTAG for PROM; Refer to the programming manual for VME to JTAG design for details.

Address offset: 0x2XXXX: JTAG for FPGA;

Address offset: 0x5XXXX: I2C interface for the front panel optic transceivers.

Address offset: 0x6XXXX: Serial Flash memory interface.

Address offset: 0x0NXXX: SFM memory readout: (to be implemented)

0x07X0: IO_Delay #X reset;

0x07X4: IO_Delay #X delay increment (by 1);

0x07X8: IO_Delay #X de-serialized data readout, idle='0xFFFF';

0x07Xc: IO_Delay #X automatic delay increment by a number stored in SFM.

6.4 VME data acquisition:

For data acquisition, the A32 block reads are used. The base address is set by the upper 9 bits of A24 register 0x00010, that is A[31:23] = RegData[31:23] of A24=0x00010.

7 Backplane pin out tables:

7.1 VXS P0 Pinout Table

DP23 (B12+, C12-)	TRIG_LINK	LVPECL(DP)	PP ← SWB
DP24 (E12+, F12-)	SYNC	LVPECL(DP)	PP ← SWB
DP25 (A13+, B13-)	CLK250MHz	LVPECL(DP)	PP ← SWB
DP26 (D13+, E13-)	Pulse Trigger	LVPECL(DP)	PP ← SWB
DP27			
DP28			
DP29	SD_Data_link	LVDS	PP ↔ SWB
DP30	BUSY	LVDS	PP → SWB
SE7			
SE8			

7.2 VME P2 User-defined pin table

Similar to this, but Row-C is used. The two adjacent pins are used as a pair for differential signals.

Pin name	Signal Name	Signal Level
C29	Pulsed Trigger +	ECL
C30	Pulsed Trigger -	ECL

8 TD Operation examples:

The following is some operating procedures at VxWorks interactive mode. This is just a memo for the quick test of the TD board. They may change as the TD debug proceeds. First, one needs to login the VME controller. Here is the sequence:

Xming to PHECDA, linux server computer

From any xterm (or PUTTY), telnet to DAVW1 (neither username, nor password is needed). Only one telnet process is supported for the MVME6100 module). The address mapping for A24 is 0x90xxxxxx. For DAVW8, which is a MVME5100 module, the address mapping for A24 is 0xFA000000. The M6100 has twice as much as M5100 in A32 memory. The M5100 is 0x08000000-0x0FFFFFFF; while the M6100 is 0x08000000-0x17FFFFFFF.

The following commands are assuming that the TID is in slot#6 VME64x compatible crate (Geographic address available). 0x30 = 00110xxx, that is the Geographic Address GA=6 or 00110.

8.1 A24 register echoing (write and read):

➔ *(0x90A80008)=0x5566aa99; the same register should be read out

8.2 Readout the FPGA user_ID:

The FPGA user code is readout through VME_to_JTAG engine. The FPGA user_ID is firmware specific. If this code matches, it is TID and the right version of the firmware is loaded.

- ➔ *(0x90a80100)=0x04: VME_to_JTAG engine logic reset
- ➔ *(0x90aa003C)=0x0: Reset FPGA JTAG to 'reset_idle' state
- ➔ *(0x90aa092C)=0x3C8: enable user_ID readback
- ➔ *(0x90aa1F1C)=0x00: shift in 32-bit data, and the readback is user_ID. The user_ID should be 710xnmmm: n is the major version of the firmware, mmm is the revision of the firmware.

9 TD Operation procedures (software setup):

The following is the operating procedures at VxWorks interactive mode. This is just a memo for the quick test of the TD board. The procedure will be optimized as the test goes along. This assumes that the hardware switch is set properly.

The following commands are assuming that the TD is in slot#6 VME64x compatible crate (Geographic address available). The MVME6100 controller is used, which has A24 memory mapping to 0x90#####. For slot#6 TID, the A24 address will be: 0x9030xxxx. The A32 address will be 0x08-0x17##### on VME, and mapped to 0x80000000-0x8FFFFFFF on CPU.

The software is located at phedca:~jgu/software/tid.c. The tid.c works with the ~jgu/usrTempeDma_AM.o, which is the modified version of usrTempeDma.o for user defined AM codes, on MVME6100. The software for different platforms can be written with minor changes.

9.1 Trigger/DAQ monitoring:

- ➔ M 0x90a80034, 4 //polling the register to see if there is data block to read
- ➔ M 0x90a800a8, 4 //TID trigger live timer (live time)
- ➔ M 0x90a800ac, 4 //TID trigger busy timer (dead time)

9.2 Data Readout:

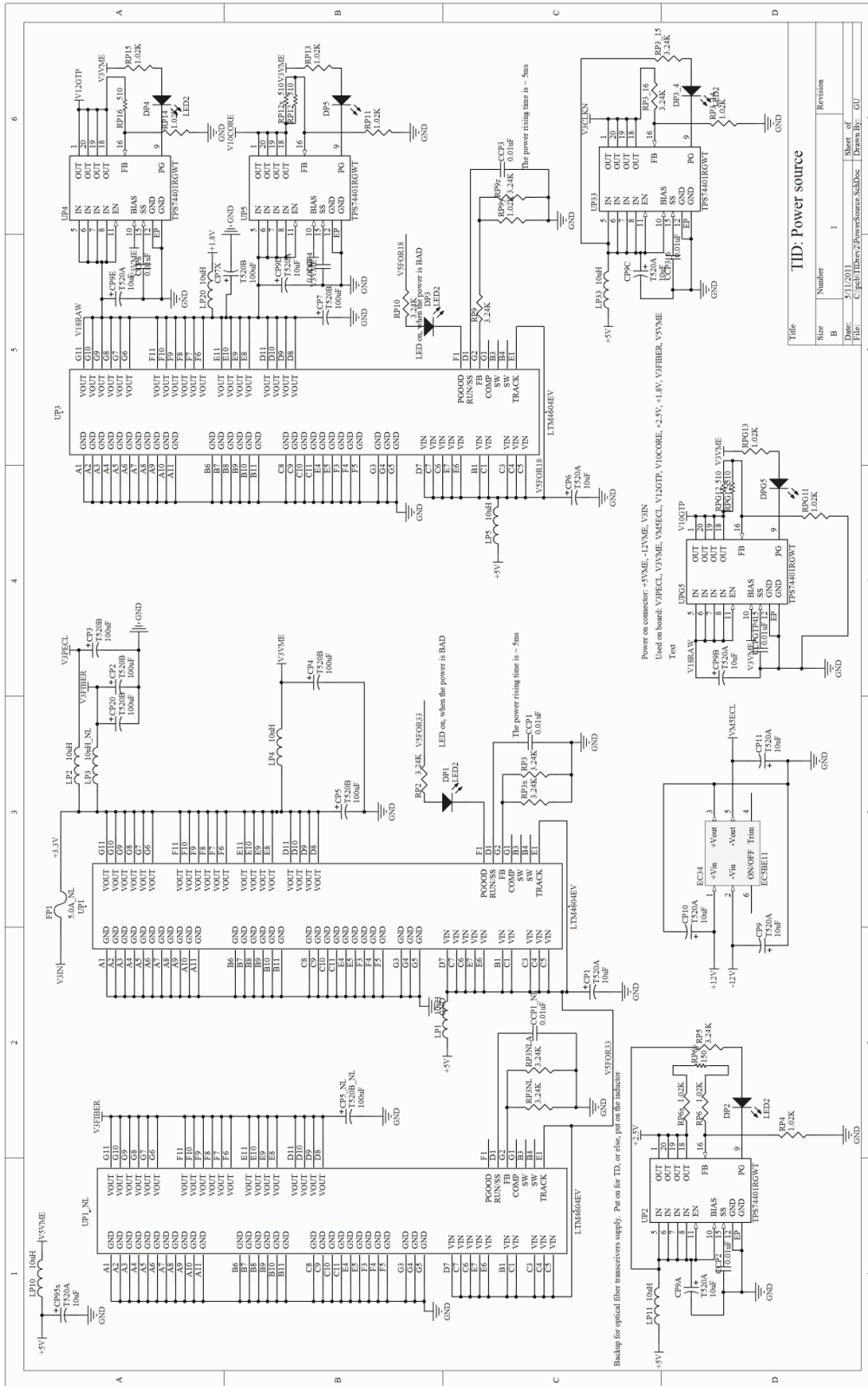
- ➔ M 0x80300100,4 //A32 readout; or
- ➔ tidRead(slot, nwords) //readout nwords from TI; or
- ➔ tidBERead(slot) // readout a block, and using Bus_error to terminate the read; or
- ➔

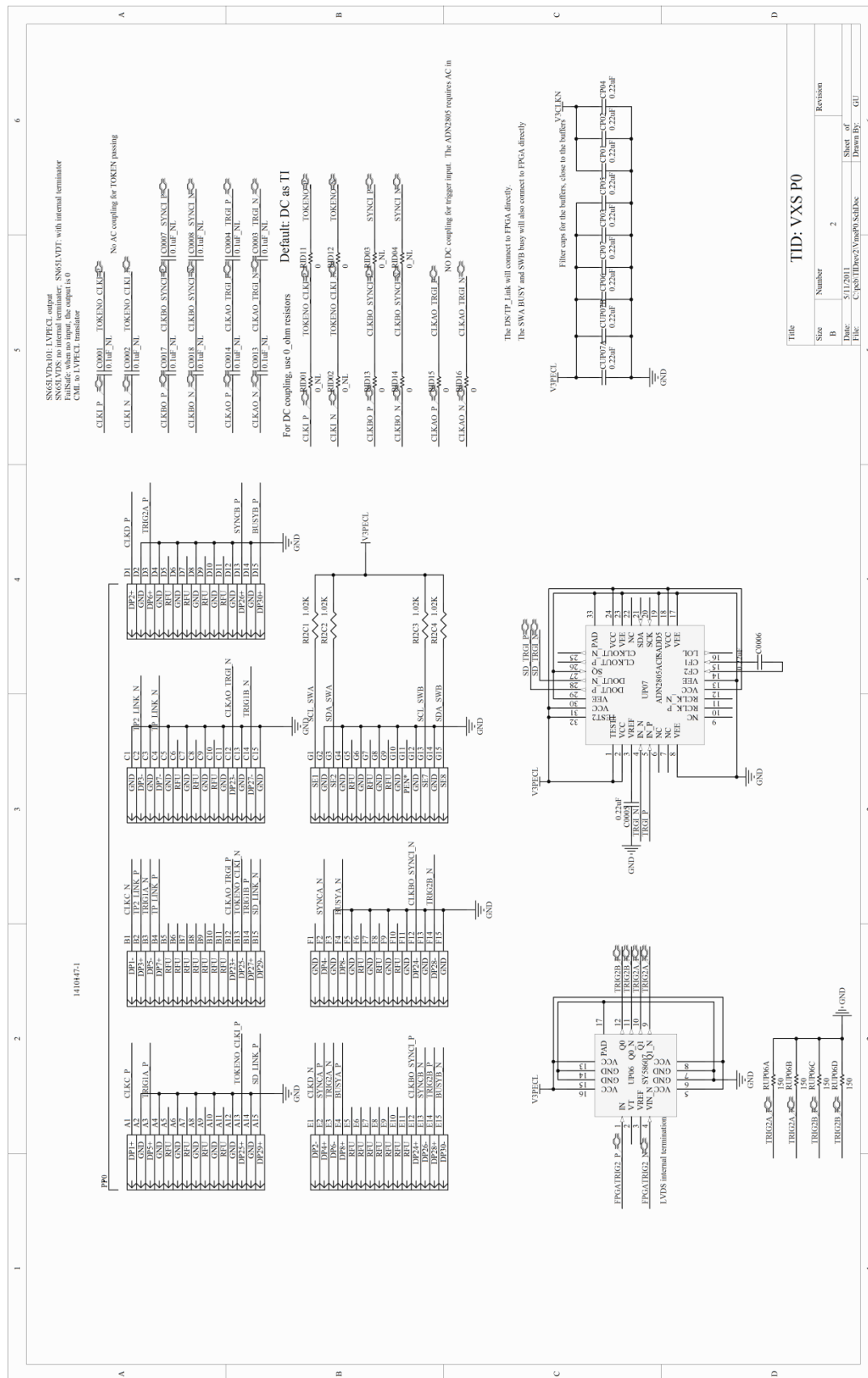
10. Citations:

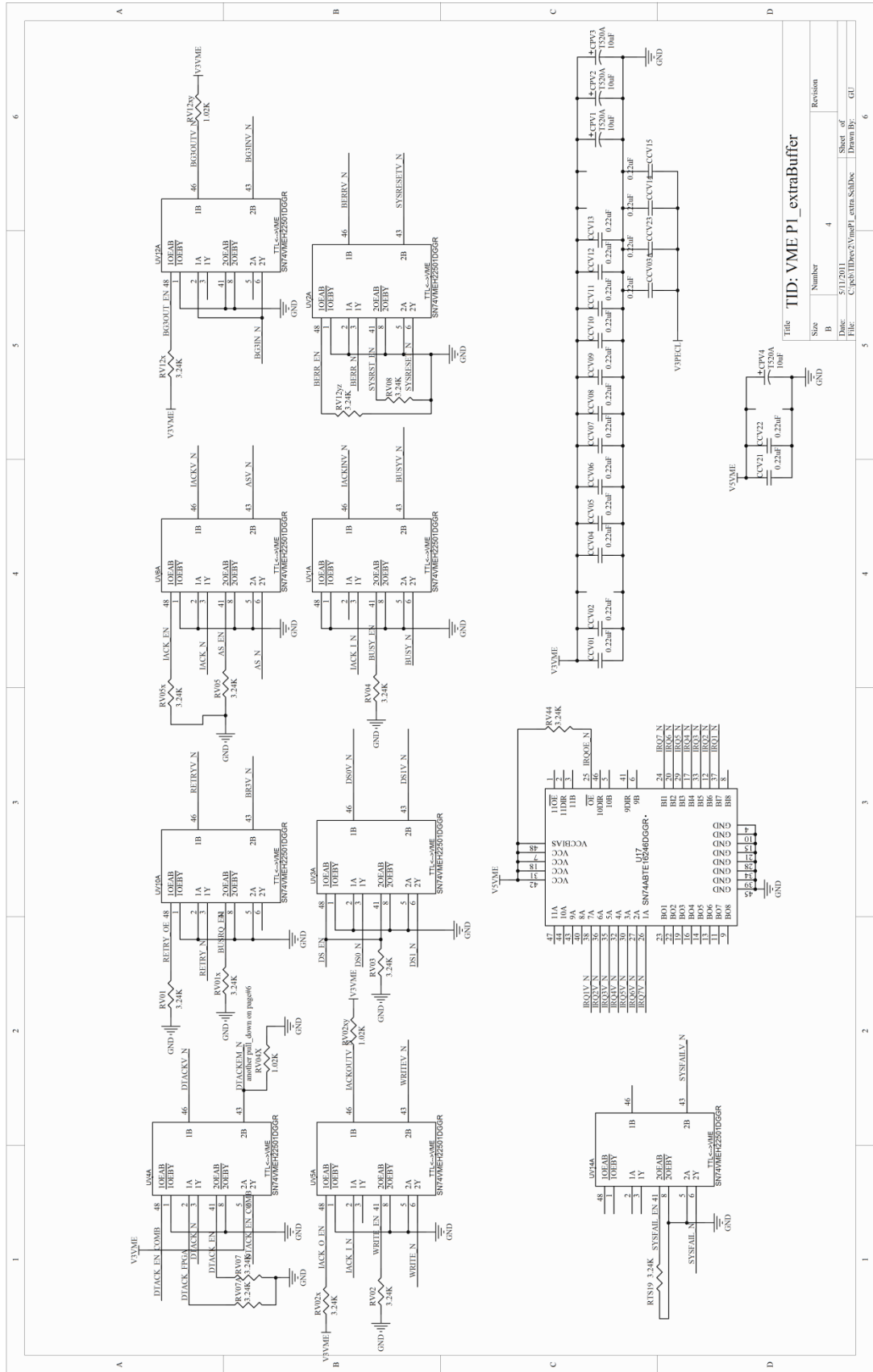
Works Cited

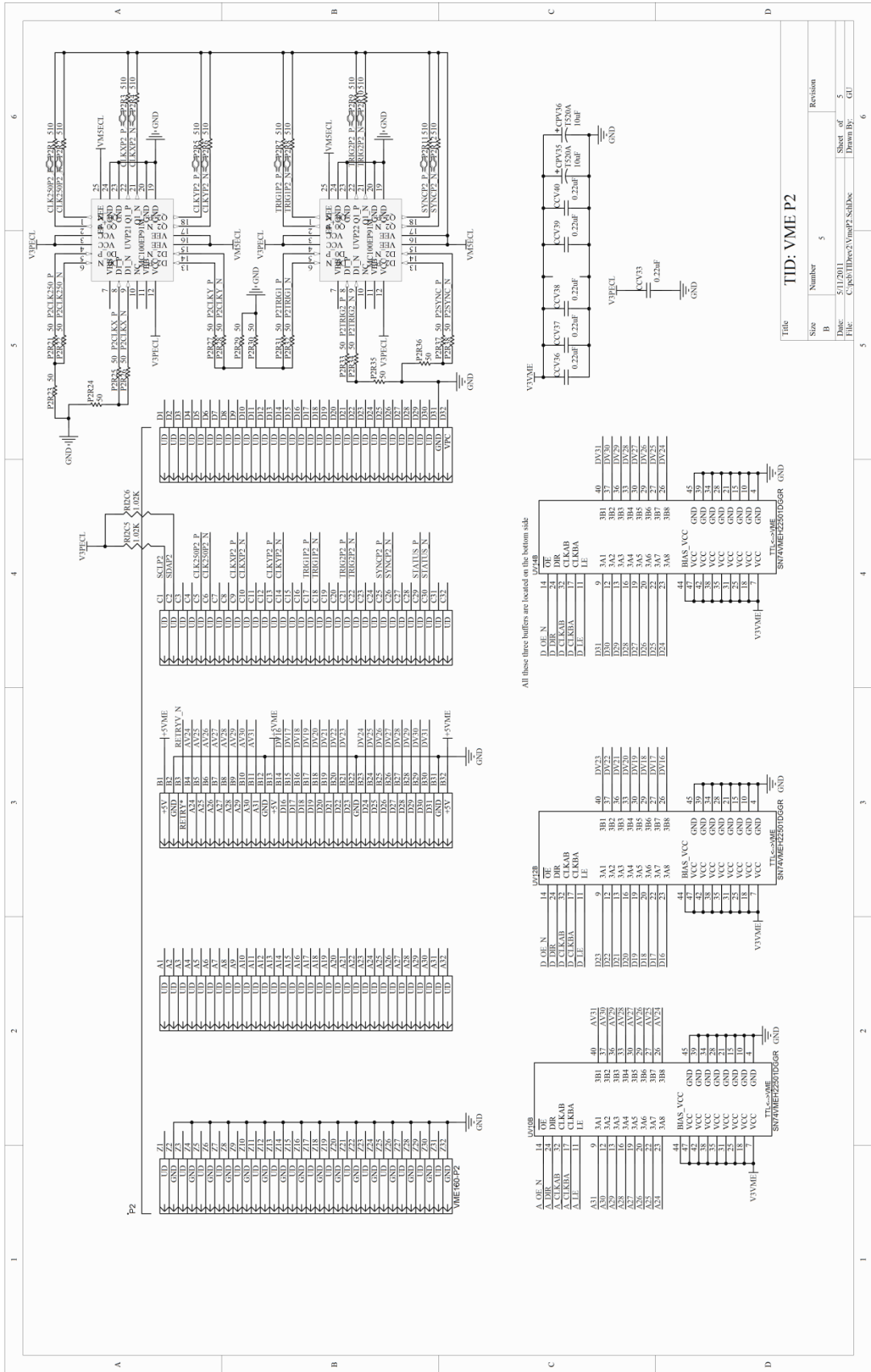
- Chris. (2009). Gloabal Trigger Processor., (pp. 1-14).
- Chris. (2009). Hall_D trigger layout., (pp. 20-25). Virginia.
- Collaboration, C. (2009). CLAS12 experiment. *Journal* , 1-25.
- Collaboration, G. (2009). GlueX experiment. *journal* , 1-20.
- Cuevas, C. (2008). Signal Distribution Module., (pp. 1-10).
- Ed. (2010). Trigger Supervisor Module., (pp. 1-19).
- experiments, C. (1990). CEBAF experiements. *journal* , 1-10.
- GU. (2010). Optical transceiver jitter measurement., (pp. 1-12).
- Raydo, B. (2008). Trigger Distribution board., (pp. 1-10).
- GU, (2010). VME to JTAG implementation
- GU, (2010). VME to I2C implementation

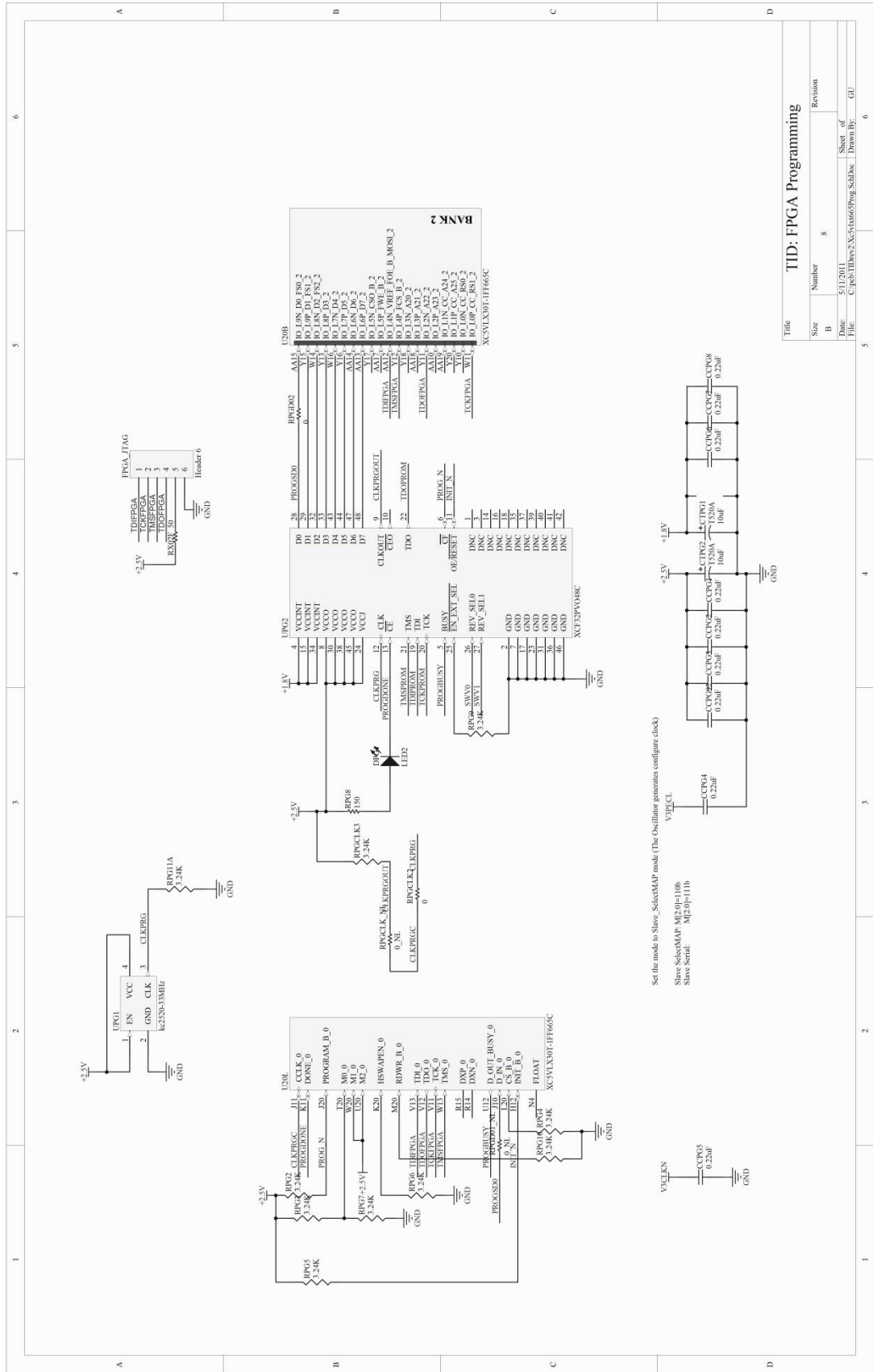
Appendix A: TID Schematics:

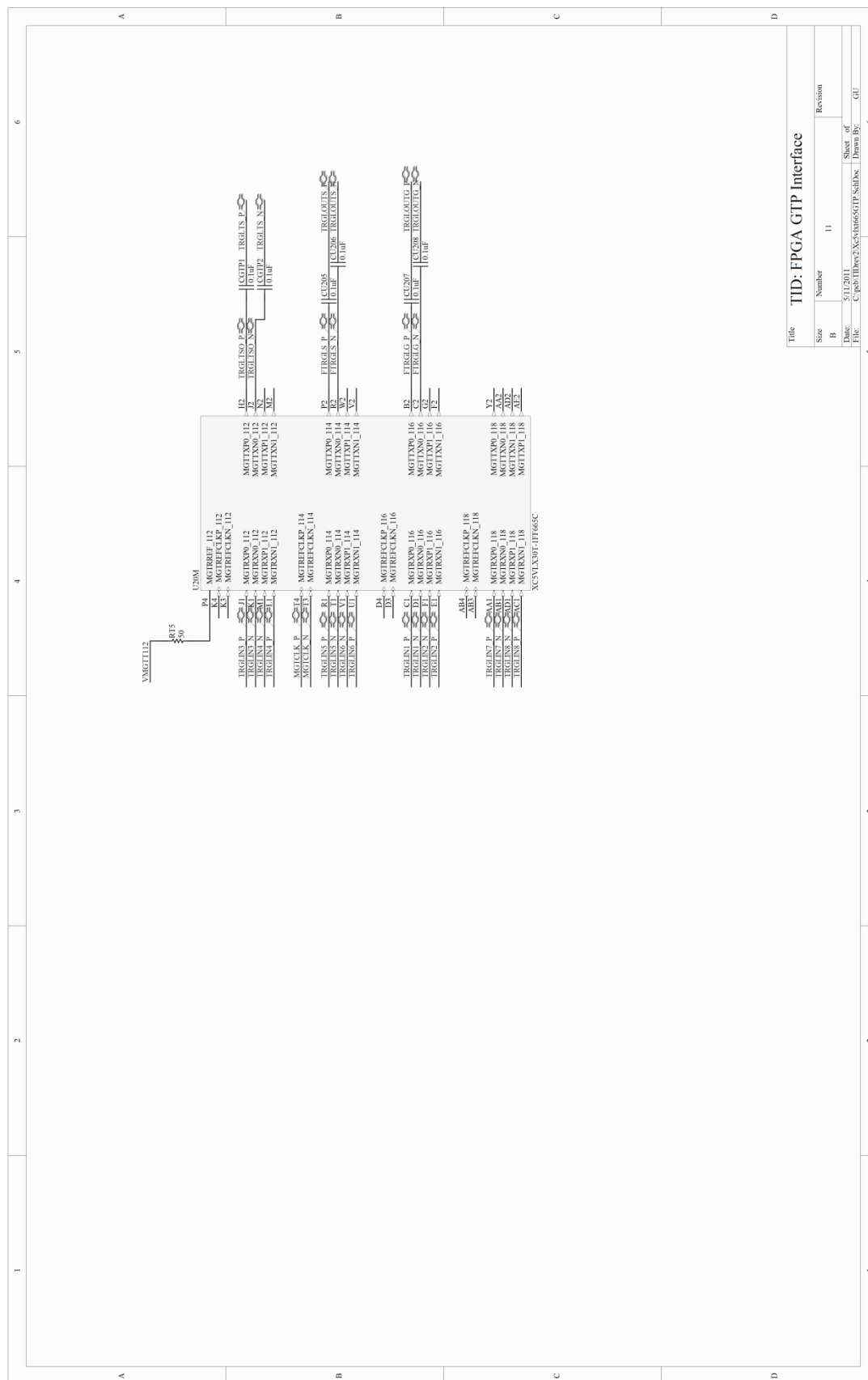


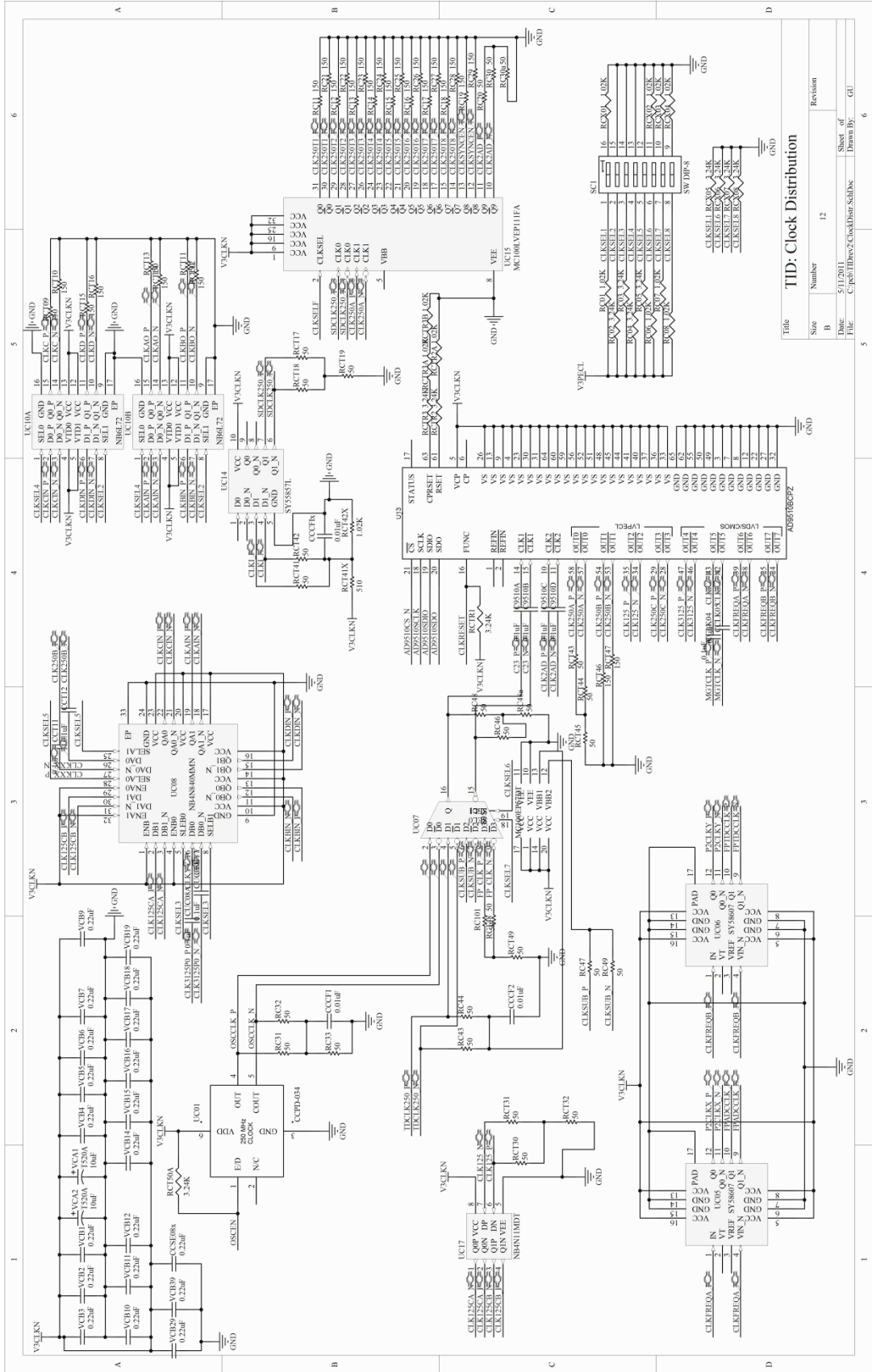






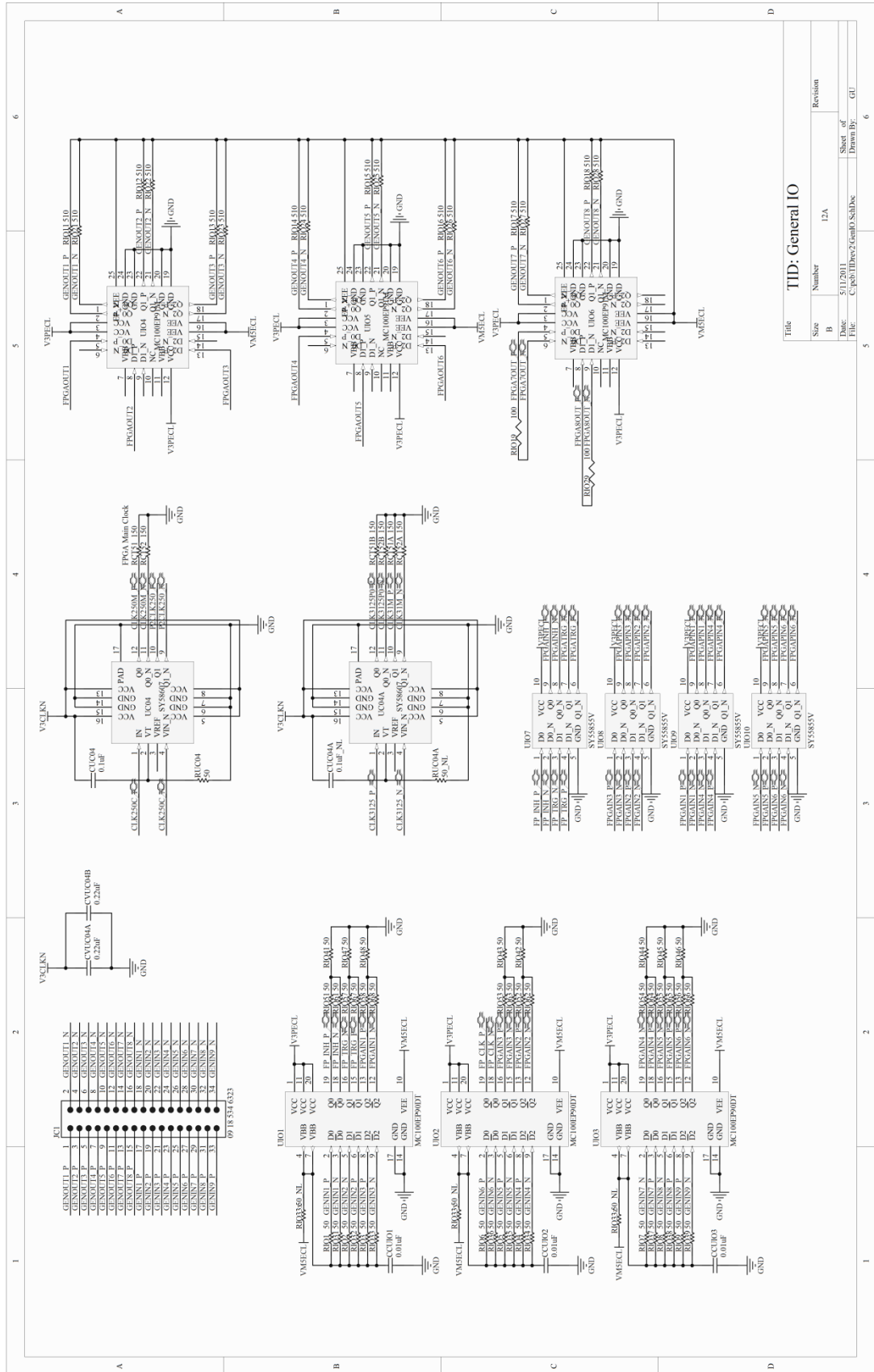


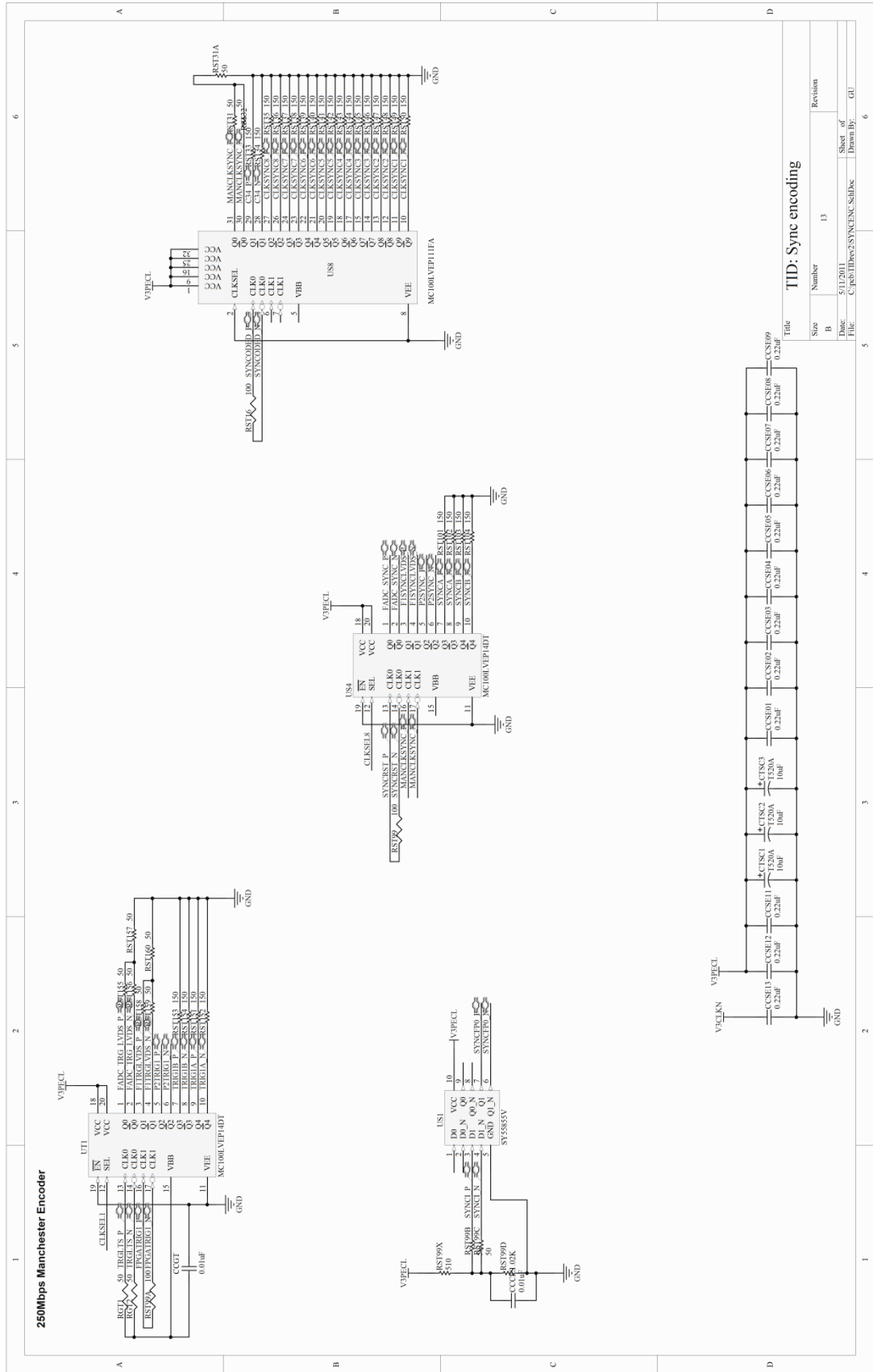


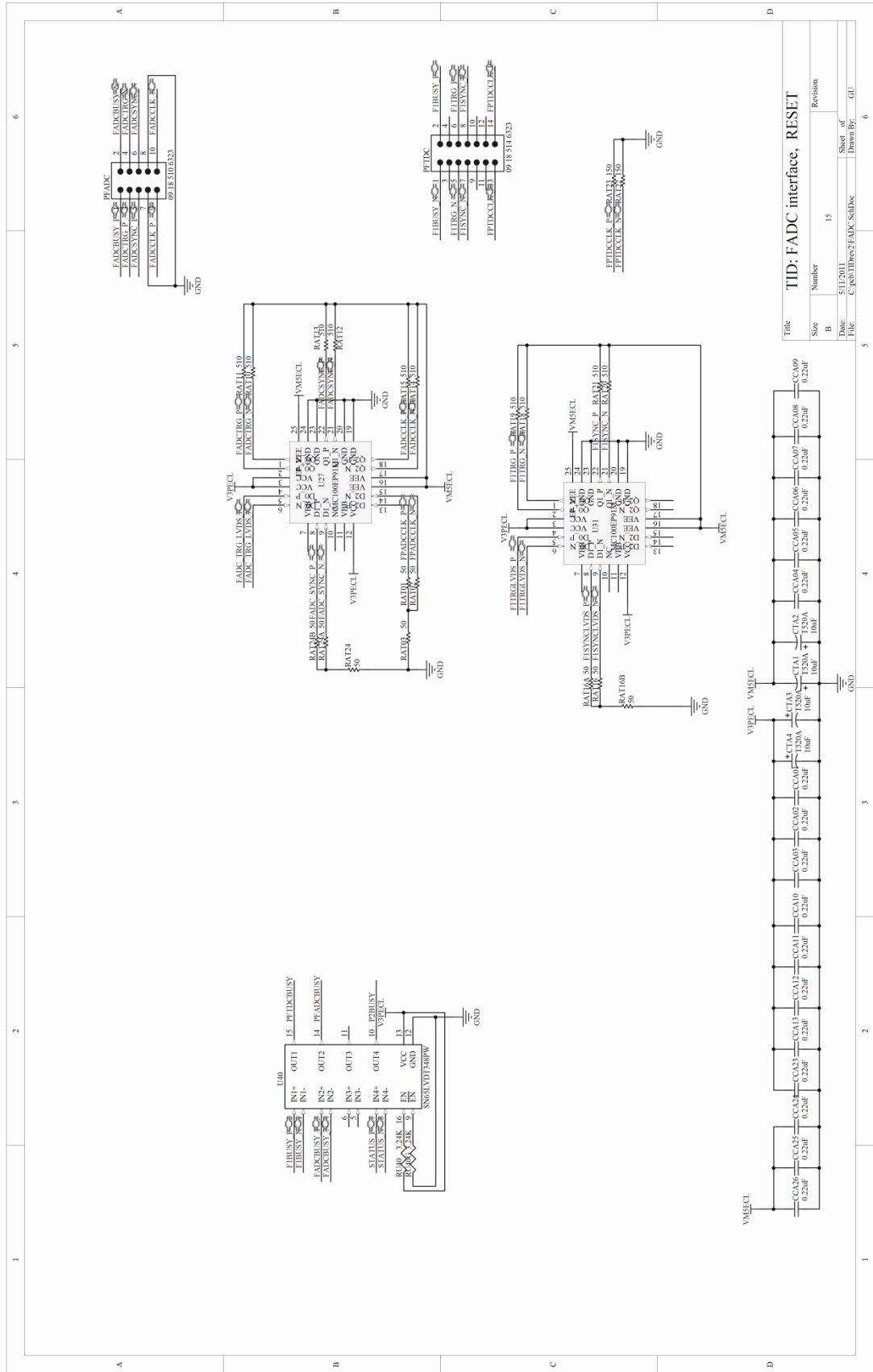


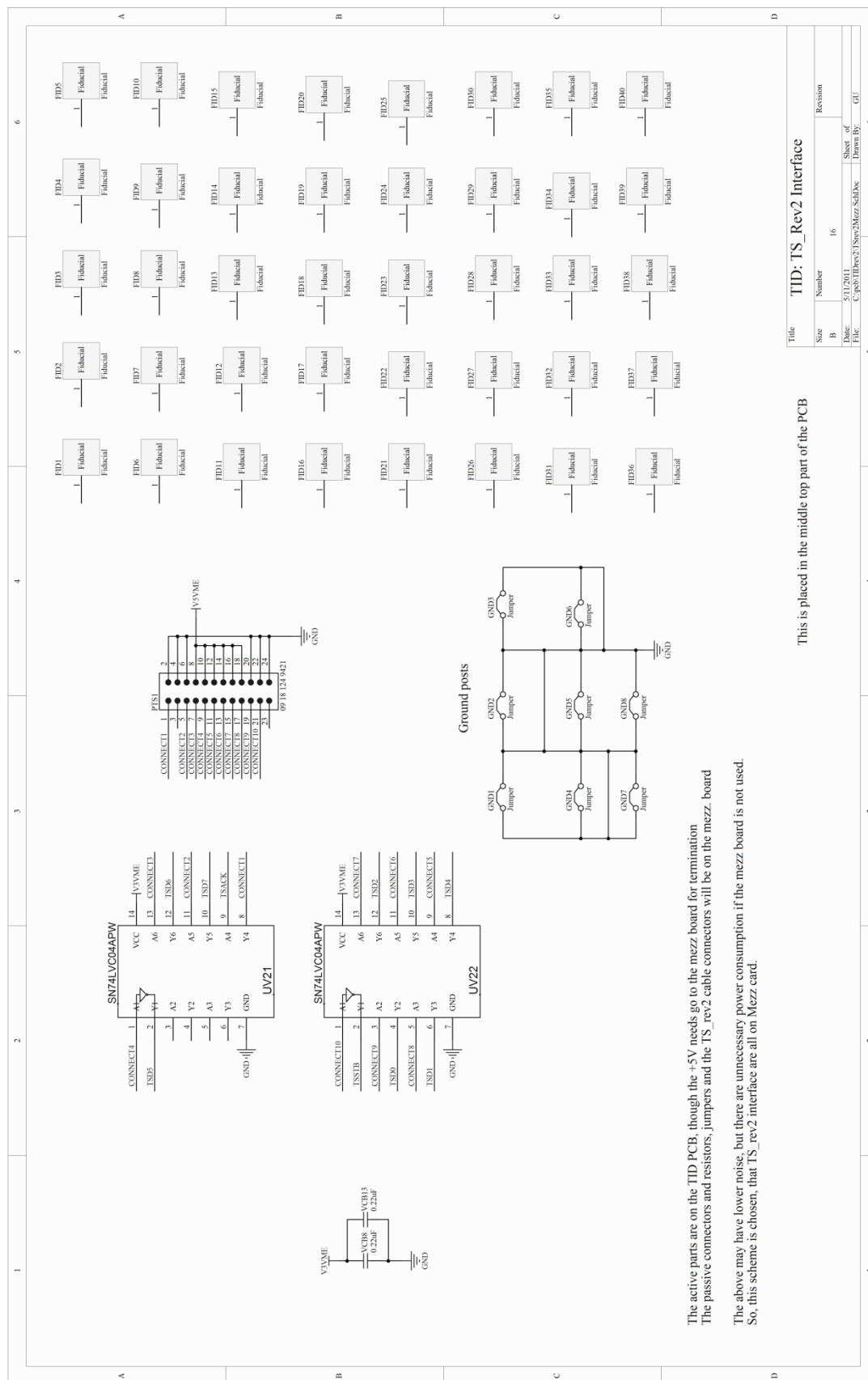
TID: Clock Distribution

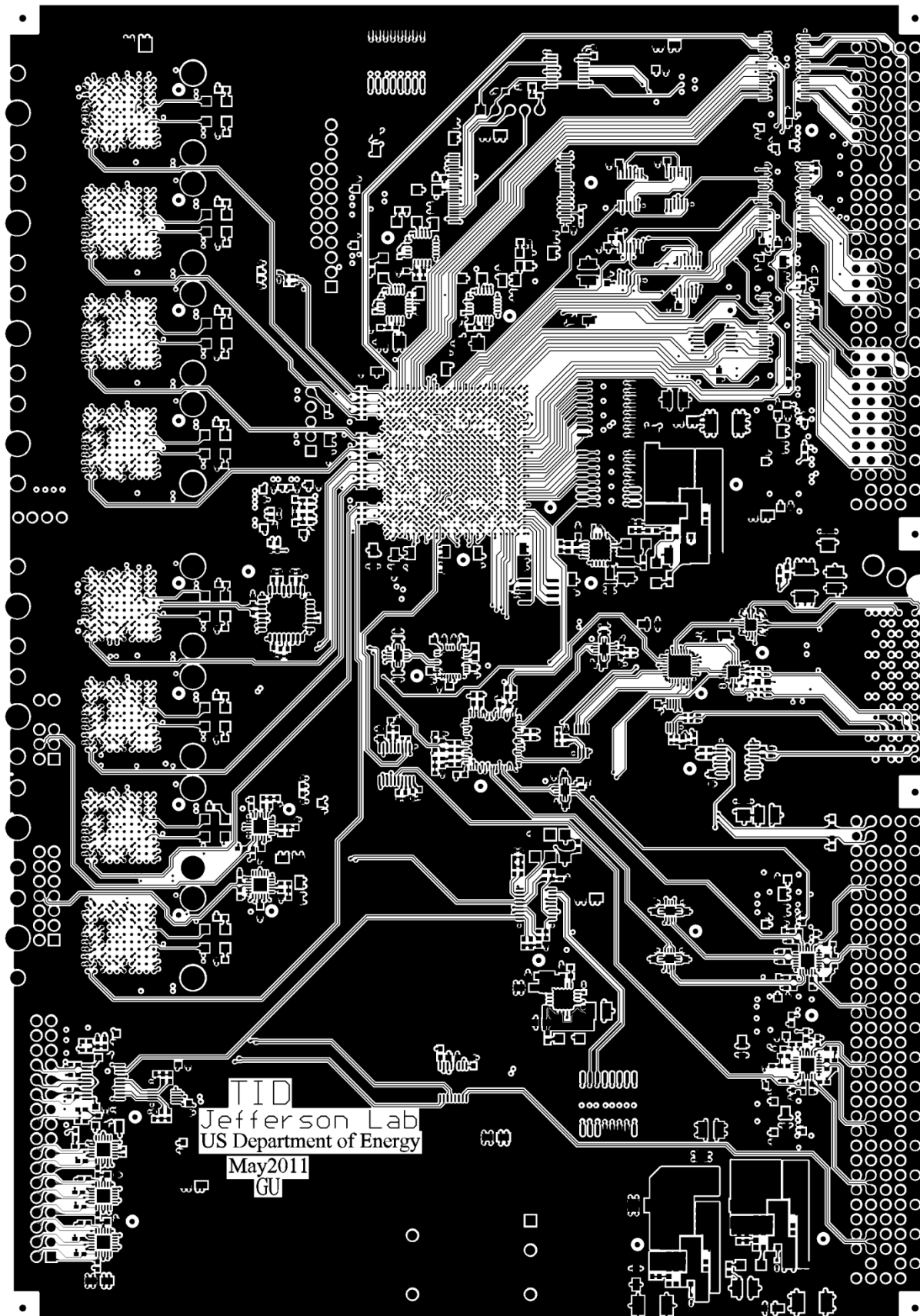
Title	Size	Number	Revision
B	12		
Time: 01/2001			
File: C:\P1\Brow2\ClockDist.SchDoc		Sheet 2 of 6	GI

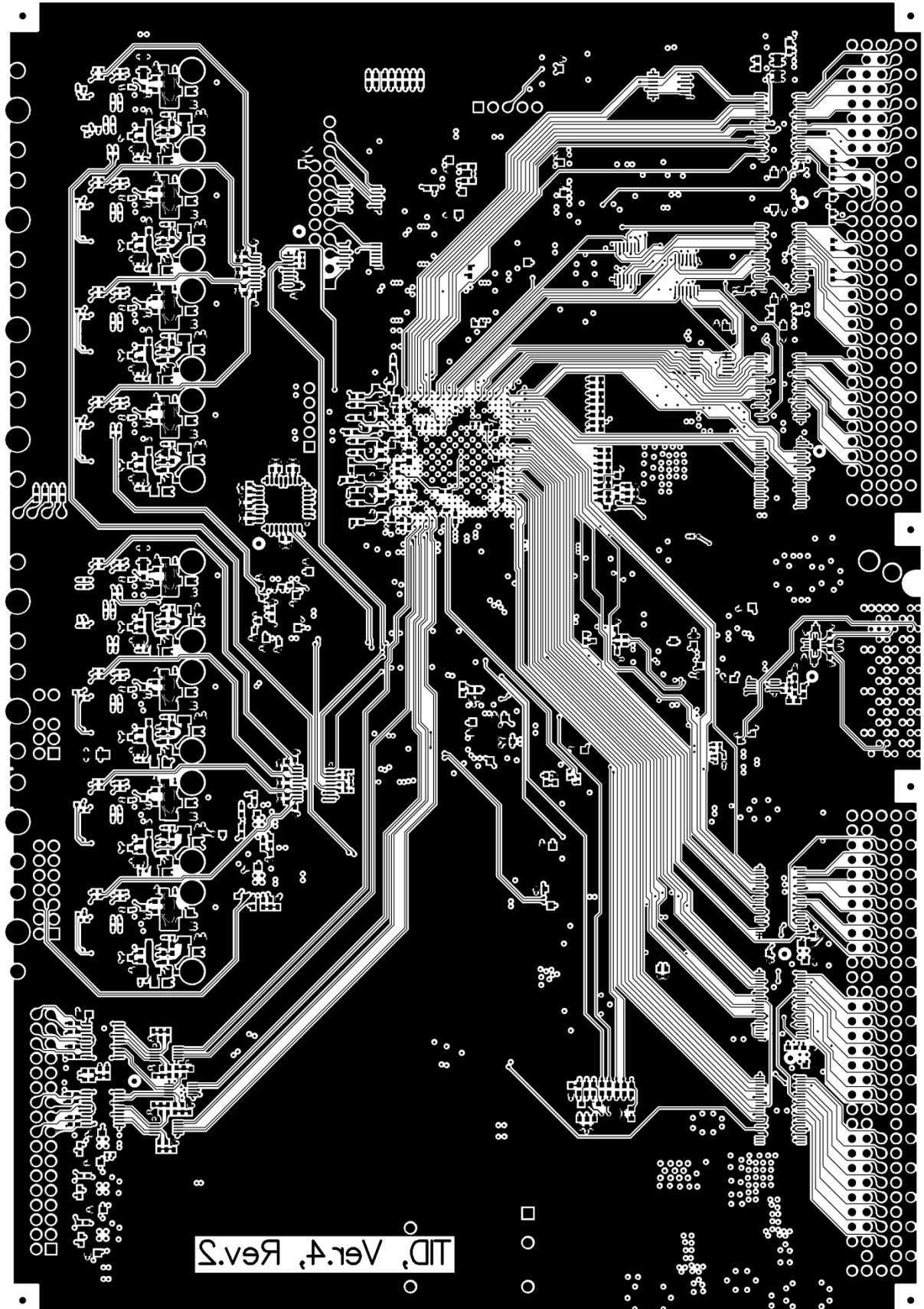












Appendix C: Bill of materials:

Component list

Source Data From:

Project:

Variant:

Report

Date: 5/12/2011

Print Date: 12-May-11

Description	Footprint	Quantity	Designator
Capacitor	0402	11	C0001, C0002, C0003, C0004, C0007, C0008, C0013, C0014, C0017, C0018, CUC04A
Capacitor (Semiconductor SIM Model)	1608[0603]	28	C0005, C0006, CCL01, CCL02, CCL03, CCL04, CCL05, CCL06, CCL07, CCL08, CCL09, CCL11, CCL12, CCL13, CCL14, CCL15, CCL16, CCL17, CCL18, CP01, CP02, CP03, CP04, CP05, CP06, CP07, CUP07A, CUP07B
Capacitor, Capacitor (Semiconductor SIM Model)	0402	121	C9510A, C9510B, C9510C, C9510D, CCAU1, CCAU2, CCAU3, CCAU4, CCAU5, CCAU6, CCAU7, CCAU8, CCF01, CCF02, CCF03, CCF04, CCF11, CCF12, CCF13, CCF14, CCF15, CCF16, CCF17, CCF18, CCF21, CCF22, CCF23, CCF24, CCF25, CCF26, CCF27, CCF28, CCF31, CCF32, CCF33, CCF34, CCF35, CCF36, CCF37, CCF38, CCF41, CCF42, CCF43, CCF44, CCF45, CCF46, CCF47, CCF48, CCF51, CCF52, CCF53, CCF54, CCF55, CCF56, CCF57, CCF58, CCF61, CCF62, CCF63, CCF64, CCF65, CCF66, CCF67, CCF68, CCF71, CCF72, CCF73, CCF74, CCF75, CCF76, CCF77, CCF78, CCF81, CCF82, CCF83, CCF84, CCF85, CCF86, CCF87, CCF88, CCF101, CCF102, CCF103, CCF104, CCF119, CCF129, CCF139, CCF149, CCF159, CCF169, CCF179, CCF189, CCLK04, CCLK05, CCT11, CCT12, CFB21, CFB22, CFB31, CFB32, CFB41, CFB42, CFB61, CFB62, CFB71, CFB72, CFB81, CFB82, CGTP1, CGTP2, CU201, CU202, CU203, CU204, CU205, CU206, CU207, CU208, CUC04, CUC08A, CUC08B

Capacitor, Ceramic Chip Capacitor - Standard	0603	143	CCA01, CCA02, CCA03, CCA04, CCA05, CCA06, CCA07, CCA08, CCA09, CCA10, CCA11, CCA12, CCA13, CCA23, CCA24, CCA25, CCA26, CCE01, CCE02, CCE03, CCE04, CCE05, CCE06, CCE08, CCE09, CCE10, CCF111, CCF112, CCF114, CCF115, CCF117, CCF118, CCF121, CCF122, CCF124, CCF125, CCF127, CCF128, CCF131, CCF132, CCF134, CCF135, CCF137, CCF138, CCF141, CCF142, CCF144, CCF145, CCF147, CCF148, CCF151, CCF152, CCF154, CCF155, CCF157, CCF158, CCF161, CCF162, CCF164, CCF165, CCF167, CCF168, CCF171, CCF172, CCF174, CCF175, CCF177, CCF178, CCF181, CCF182, CCF184, CCF185, CCF187, CCF188, CCPG1, CCPG2, CCPG3, CCPG4, CCPG5, CCPG6, CCPG7, CCPG8, CCPG92, CCSE01, CCSE02, CCSE03, CCSE04, CCSE05, CCSE06, CCSE07, CCSE08, CCSE08x, CCSE09, CCSE11, CCSE12, CCSE13, CCV01, CCV02, CCV03A, CCV04, CCV05, CCV06, CCV07, CCV08, CCV09, CCV10, CCV11, CCV12, CCV13, CCV14, CCV15, CCV21, CCV22, CCV23, CCV33, CCV36, CCV37, CCV38, CCV39, CCV40, CVUC04A, CVUC04B, VCB1, VCB2, VCB3, VCB4, VCB5, VCB6, VCB7, VCB8, VCB9, VCB10, VCB11, VCB12, VCB13, VCB14, VCB15, VCB16, VCB17, VCB18, VCB19, VCB29, VCB39
Capacitor, Capacitor (Semiconductor SIM Model)	0402	18	CCCF1, CCCF2, CCCFix, CCCFS, CCGT, CCP1, CCP1_NL, CCP2, CCP3, CCP3_6, CCP4, CCP6, CCPGTP4, CCUI01, CCUI02, CCUI03, CUF12BB, CUF13BB
Solid Tantalum Chip Capacitor, Standard T491 Series - Industrial Grade	A	71	CP1, CP6, CP9, CP9A, CP9B, CP9C, CP9D, CP9E, CP10, CP11, CP95x, CPE1, CPE2, CPF11, CPF12, CPF13, CPF14, CPF22, CPF23, CPF24, CPF32, CPF33, CPF34, CPF42, CPF43, CPF44, CPF51, CPF52, CPF53, CPF54, CPF62, CPF63, CPF64, CPF71, CPF72, CPF73, CPF74, CPF82, CPF83, CPF84, CPL02, CPL03, CPL04, CPL05, CPL06, CPL07, CPL08, CPL09, CPL10, CPL11, CPL12, CPL13, CPL14, CPL15, CPV1, CPV2, CPV3, CPV4, CPV35, CPV36, CTA1, CTA2, CTA3, CTA4, CTPG1, CTPG2, CTSC1, CTSC2, CTSC3, VCA1, VCA2
Solid Tantalum Chip Capacitor, Standard T491 Series - Industrial Grade, Solid Tantalum Chip Capacitor, Standard T520 Series - Industrial Grade	B	9	CP2, CP3, CP4, CP5, CP7, CP7X, CP20, CPL01, CPL20
Solid Tantalum Chip Capacitor, Standard T491 Series - Industrial Grade	B	1	CP5_NL
Typical RED, GREEN, YELLOW, AMBER GaAs LED	3.2X1.6X1 .1	24	DF11, DF12, DF21, DF22, DF31, DF32, DF41, DF42, DF51, DF52, DF61, DF62, DF71, DF72, DF81, DF82, DP1, DP2, DP3, DP3_4, DP4, DP5, DPG1, DPG5
	EC5BE17	1	EC34
FUSE 5A SLO BLO NANO 2 SMD	NANO_F USE	3	F5, F12, F15
	fiducial	40	FID1, FID2, FID3, FID4, FID5, FID6, FID7, FID8, FID9, FID10, FID11, FID12, FID13, FID14, FID15, FID16, FID17, FID18, FID19, FID20, FID21, FID22, FID23, FID24, FID25, FID26, FID27, FID28, FID29, FID30, FID31, FID32, FID33, FID34, FID35, FID36, FID37, FID38, FID39, FID40

FUSE 5A SLO BLO NANO 2 SMD	NANO_F USE	1	FP1
Header, 6-Pin	HDR1X6	2	FPGA_JTAG, PROM_JTAG
Jumper Wire	RAD-0.2	8	GND1, GND2, GND3, GND4, GND5, GND6, GND7, GND8
Flat Cable Connector (IDC), Low-Profile Male Header, Angled Solder Pin, 34 Contacts, Performance Level 2	918534x3 23	1	JC1
INDUCTOR 1.0UH 300MA 20% 0805	0805	24	LF11, LF13, LF15, LF21, LF23, LF25, LF31, LF33, LF35, LF41, LF43, LF45, LF51, LF53, LF55, LF61, LF63, LF65, LF71, LF73, LF75, LF81, LF83, LF85
INDUCTOR 6.8NH 10% 0603 SMD	0603	24	LF12, LF14, LF16, LF22, LF24, LF26, LF32, LF34, LF36, LF42, LF44, LF46, LF52, LF54, LF56, LF62, LF64, LF66, LF72, LF74, LF76, LF82, LF84, LF86
Inductor	L0603	17	LL01, LL02, LL03, LL04, LL05, LL06, LL07, LL08, LL09, LL11, LL12, LL13, LL14, LL15, LL16, LL17, LL18
Inductor	1210	9	LP1, LP2, LP3, LP4, LP5, LP10, LP11, LP20, LP33
VME160-P1	VME160	1	P1
VME160-P2	VME160	1	P2
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W, Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	2-0402	45	P2R1, P2R2, P2R3, P2R4, P2R5, P2R6, P2R7, P2R8, P2R9, P2R10, P2R11, P2R12, RAT10, RAT11, RAT12, RAT13, RAT14, RAT15, RAT18, RAT19, RAT20, RAT21, RCT41X, RIO11, RIO12, RIO13, RIO14, RIO15, RIO16, RIO17, RIO18, RIO21, RIO22, RIO23, RIO24, RIO25, RIO26, RIO27, RIO28, RP12, RP12x, RP16, RPG12, RPG12x, RST99X
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W, Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	2-0402	112	P2R21, P2R22, P2R23, P2R24, P2R25, P2R26, P2R27, P2R28, P2R29, P2R30, P2R31, P2R32, P2R33, P2R34, P2R35, P2R36, P2R37, P2R38, RAT01, RAT02, RAT03, RAT16, RAT16A, RAT16B, RAT24, RAT24A, RAT24B, RC20, RC30, RC30a, RC31, RC32, RC33, RC43, RC44, RC46, RC47, RC48, RC48a, RC49, RC101, RCT17, RCT18, RCT19, RCT30, RCT31, RCT32, RCT43, RCT44, RCT45, RCT48, RCT49, RIO1, RIO2, RIO3, RIO4, RIO5, RIO6, RIO7, RIO8, RIO9, RIO31, RIO32, RIO33, RIO34, RIO35, RIO36, RIO37, RIO38, RIO39, RIO41, RIO42, RIO43, RIO44, RIO45, RIO46, RIO47, RIO48, RIO51, RIO52, RIO53, RIO54, RIO55, RIO56, RIO57, RIO58, RIO61, RIO62, RIO63, RIO64, RIO65, RIO66, RIO67, RIO68, RST31, RST31A, RST32, RST155, RST156, RST157, RST158, RST159, RST160, RT1, RT2, RT3, RT4, RT5, RUC04, RVP0, RX02, RX02F
Flat Cable Connector (IDC), Low-Profile Male Header, Angled Solder Pin, 10 Contacts, Performance Level 2	918510x3 23	1	PFADC
Flat Cable Connector (IDC), Low-Profile Male Header, Angled Solder Pin, 14 Contacts, Performance Level 2	918514x3 23	1	PFTDC
P0-PL-VXS	P0-105_P0-	1	PP0

	PL-VXS		
Flat Cable Connector (IDC), PCB Transition Connector, 2 Rows, Kinked Solder Pin, 24 Contacts	91812494 21	1	PTS1
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W, Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	2-0402	80	RAT22, RAT23, RC11, RC12, RC13, RC14, RC15, RC16, RC17, RC18, RC19, RC21, RC22, RC23, RC24, RC25, RC26, RC27, RC28, RC29, RCT46, RCT47, RCT51, RCT51A, RCT51B, RCT52, RCT52A, RCT52B, RF90, RF91, RF92, RF93, RF94, RF95, RF96, RF97, RF98, RF99, RF101, RF102, RF103, RF104, RF105, RF106, RF107, RF108, RF109, RF110, RP6y, RPG8, RST33, RST34, RST35, RST36, RST37, RST38, RST39, RST40, RST41, RST42, RST43, RST44, RST45, RST46, RST47, RST48, RST49, RST50, RST101, RST102, RST103, RST104, RST151, RST152, RST153, RST154, RUP06A, RUP06B, RUP06C, RUP06D
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W, RES 100 OHM 1/16W 1% 0402 SMD, Resistor	0603	85	RC01, RC06, RC07, RC08, RCT42X, RCTR2A, RCTR3A, RCTR3B, RCX01, RCX02, RCX03, RCX04, RCX09, RCX10, RCX11, RE01X, RE06X, RF11, RF12, RF14, RF16, RF18, RF21, RF22, RF24, RF26, RF28, RF31, RF32, RF34, RF36, RF38, RF41, RF42, RF44, RF46, RF48, RF51, RF52, RF54, RF56, RF58, RF61, RF62, RF64, RF66, RF68, RF71, RF72, RF74, RF76, RF78, RF81, RF82, RF84, RF86, RF88, RI2C1, RI2C2, RI2C3, RI2C4, RI2C5, RI2C6, RP3_14, RP4, RP6, RP6x, RP9y, RP11, RP13, RP14, RP15, RPG11, RPG13, RS16, RS17, RS18, RS21A, RS22A, RS23A, RS24A, RST99D, RV02xy, RV04X, RV12xy
Resistor	0603	88	RC02, RC03, RC04, RC05, RCT50A, RCTR1, RCTR2, RCTR3, RCX05, RCX06, RCX07, RCX08, RCX12, RCX13, RCX14, RE01, RP2, RP3, RP3_15, RP3_16, RP3NL, RP3NLA, RP3x, RP5, RP9, RP9z, RP10, RP101, RP102, RP103, RP104, RP105, RP106, RP107, RP108, RP109, RP110, RP111, RP112, RPG2, RPG3, RPG4, RPG5, RPG6, RPG7, RPG9, RPG10, RPG11A, RPGCLK3, RS1, RS2, RS3, RS4, RS5, RS6, RS7, RS8, RS11, RS12, RS13, RS14, RS15, RS21, RS22, RS23, RS24, RS25, RS26, RS27, RS28, RTS19, RU40, RU40G, RUSFM, RV01, RV01x, RV02, RV02x, RV03, RV04, RV05, RV05x, RV07, RV07A, RV08, RV12x, RV12yz, RV44
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W	0402	8	RCT09, RCT10, RCT11, RCT12, RCT13, RCT14, RCT15, RCT16
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W, RES 100 OHM 1/16W 1% 0402 SMD, Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	0402	16	RCT41, RCT42, RGT1, RGT2, RST99B, RST99C, RTD0x, RTD01, RTD02, RTD03, RTD04, RTD05, RTD05X, RTD06, RTD07, RTD08

Resistor	0603	1	RE05X
RES 100 OHM 1/16W 1% 0402 SMD, Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	0402	32	RF13, RF15, RF17, RF23, RF25, RF27, RF33, RF35, RF37, RF43, RF45, RF47, RF53, RF55, RF57, RF63, RF65, RF67, RF73, RF75, RF77, RF83, RF85, RF87, RIO19, RIO29, RST16, RST99, RST99A, RT4A, RT4B, RT4C
Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	0402	6	RID01, RID02, RID03, RID04, RPGCLK_NL, RPGD01_NL
Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	0402	8	RID11, RID12, RID13, RID14, RID15, RID16, RPGCLK2, RPGD02
Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	2-0402	4	RIO33x, RIO33y, RIO33z, RUC04A
DIP Switch, 8 Position, SPST	SW16_L	4	S1, S2, SC01, SC1
AD9510	CP-64-1_N	1	U13
IC 11-BIT I-WS BUS TXRX 48-TSSOP	TSSOP50 P810-48AL	1	U17
Xilinx Virtex-5 LXT Platform FPGA, 665-Ball FFBGA, Speed Grade 1, 360 User I/Os, Commercial Grade	FF665	1	U20
On Semiconductor, Any level positive to ECL translator	QFN50P4 00X400-24W4M	7	U27, U31, UIO4, UIO5, UIO6, UVP21, UVP22
4 Channel ECL/PECL/LVDS - > LVTTTL	TSSOP-16	1	U40
CCPD-034	SO6-5X7	1	UC01
Any level in, LVPECL out 1:2 fanout	QFN50P3 00X300-16V7N	6	UC04, UC04A, UC05, UC06, UF11, UP06
4:1 Differential Multiplexer	948E-02_L	1	UC07
ON-Semi Dual 2 X 2 CrossSwitch	RHB32_N	1	UC08
2x2 crosspoint switch with LVPECL output	QFN50P3 00X300-16V4N	2	UC10A, UC10B
Micrel dual Anylevel to LVPECL translator	TSSOP50 P490-10AN	1	UC14
Low-Voltage 1:10 Differential LVECL/LVPECL/LVEPECL/H STL Clock Driver	873A-02_L	2	UC15, US8
Differential to CML buffer	846A-02	1	UC17

	TSSOP14	4	UE01, UE02, UE07, UE08
	TSSOP14	2	UE03, UE05
	TSSOP14	2	UE04, UE06
	TSSOP14	3	UE09, UV21, UV22
	TSSOP20	1	UE10
HFBR7934	84512-102LF	8	UF1, UF2, UF3, UF4, UF5, UF6, UF7, UF8
Low-Voltage 1:5 Differential LVECL/LVPECL/LVEPECL/H STL Clock Driver	948E-02_N	4	UF12, UF13, US4, UT1
Triple ECL to PECL Translator	948E-02_N	3	UIO1, UIO2, UIO3
Dual LVPECL to LVDS translator	TSSOP50 P490-10AN	5	UIO7, UIO8, UIO9, UIO10, US1
LUMEX, Quad pack LEDs	LED14	1	ULED
LTM4604EV	LGA-66_LTM4604EV(Pri mary)	3	UP1, UP1_NL, UP3
IC LDO REG 3.0A W/SS 20-VQFN	QFN-20	5	UP2, UP4, UP5, UP33, UPG5
Analog 1.25Gbps Clock and Data Recovery IC	QFN50P500X500-32W2N	1	UP07
Miniature Oscillator	CFPX-5	1	UPG1
XCF00P Series, Platform Flash In-System Programmable Configuration 1.8V PROM, 48-Pin TSSOP, 32-Megabit, Commercial Grade	VO48	1	UPG2
Atmel flash memory	8S1_N	1	USFM
IC UNIV BUS TXRX TRI-ST 48-TSSOP	TSSOP50 P810-48AL	9	UV1, UV2, UV3, UV4, UV5, UV6, UV10, UV12, UV14

Appendix D: Glossory:

TID: Trigger Interface and Distribution module; a PCB design can be configured as TI, TD, TS or TM;

TI: Trigger Interface module; It seats in payload slot#18 in front end crates, interfaces the trigger and the DAQ system; It is one stuffing variation of the TID.

TD: Trigger Distribution module; It seats in payload slot#1-16 in the global trigger distribution and fans out the TRIGGER/CLOCK/SYNC to eight TIs; it is one stuffing variation of the TID.

TS: Trigger Supervisor; It seats in payload#18 in the global trigger distribution crate; It is the interface between DAQ and trigger system; A simplified (pre-prototype) TS can be stuffed from a TID;

TM: TID Master. It is used in the subsystem test or commissioning setup; It generates TRG/CLK/SYNC as a TS, sends TRG/CLK/SYNC to P0 and P2 like a TI, and fans out TRG/CLK/SYNC through fiber to other TI like a TD.

SD: Signal Distribution module; It fans out TRG/CLK/SYNC from payload slot#18 to payload slots#1-16; It has clock jitter cleanup capability.

GTP: Global Trigger Processor module.

CTP: Crate Trigger Processor module.

DAQ: Data Acquisition.

ROC: Readout Controller; A VME CPU module used to readout the front end data through VME bus.

VXS: VME Switched Serial; A VME extension with dual-star serial switch slots.

MGT: Multiple Gbps Transceiver; A builtin transceiver module in Xilinx FPGA. In XC5VLX30T FPGA, it supports up to 3.125 Gbps.

Appendix E: TID data format:

The TID data is formatted in blocks of events. Each Trigger_1 is one event. A block of data contains a predefined number (the number could be 1) of triggers. Each block has block header, block trailer, possible place holder, and event data. The data format is summarized here:

Block headers
Event#1 data
Event#2 data
.....
Event#N data
Optional data
Block trailer

Block Header#1:

bit(31:28): 0001;
Bit(27:22): CrateID, which is set by register A24 offset 0x00;
Bit(21:16): BoardID, the VME64x geographic address;
Bit(15:8): block number;
Bit(7:0): block size;

Block Header#2:

Bit(31:8): 0x0f0120;
Bit(7:0): Block size;

Block Trailer#1:

Bit(31:28): 0010;
Bit(27:16): floating, I guess that they default to 0;
Bit(15:0): Word count; as suggested by Dave, some data do not count.

Extra word:

0xF0DA0BAD

Dummy word:

bit(31:16): 0x965A;
Bit(15:0): Block number

Event data word1: (event header)

Bit(31:24): Trigger Type;
Bit(24:2): 0000,0001,0000,0000,0000,00
Bit(1:0): Event wordcount; as suggested by Dave, some data do not count

Event data word2:

Bit(31:0): trigger number; counting from 0 to be consistent with wrap around;

Event data word3:

Bit(31:0): trigger timing; 16ns step

Event data word4:

Bit(31:16): Current trigger data (received data from fiber trigger_link as TI);
Bit(15:0): Current trigger data (sent data from fiber trigger_link as TS)

Appendix F: Document revision history:

Updated on Apr. 20th, 2010

Updated on May 13th, 2010

Updated on May 19th, 2010: add the trigger acknowledge in the status word;

Updated on July 6th, 2010: Define the TI/TD mode in section 5.2.2;

Updated on Sept. 20th, 2010: Re-define the A24 address space;

Updated on Oct. 15th, 2010: Added Busy_Input_Enable (A24, 0x0004);

Updated on Oct. 18th, 2010: updated the Emergency loading after tests;

Updated on Jan. 13th, 2011: Add examples for VME trigger word loading;

Updated on Feb. 2nd, 2011: clarify the A24 0x00-0x1C registers;

Updated on Mar. 21st, 2011: further updates on registers to match with the firmware;

Updated on Mar. 25th, 2011: Added the software setup procedure section, with some updates on the registers;

Updated on Apr. 5th, 2011: Register offset 0x14 and 0x2C update.

Updated on Apr. 18th, 2011: Enables for each GTP input bits, CLK250 source selection

Updated on Apr. 20th, 2011: added the Sync decoding, and two more A24 read registers;

Updated on May 12th, 2011: Added the PCB schematics, fab layers, and BOM as appendix A, appendix B and appendix C.

Updated on June 6th, 2011: Added A24 offsets 0x38 and 0x3C for extra readout (v10)

Updated on June 22nd, 2011: Redefined A24, 0x08 and 0x30 registers;

Updated on Aug. 18th, 2011: Overall revision to add the TM description, Glossary and data format;

Updated on May 31st, 2012: expanded the trigger rule bits from 5 to 7 bits;

Updated on Oct. 12, 2012: Separated from TID, updated to the new register map;

Updated on Sept. 13, 2013: updated the register offset 0x04, 0xB0;

Updated on Oct. 17, 2013: updated register offset 0x14 and 0x78;

Updated on Dec. 3, 2013: Added register offsets 0xD0 – 0xEC. Moved the original 0xD0 to 0x90

Updated on Jan. 6, 2015: use A24 offset 0x28 bit 6 to enable trigger acknowledge BUSY. Bit#22 is used to monitor the ‘trigger loss’ (trigger is sent out, but the trigger acknowledge has not been received)

Updated on Feb. 22, 2016: Updated the register 0x04 for AFBR-79EIDZ optic transceivers; added 0x5XXXX for AFBR-79EIDZ I2C interface; 0x0DC00-0x0DDFC for virtex-5 system monitor registers.

Updated on Feb. 23, 2016: added register 0x19C-0x1BC for individual TI busy scalars.

Updated on Apr. 7, 2016: Added the front panel differential signal outputs (section 4.4).

Updated on June 14, 2016: Move registers 0xD0-0xEC to 0x1D0-0x1EC (Undo the changed in Dec. 3rd 2013) for TI busy counters. Remove the **RED** marded register. Now, the registers are very similar to that of the TImaster. This leaves the potential to use the TD as sub-system TImaster, though some register functions have not been implemented or tested yet. Merge with TD_common.docx.

Updated on July 13, 2016: updated some of the registers, esp. 0x98 etc.