Nuclear Physics Division
Fast Electronics Group

Description and Technical Information
for the
VXS Signal Distribution Module

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Fast Electronics Group
Jefferson Lab

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1.0 Introduction

The VME Switched Serial (VXS) base standard defines the physical arrangement of the VXS payload slots and the switch slot as a redundant star (see figure 1). Each payload slots has 8 differential pairs and two single-ended connections to the "A" and "B" switch slots. The Signal Distribution Board (SD) module occupies the "B" switch card slot as specified in VITA 41.The main purpose of this module is to distribute signals received from payload slot 18 (Trigger Interface board) of a VXS crate to 16 other payload slots (ADC boards).

The Signal Distribution (SD) module distributes the 4 differential pair LVPECL signals from payload slot 18 to 16 VXS payload slots within the crate. This is done using the high speed point to point connections from the switch slot to each payload slot. The four signals distributed are length matched to minimize output jitter seen on all the payload slots. Three of the four remaining pairs are LVDS signals routed from the each payload module to the FPGA on the SD module. The last pair is an LVDS signal routed from the FPGA on the SD module to each payload module. Each of the 16 payload modules has a single-ended signal to the SD module and one from the SD module back to the payload module.

A Jefferson Lab VXS crate will be configured to use up to eighteen (18) payload slots. Payload slot 17 is reserved for the CPU and slot 18 is used for the Trigger interface board.
The distribution of the remaining 16 slots can be such that:

a) Each half of the crate can hold eight: FADC-250, ADC125 or F1TDC boards.
b) All 16 payload slots can be populated with boards of the same type.

The switch slots are connected to each payload slot in a VXS crate. There are no inter-slot connections between the payload slots, therefore any inter-slot communication is handled by the Switch module. Therefore, in addition to using Switch B for signal distribution, other secondary functions of the Signal Distribution module are:

a) Managing payload module access to the VME bus (using the Token Passing scheme)]
b) Managing Intra-crate generated signals (i.e. collecting trigger and busy signals from the FADCs and passing them to the Trigger Interface board)
c) Providing a high speed link (approx 200Mbps) for data flow from the ADC module slots to the TI slot.

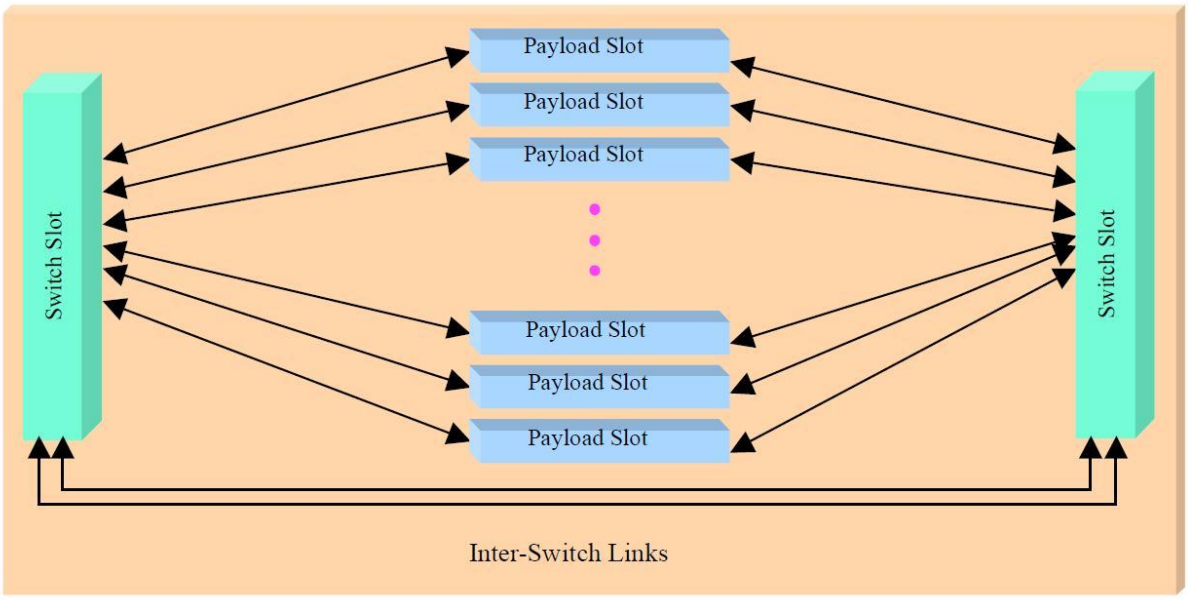


Figure 1-1 Redundant Star

Figure 1: Shows the Redundant Star configuration of the VXS crate.

2.0 Specifications Summary

MECHANICAL

- Single width VITA 41 "B" Switch Module

Front Panel:

- 5 – differential output ECL Signals
- 3 – Single-ended output LVPECL signals
- 2 – differential output LVPECL signals
- 2 – differential input LVPECL signals
- 1 - JTAG connector
- 1 - Active Serial connector
- 6 - Fault Indicator LEDs
- 1 - Reset Switch (momentary connect)

VXS OUTPUT SIGNALS

LVPECL level Signals (PP18 → PP[1 .. 16]):

- CLOCK
- SYNC
- TRIG1
- TRIG2

LVDS level Signals (PP[1 .. 16] → SD):

- SD_LINK
- TOKEN_IN
- TRIG_OUT

LVDS level Signals (PP18 → SD):

- TOKEN _OUT

LVDS level Signals (PP18 → SD):

- TOKEN _OUT

PROGRAMMING:

- Front Panel JTAG Port
- Front Panel Active Serial Port
- I^2C from Payload Port 18 (Trigger Interface)

POWER REQUIREMENTS:

- +5 V @ 8 amps Fused on board:
- local regulators for other required voltages

ENVIRONMENT:

- Forced air cooling.
- Commercial grade components (Celsius)

- Clock Jitter: (*to be tested)*
- Clock Signal Skew: (*to be tested)*

Power Section:

The switch slot in a VXS crate is powered by 5V (up to 40A). On the Signal Distribution board, most of the components are powered at 3.3V. The regulator used to provide the 3.3V is Linear Technology LTM4608 which can provide 8A of current at 3.3V. Other voltages required by the circuit are 2.5V and 1.2V, to provide power to the FPGA, these voltages are achieved by use of 1A linear regulators.
To terminate most of the LVPECL signals, 1.3V is provided by use of a linear regulator which can sink up to 2A. Addition of ECL signals required the use of an isolated power supply that provides -3.3V.

Total theoretical maximum current draw of the board is about 7A. The board is fused with 10A at the input and a reverse polarity diode protects the circuit from being damaged.

3.0 Functional Description [Block Diagram]

A VITA41 switch slot module is shown in Figure 2. Note the high speed multi-gigabit connectors (P1→P5) used for the point to point signals from payload modules to the switch card. The switch slot module only receives +5V power from the VXS backplane. Other voltages are generated using onboard voltage regulators. There are two mechanical alignment keys (K1 and K2) that are required to facilitate the proper mating between the board connectors and the backplane connectors. The switch board is a standard form factor of dimensions, 6U x 160mm x 4HP, as defined by IEEE 1101.1 standard.

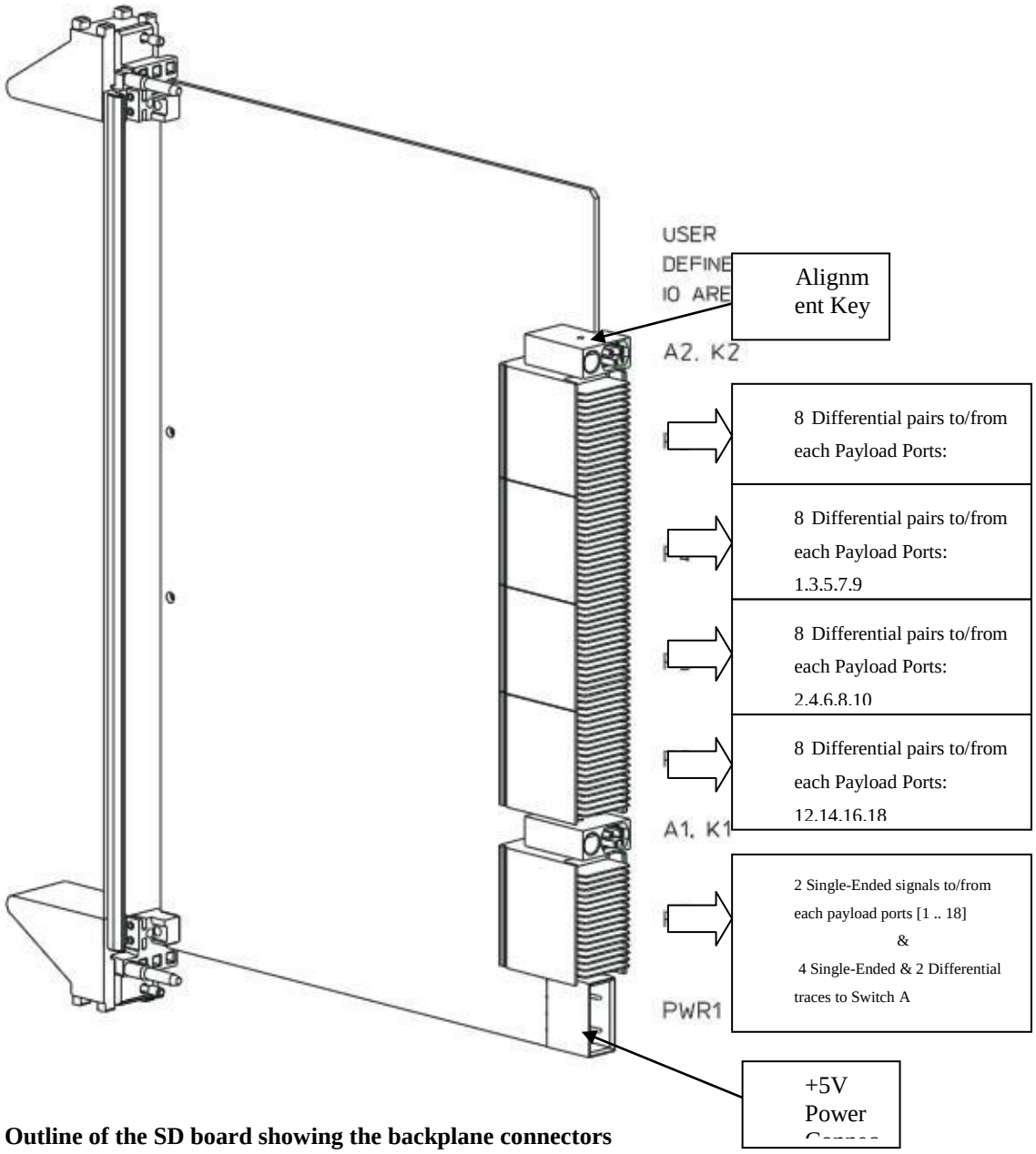


Figure 2. Outline of the SD board showing the backplane connectors

3.1: All Signals to/from the SD board.
Figure 3 below shows how the payload slots are logically connected to the "B" switch slot. The Signal Distribution module has been designed to accept all eight (8) differential pairs and two (2) single-ended from each payload port. The signal direction is defined by the user-defined function and the type of signal buffer (driver/receiver).

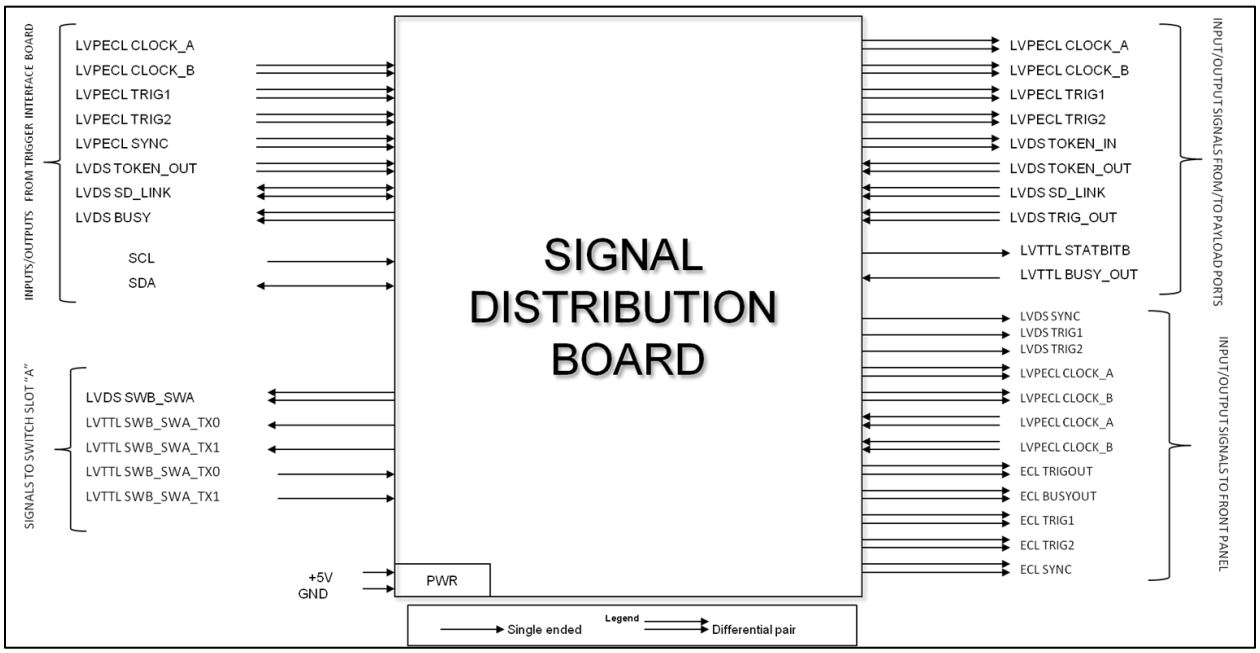


Figure 3 Shows the names and types of signals to/from the SD board

3.2: LVPECL Signals from the TI to Payload Boards via the SD board.
As shown in Figure 4 below the clock signals (ClockA and ClockB) from Trigger Interface board (PP18) are fanned out to drive the sixteen payload modules and Switch A (Crate Trigger Processor) module. To further reduce jitter on the clocks, a jitter attenuating PLL circuit is used before fanning out the signals to the payload slots. All the signals from the fanout buffer chip to the payload slot connectors are length matched to minimize device-to-device skew. CLOCKA and CLOCKB signals are 3000mils ± 10mils

ClockA and ClockB are independent and can therefore distribute different frequencies in the same crate. This makes it possible to populate the same front-end crate with different payload module types (e.g. FADC and TDC). Note also that it is possible to get a clock input from the front panel to be fanned out.

Trig1, Trig2 and Sync signals are received from the Trigger Interface board (PP18) and are fanned out to the sixteen payload modules. The signals can be distributed in two ways:

a) They can be registered to reduce skew between the clock and these signals. That means the signals can be delayed to be in sync with the clock edge before being fanned out.
b) They can also be unregistered which means that they can be fanned out as received from the payload port 18 (TI).

All the signal traces from the fanout buffers to the backplane are length-matched to minimize propagation delay and device to device jitter between the fanout buffer chip and the backplane connectors.

- TRIG1 signals are 4000mils ± 0.5%
- TRIG1 signals are 5000mils ± 0.5%
- TRIG2 signals are 6000mils ± 0.5%

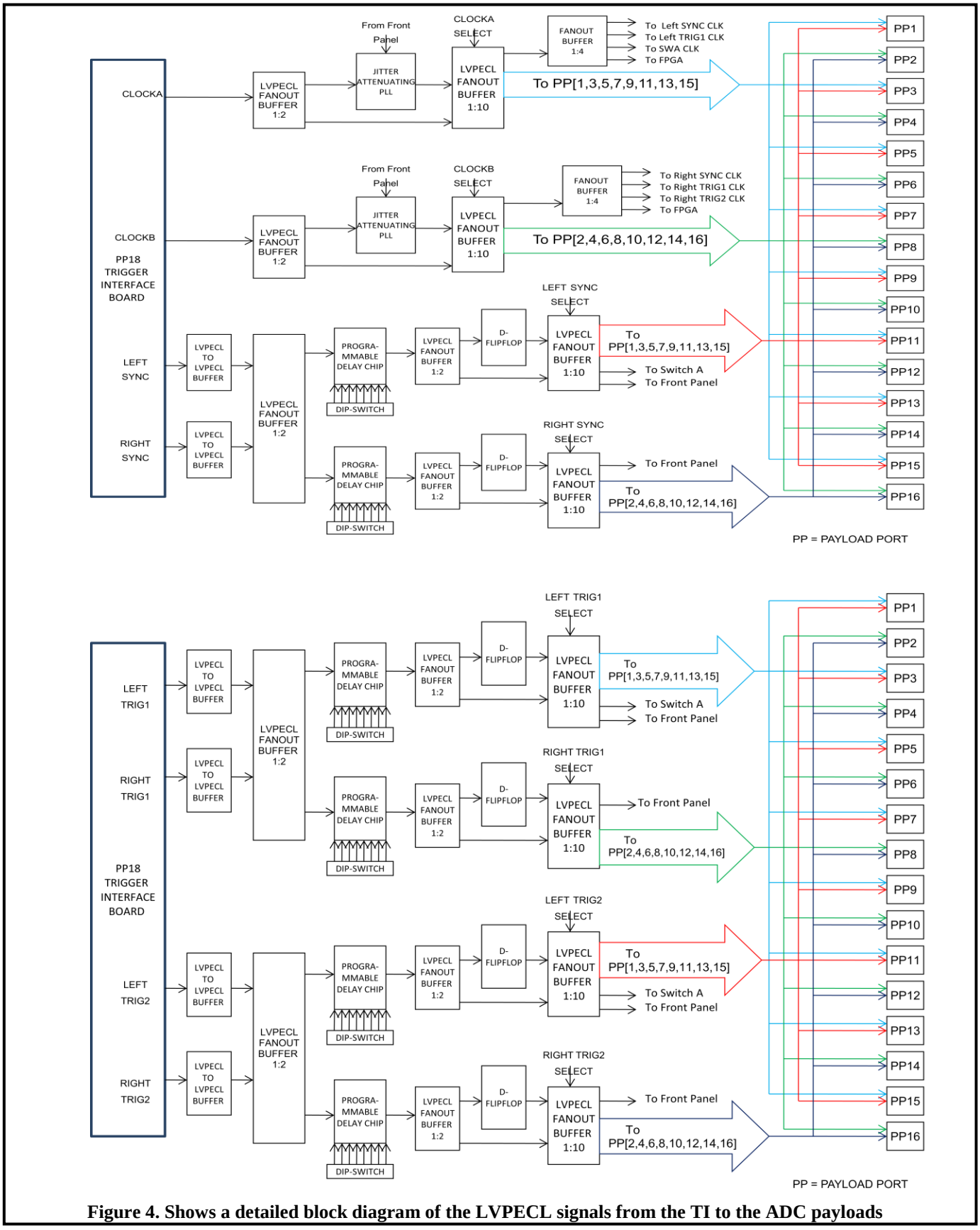


Figure 4. Shows a detailed block diagram of the LVPECL signals from the TI to the ADC payloads

3.3: LVDS Signals to/from the Payload Boards from/to the SD board.

Figure 5 shows other backplane signal pairs that the Signal Distribution module must manage. 3 LVDS inputs and 1 LVTTL input signal from each payload module and 1 LVDS and 1 LVTTL output signals to each payload module are connected to the FPGA.

The (3) LVDS input signals are:

i) SD_LINK: This connection is for high speed data transfer (200Mbps peak) from the PP[1 → 16] to the SD board.

ii) Token_IN: This connection receives the token from a payload board and sends the token to the next payload board in the token passing sequence. The token is used to prevent bus conflict therefore only the payload board that holds the token has access to read/write on the VME bus.

iii) Trig_OUT: This connection is for receiving FADC generated triggers.

The LVDS output signal is Token_OUT which sends out the token to the next payload in the token passing sequence.

The LVTTL input signal is Busy_Out which is asserted by a payload module when its data buffer is full. The signal is passed on to the TI module via the SD board.

The LVTTL output signal is StatBitB which can simultaneously send data to all 16 payload module or to individual payload modules.

All the LVDS signals are translated to LVTTL signals before connection to the FPGA; this was done to reduce the FPGA I/O pin requirement.

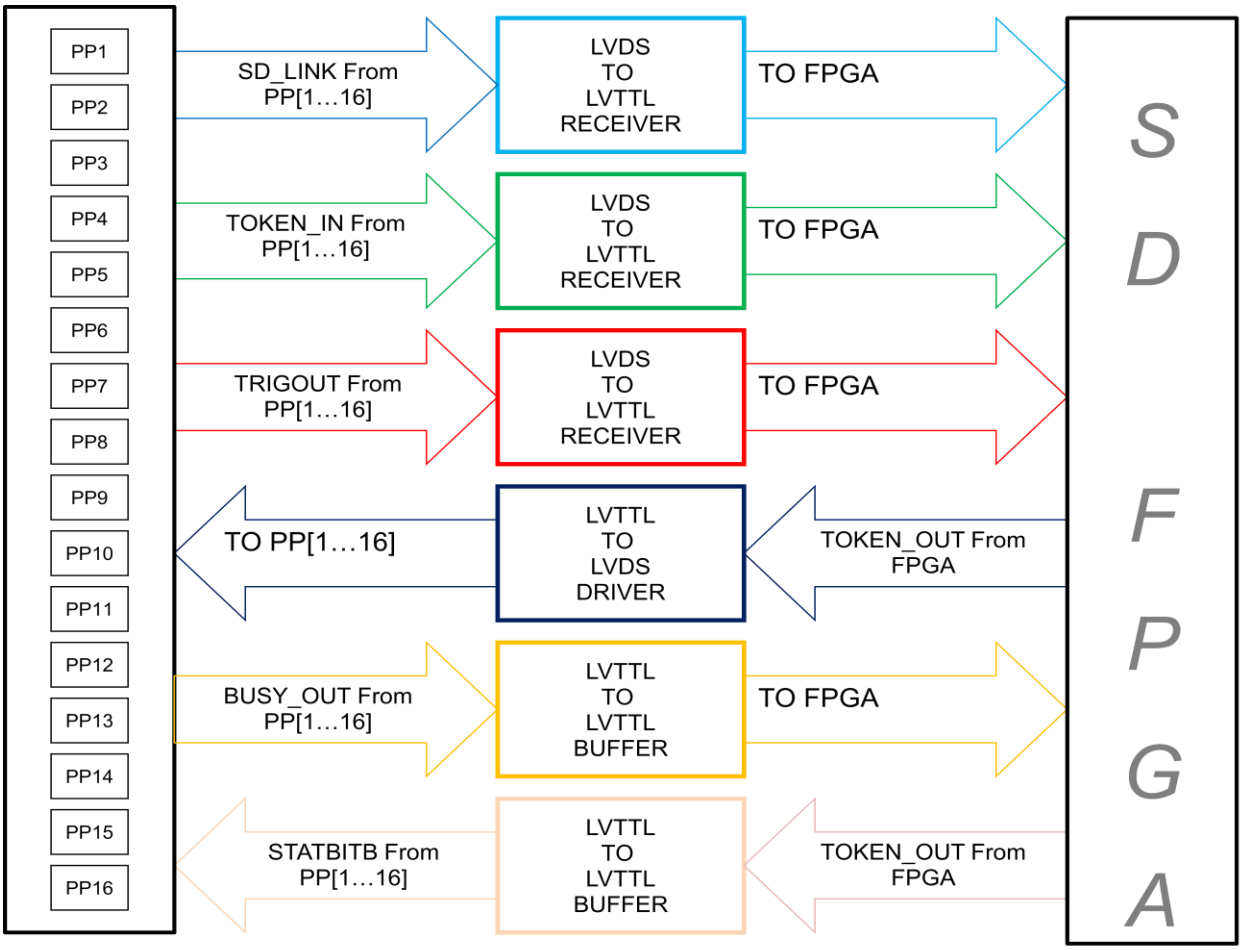
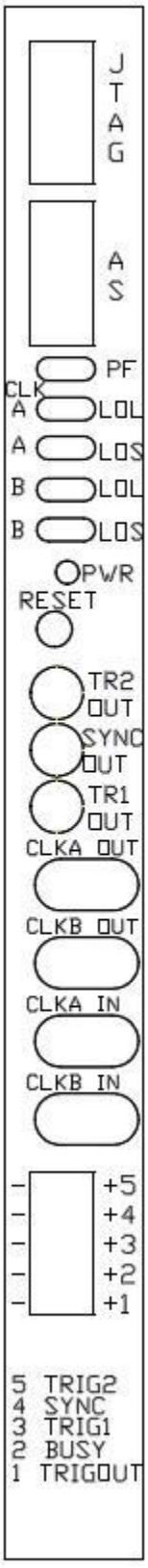


Figure 5: Shows the LVDS to LVTTL signal connections from the Payload Modules to the FPGA

Front Panel Specification Sheet



MECHANICAL

- Single width VITA 41 "B" Switch Module

INPUT SIGNALS

- CLOCKA (LVPECL)
- CLOCKB (LVPECL)

OUTPUT SIGNALS

- CLOCKA (LVPECL)
- CLOCKA (LVPECL)
- SYNC (LVPECL)
- TRIG1 (LVPECL)
- TRIG2 (LVPECL)
- BUSY (ECL)
- SYNC (ECL)
- TRIG1 (ECL)
- TRIG2 (ECL)
- TRIGOUT (ECL)

PROGRAMMING:

- JTAG Port
- Active Serial Port

LEDS:

- Power LED: Illuminates green when the board is powered up.
- PF: Power Fault (illuminates Red if the switching regulator LTM4608 malfunctions, green otherwise.
- CLOCKA loss of signal (LOS) illuminates red if the jitter attenuating PLL loses input signal, green otherwise.
- CLOCKB loss of signal (LOS) illuminates red if the jitter attenuating PLL loses input signal, green otherwise.
- CLOCKA loss of lock (LOL) illuminates red if the jitter attenuating PLL is unlocked, green otherwise.
- CLOCKB loss of lock (LOL) illuminates red if the jitter attenuating PLL is unlocked, green otherwise.

RESET:

- Momentary connect switch that puts the SD board in a known initial state when it is enabled.

4.0 Detailed Functional Description

4.1: Introduction

The Signal Distribution module is an integral part of the level 1 trigger architecture proposed for Jefferson Lab experimental halls. The Trigger architecture is composed of 3-unique crates:

- Trigger Distribution Crate
- Front End Crate
- Global Trigger Crate

The Signal Distribution module is present in all of the above crates which makes its function critical to the performance of the trigger architecture. The SD board is in the switch B position of the VME crate. Its purpose is to:

1. Distribute the ClockA, ClockB, Sync, Trig1 and Trig2 signals from the TI to all the payloads.
2. Collect TrigOUT and BusyOUT signals from all the payloads and send them to the TI.
3. Implement the token passing scheme for all payloads.
4. Communicate with the TI board (payload port 18) via I^2C.
5. Program the Jitter attenuating PLLs via SPI.
6. Collect high speed data (up to 200Mbps) from the payload boards and send the data to the TI.

1. Signal distribution

a) Clock Distribution

The main function of the SD board is signal distribution. Low skew, low jitter, low voltage PECL chips are used on the board for the distribution scheme. All the signals being fanned out from the TI to the payload modules is in LVPECL format.
The fanout scheme has been chosen such that the signals received from the Trigger Interface board are distributed to the right and left side of the crate using separate fanout chips.
Jitter on ClockA and ClockB is further attenuated using a jitter attenuating PLL. The PLLs are programmed via SPI protocol with the registers programmed according to the output frequency expected. The jitter attenuating PLLs were added to the SD board to enhance the clock jitter before distributing the clock to the FADCs. Clock jitter is prevalent mostly due to the fiber optic links used to connect the front end crate to the Trigger Distribution crate. The SD is the last board to receive the clock before distributing it to the FADCs, SSPs, TDs and other payload boards, therefore it makes sense that the jitter attenuation is done on the SD board.

b) Trigger and Sync signal Distribution

In order to compensate for the delay between clock, trigger and sync signals, a programmable delay is added to the trigger and the sync signal lines. In the front-end crate, these signals are registered (synchronized with the clock) before being fanned out to the payload modules. The delay is empirically calculated and adjusted using hardware mounted on the SD board.
It is also possible to fanout the trigger and sync signals without registering. This option is needed when the SD board is mounted in the Global Trigger crate. The delay chip has a resolution of 10ps selectable to a range of 10ns.

c) Inter switch Communication

Sync, Trigger (Trig1 and Trig2) and ClockA signals are shared by the Signal Distribution board and the Crate Trigger Processor board (Switch "A"). This is to maintain backwards compatibility between the new revision boards and the boards manufactured before the backplane mapping was changed. In addition, two spare single-ended signals and two differential pairs have also been assigned for inter switch communication.

2.

3. Token passing

A token passing scheme has been implemented for the Signal Distribution board and the payload ports. The token passing scheme is necessary to manage payload module access to the VME bus to prevent bus conflict. Payload modules access the VME bus for write purposes and because they are slaves on the VME bus, they need a control signal to manage the VME bus write. The control signal is initialized by the TI board and is passed to each payload module in a predetermined sequence. Only the payload module that holds the control signal (token) is allowed to write to the VME bus.
After appropriate processing at a payload port, the token signal is handed back to the SD to be passed on to the next payload port. In this scheme bypassing of payload ports is also possible. The order of flow of the token signal is from the leftmost to rightmost slot in the VXS crate. The last board in the token passing scheme alerts the TI after it completes its write. The system is initialized when the TI provides a token.
Any change to the token passing scheme is done during the board initialization process and can only be changed if the TI reprograms the SD board registers.

4. Aggregate TrigOUT and BusyOut signals

The Signal Distribution board receives TrigOut and BusyOut signals from all the payload boards.

TrigOut is asserted by the FADCs when certain preset conditions are met to generate a trigger. TrigOut signals from all the payloads are OR'ed and passed to the front panel of the SD board. The front panel TrigOut signal is reserved for intra-crate triggering where the signal is then connected to the front panel of the TI board which manages the incoming trigger signal.
BusyOut is asserted by the FADCs when its data buffer reaches a preset threshold. The finite data buffer will become full if the payload board is collecting more data than it's writing to the readout bus. The BusyOut signals are OR'ed from all the payloads and sent to the TI which in turn passes the signal to the Trigger Distribution Crate to alert the trigger supervisor which will manage resources. The BusyOut signal is handled the same way in both the Front End Crate and the Trigger Distribution Crate.
The SD keeps track of the source of the BusyOut signal by keeping a count of the number of times each board has asserted the signal and which board last asserted the signal. This information is important when troubleshooting to find a faulty payload module.
There are three registers that are related to the BusyOut signal:

- BusyOut_State (Read Only) register 6. This is a 16-bit register that sets a flag for each slot that has asserted it's BusyOut signal. The flag is cleared after this register is read.
- BusyOut_Mask (Read/Write) register 3. This is a 16-bit register that is used to mask the slots that the user chooses to keep track of BusyOut signals. Write a '1' to keep track of the BusyOut signal of the corresponding slot or a '0' to mask out a particular slot. The default is to keep track of all Slots.
- BusyOut_Counter (read only) registers 8 (slot 2) to register 23 (slot 19). Each payload is assigned a 16-bit register that holds the number of times the BusyOut signal has been asserted for the particular payload. The counter in each register is cleared after the register is read.

5. I^2C Communication

The Signal Distribution board gets its initial register configuration from the Trigger Interface (TI) board (Payload Port 18) in each unique crate. Data transfer between the SD and the TI board is done through I^2C protocol. There are two dedicated single-ended lines that are reserved for this purpose. The proposed method of keeping the TI and the SD synchronized is to have a memory map on the TI that is a duplicate copy of the SD memory map.
The TI board is the always the master in the protocol and the SD is always the slave. Therefore, to keep the memory map up to date the TI will have to request data from the SD frequently. To reduce the amount of time it

takes for this data exchange, the proposal is to run the I^2C communication protocol at a high data rate (the final value of which will be determined through testing).
The memory map and the programming requirements are detailed in section 5.0 below.

6. SPI Communication

The Signal Distribution board is responsible for configuring the jitter attenuating PLLs (Silicon Labs Si5326). Some of the register information needed to correctly configure the PLLs is written by the TI board. Data transfer between the SD and the PLLs board is done through SPI protocol. There are two jitter attenuating PLLs on the SD board one for ClockA and one for ClockB.
There are dedicated communication lines that are reserved for SPI communication purpose. Both PLLs share a common: Data In, Data Out, and Clock lines but each has a unique Slave Select line. The proposed method of keeping the SD and the PLLs synchronized is to have a memory map on the SD that is a duplicate copy of the PLL memory map. This will reduce the need to constantly poll the PLLs each time a data read is requested by the TI. Constant data reads can theoretically inject noise into the circuit.
The SD board is the always the master in the protocol and the PLLs are always the slave. Therefore, to keep the memory map up to date the SD will have to request data from the PLL as needed. To reduce the amount of time it takes for this data exchange, the proposal is to run the SPI communication protocol at a high data rate (the final value of which will be determined through testing). The minimum Clock period for the PLLs is 100ns which limits the data rate to a maximum of 10MHz.
The PLL memory map and the programming requirements are detailed in section 5.0 below.

7. High speed data

There is a dedicated differential pair between the all payload boards and the SD boards. It is a unidirectional link from the payloads [1 → 16] to the SD and a half-duplex link between SD and the TI. The proposed function is to have an alternative data path from the Payload modules to the TI board. Data speeds and frequency of use is yet to be tested and determined. However, hardware limits the data rate to a maximum of 200Mbps.

5.0 Programming Requirements

There are two main ways that the FPGA register configuration on the SD board can be programmed:

a) Using the JTAG or AS device connection on the front panel of the board.
b) Writing to the FPGA using I^2C.

Initial programming of the SD board is done using the Active Serial (AS) configuration and registers are initialized with specified Reset Values.

The VXS Signal Distribution module receives initial register status settings from the Trigger Interface (TI) board using I^2C bus protocol. The TI always plays the role of bus master and the SD board plays the role of bus slave.
The following register definitions will always be written with the specified Reset Values until programmed by the TI board through I^2C.

The register addresses are two bytes and the data is also two bytes long. The TI sends data to the SD in the following sequence:

i) First sends the SD address (one byte)
ii) Sends the MSB of the register address.
iii) Sends the LSB of the register address.
iv) Send the MSB of data_1.
v) Send the LSB of data_1.
vi) Send the MSB of data_2
vii) Send the LSB of data_2.

The register address is automatically incremented as more data is received until a stop condition is encountered which resets the state machine.

Register Map

Physical Slot #	2	3	4	5	6	7	8	9	12	13	14	15	16	17	18	19
Payload Port #	15	13	11	9	7	5	3	1	2	4	6	8	10	12	14	16
Logical Slot #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

The register map is defined according to the Physical slot location in the crate. The first slot is the left most slot in the crate and the last slot is the rightmost slot in the crate. In a 20 slot crate the designation is as shown in the table above.
Physical slot #2 is the leftmost slot occupied by an FADC module and is designated as the first slot (logical slot #0). Physical slots #10 and #11 are occupied by switch modules and are therefore not assigned corresponding logical slot numbers.

The logical slot designation described above is the one used in the following register map definition.

Register Address Map Summary:

i) SD Main Status: 16-bit wide register that shows the settings for the main SD functions.
ii) Updated Registers: 16-bit wide register showing the registers updated since the last read by TI.
iii) Populated boards: 16-bit register that shows all the boards populated in the crate.
iv) TokenPassingReg 16-Bit register that shows payloads taking part in the token passing scheme.
v) BusyOutMask 16-bit register containing the payload(s) to take part in the masked OR.
vi) TrigOutMask 16-bit register containing the payload(s) to take part in the masked OR.
vii) BusyOutState 16-bit register showing the payload(s) which have asserted busy since last read.
viii) TrigOutState 16-bit register showing the last payload(s) that asserted TrigOut.
ix) BusyOutCounter Sixteen 16-bit registers keeping count of how many times each payload has asserted busy since the last read.

Command, Status and Configuration Registers

Register 0.

Address = 0x00

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Name	SYSTEM RESET	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Type	R/W	R	R	R	R	R	R	R

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLKB FREQ5	CLKB FREQ	CLKB HW ENABLE	CLKB PLL BYPASS	CLKA FREQ	CLKA FREQ	CLKA HW ENABLE	CLKA PLL BYPASS
Type	R/W	R/W	R	R/W	R/W	R/W	R	R/W

Reset value = 1000 0000 1110 1110

Bit	Name	Function
15	SYSTEM RESET	This bit resets the SD Test Code when set to 1, the bit should be set to 0 to operate normally. 0: Reset SD 1: Normal Operation
14:8	RFU	Reserved for Future Use
7:6	CLKB FREQUENCY	Note: ClockB is routed to the FPGA. (Freq in MHz) **3:2 | Freq** 00: 31.25 01: 62.50 10: 125.00 11: 250.00
5	CLKA HW ENABLE	This bit shows whether the clock mode (bypass or pll-based) is set using a hardware jumper. If it is set, then the clock mode cannot be chanced using firmware 1: Hardware Jumper is closed 0: Hardware Jumper is open
4	CLKB PLL BYPASS	This selects whether ClockB fanned out will be jitter attenuated or as received from the TI. 0: Bypass Mode 1: PLL Mode
3:2	CLKA FREQUENCY	Note: ClockA is routed to the FPGA on the SD. (Freq in MHz) **3:2 | Freq** 00 : 31.25 01 : 62.50S 10: 125.00 11: 250.00
1	CLKA HW ENABLE	This bit shows whether the clock mode (bypass or pll-based) is set using a hardware jumper. If it is set, then the clock mode cannot be chanced using firmware 1: Hardware Jumper is closed 0: Hardware Jumper is open
0	CLKA PLL BYPASS	This selects whether ClockA fanned out will be jitter attenuated or as received from the TI. 0: Bypass Mode 1: PLL Mode

Register 1.

Address = 0x01

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Name	RFU	RFU	RFU	LAST_TOKEN_ADDR				
Type	R	R	R	R	R	R	R	R

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RFU	BUSYOUT STATUS	TRIGOUT STATUS	POWER FAULT	CLKA LOL	CLKA LOS	CLKB LOL	CLKB LOS
Type	R	R	R	R	R	R	R	R

Reset value = 0000 0000 0000 0000

Bit	Name	Function
15:13	RFU	Reserved for Future Use
12:8	LAST_TOKEN_ ADDR	Shows the value of the payload slot that received the token last. 00000: Default – No board selected. 00001: Payload 1. 00010: Payload 2. …. 10000: Payload 16.
7	RFU	Reserved for Future Use
6	BUSYOUT_ STATUS	This bit is set when any board has asserted its BusyOut since the last read and is set to zero after each read. 0: No change since last read. 1:At least one board has asserted busy since last read.
5	TRIGOUT_ STATUS	This bit is set when any board has asserted its TrigOut since the last read and is set to zero after each read. 0: No change since last read. 1:At least one board has asserted TrigOut since last read.
4	POWER_FAULT	This bit is set when there is a power fault detected, the bit is set to 0 after the last read. 0: Normal Operation 1: Powerfault detected
3	CLKA_LOL	This bit is set after ClockA PLL Loss of Lock is detected and set to 0 after Loss of Lock is resolved 0: Normal Operation 1: Loss of Lock on ClockA PLL.
2	CLKA_LOS	This bit is set after ClockA PLL Loss of Signal is detected and set to 0 after Loss of Signal is resolved 0: Normal Operation 1: Loss of Signal on ClockA PLL.
1	CLKB_LOL	This bit is set after ClockB PLL Loss of Lock is detected and set to 0 after Loss of Lock is resolved 0: Normal Operation 1: Loss of Lock on ClockB PLL.

0	CLKB_LOS	This bit is set after ClockB PLL Loss of Signal is detected and set to 0 after Loss of Signal is resolved 0: Normal Operation 1: Loss of Signal on ClockB PLL.

Register 2.

Address = 0x02

Bit	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Name	PAYLOAD_BOARDS[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	PAYLOAD_BOARDS[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000 0000 0000

Bit	**Name**	**Function**
15:0	POPULATED_ BOARDS[15:0]	Sets the value for the payload boards that are populated in the crate. 0: Board not present in crate 1: Board present in crate *Note: D0 → Slot 1 … D15 → Slot 16*

Register 3.

Address = 0x03

Bit	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Name	TOKEN_PASSING_REG[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name	TOKEN_PASSING_REG[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000 0000 0000

Bit	**Name**	**Function**
15:0	TOKEN_ PASSING _REG[15:0]	Sets the value for the payload boards that are taking part in the Token Passing Scheme. 0: Board not participating in token passing. 1: Board participating. *Note: D0 → First Slot in Token Passing Sequence … D15 → last Slot in Token Passing Sequence*

Register 4.

Address = 0x04

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Name	BUSYOUT_MASK[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BUSYOUT_MASK[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 1111 1111 1111 1111

Bit	Name	Function
15:0	BUSYOUT _MASK[15:0]	Sets the value for the payload boards whose BusyOut needs to be sent to the TI board. 0: Board not participating in BusyOut to TI. 1: Board participating.

Register 5.

Address = 0x05

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Name	TRIGOUT_MASK[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TRIGOUT_MASK[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 1111 1111 1111 1111

Bit	Name	Function
15:0	TRIGOUT _MASK[15:0]	Sets the value for the payload boards whose TrigOut is participating in generating a trigger output. 0: Board **not** participating in generating a trigger. 1: Board participating.

Register 6.

Address = 0x06

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Name	BUSYOUT_STATE[15:8]							
Type	R	R	R	R	R	R	R	R

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BUSYOUT_STATE[7:0]							
Type	R	R	R	R	R	R	R	R

Reset value = 0000 0000 0000 0000

Bit	Name	Function
15:0	BUSYOUT_ STATE[7:0]	Shows the current BusyOut state of the payload boards. 0: Normal Operation 1: Busy Out asserted. *Note: D0→ Slot 1 … D15→ Slot 16*

Register 7.

Address = 0x07

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Name	TRIGOUT_STATE[15:8]							
Type	R	R	R	R	R	R	R	R

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TRIGOUT_STATE[7:0]							
Type	R	R	R	R	R	R	R	R

Reset value = 0000 0000 0000 0000

Bit	Name	Function
15:0	TRIGOUT_ _STATE[15:0]	Shows the most recent TrigOut state of the payload boards. 0: Normal Operation 1:TrigOut asserted.

Register 8.

Address = 0x08

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Name	BUSYOUT_COUNTER[15:8]							
Type	R	R	R	R	R	R	R	R

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BUSYOUT_COUNTER[7:0]							
Type	R	R	R	R	R	R	R	R

Reset value = 0000 0000 0000 0000

Bit	Name	Function
15:0	BUSYOUT_ COUNTER[15:0]	Shows the current count for the number of times a payload board has asserted its BusyOut since the last read. The value is reset to zero after being read. 0000 0000 0000 0000: (Zero) to. 1111 1111 1111 1111: (65535)

Note: Addr 0x0008 → Payload board 1

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Addr 0x0018 → Payload board 16

Communication Summary

a. I^2C

The primary mode of communication between the SD and the TI is I^2C. This link was tested on SD_Rev001 by sending and receiving data using TI_Rev001 board. Using a CPU on one of the slots, data was written and read from the SD by sending commands using a hyperterminal window on the PC. To verify that the correct data was sent/received on the SD module, signal tap was set up on the data lines that stored/retrieved data to/from the SD board.

The protocol used to store and read data from the SD was in the format of:

- A byte representing address.
- A word (two bytes) representing data.

This link was validated as working by reading back the data as it was written to the SD. This test was done with the protocol at a speed of about 3Mbps.

The secondary mode of communication between the SD and the TI is yet to be tested.

Addendum

The following items were changed in this version of SD module description.

- On Register 0, Changed the functions of bits 2 and 5 from RFU to Hardware Jumper status.