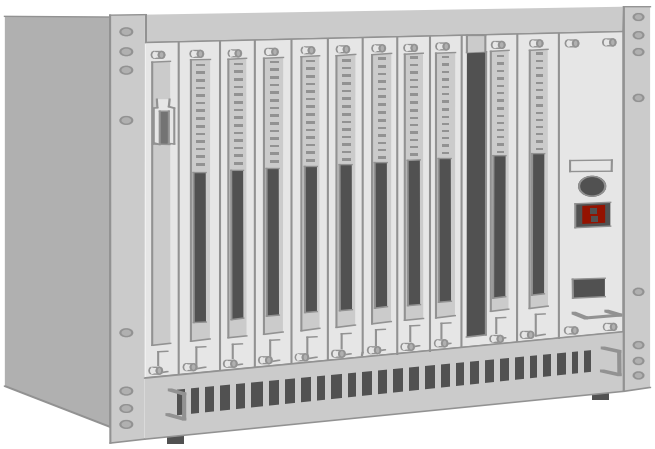

The VME Programmable “OR” Module

Version 1

Shudi Gu
Data Acquisition Group
Visitor from Institute of High Energy Physics, Beijing, China
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Introduction

There are applications in DAQ systems that require a fan in of many logic signals. As circumstances change, various subsets of these input signals are required. To avoid re-cabling, a programmable "OR" module is useful.

The Programmable "OR" Module, described in this document, is implemented as a VME module. It can accept 32 pairs of ECL differential input signals. Each can be individually enabled or disabled from contributing to the output. The outputs of the module are the logical "OR" of these enabled input signals. For flexibility, 3 kinds of output signals are provided. They are a differential ECL output, a single-ended ECL output, and a NIM output with LEMO connector. A front panel LED indicates the presence of any enabled input signals.

The 32 input signals are divided into 2 groups, having 16 input signals each. Each group has its own logical "OR" outputs (differential and single-ended ECL).

The contribution of the 32 input signals to the output is individually remotely controlled by software via VME interface. It is realized by a 32 bits Input Enable Register. The contents of the Input Enable Register can be written or read by the VME interface to ensure the correct control. The status of the 32 input signals can also be read by the VME interface. The status of the 32 input signals is latched into an Input Status Register when the lowest order byte of the Input Status Register is read (with D16, D08 or unaligned mode), to ensure that the status information of the 32 input signals is collected at the same time.

Front panel connectors and indicator

Figure 1 identifies the VME Programmable "OR" module front panel connectors and indicator.

Two 34-pin connectors are for 32 ECL differential input signals. A 100-ohm resistor inside the module terminates each channel. These SIP8 isolated resistors are socketed and can be removed for daisy chain application (see Figure 2). When the inputs are daisy chained, additional SIP10 bused resistors shown in Figure 2 (3.9K-ohm and 1.8K-ohm, note Pin 1) can also be removed. When in place, these resistors bias the input receivers so that an unconnected input results in a stable low output. Connector "INPUT A" is for the channels from 0 to 15. Connector "INPUT B" is for the channels from 16 to 31.

One 20-pin connector is for output signals. The bottom 3 signals are for differential outputs. The top 3 signals are for single-ended outputs.

TD	Differential “OR” output for the total 32 input signals
AD	Differential “OR” output for Group A input signals
BD	Differential “OR” output for Group B input signals
TS	Single-ended “OR” output for the total 32 input signals
AS	Single-ended “OR” output for Group A input signals
BS	Single-ended “OR” output for Group B input signals

A LEMO connector labeled with “NIM OR” is the “OR” output for the total 32 input signals with NIM level.

An LED labeled with “OR” is lit if any of the enabled input signals are asserted.

Grounding

This module as well as other modules connected to it should be well grounded at their own side. Although differential lines have good performance to reject common mode noise, it is still recommended that additional ground lines accompany with the differential lines to reduce the electronic and magnetic field noise. The unused pins of the input and output connectors are connected to ground inside the module to provide ground connections between modules. In addition, some modules may not be grounded properly. There may be a big static voltage difference between the ground of the modules. The differential receiver may not work properly, if the voltage difference exceeds the dynamic range of the differential receiver. The additional ground lines that accompany with the signal lines can avoid this situation.

Internal registers

The module is programmed through VME protocols (ANSI/IEEE STD1014-1987). The module is categorized as a A24:D32 slave. All storage location can be accessed as both supervisory (AM=3D) and Non-privileged (AM=39) data.

The base address (A23-A08) of the module is set by DIP switches on the board (see Figure 2). Note that a switch in the OFF position defines a “1” for the corresponding address bit.

There are two registers on the module. Each is 4 bytes wide. A description of each register and its local address is given below.

Input Enable Register (local address = 0): Can be read and written by VME interface. If a bit is set to “1”, the corresponding input channel is enabled. Otherwise, the corresponding channel is disabled.

Input Status Register (local address = 4): Read only. Each bit reflects the logical status of the corresponding input channel, whether it is enabled or not. The input signal status is latched when the lowest order byte (byte address 4) is read. This ensures that the status of

the 32 channels is collected at the same time when D16, D08 or unaligned modes are used to read the register.

For simplicity of design the address lines A03 to A07 are not decoded on the module. Thus the module occupies 256 bytes of address space. As a consequence, the Input Enable Register appears at local address 0+8N, and the Input Status Register appears at local address 4+8N, where N=0, 1, … 31.

Power supply

This module draws about 2 amps of –5.2V current. There are 2 configurations to obtain –5.2V power.

- 12V input (1A) DC/DC Converter
+12V input (1A) DC/DC Converter

The two configurations are available, so that when multiple modules are installed in the same crate the power supply limit will not be exceeded. For reconfiguration, contact with DAQ or Fast Electronics Group for assistance.

The module draws about 1 amps of +5V.

The ON/OFF status of the –5.2V power supply is indicated by an LED located at the bottom of the board. Another LED located in the middle of the board indicates the ON/OFF status of the +5V power supply. All of the +5V, +12V and –12V input power supplies have their own fuse located in the middle of the board. The fuses are rated at 3A (Figure 2).

Performance

The "OR" logic is done using ECL integrated circuits for high speed, thus making it suitable for trigger logic applications.

The propagation delay from any input to the total "OR" output is less than 8ns.

The propagation delay from an input of group A (B) to the group A (B) "OR" output is less than 7ns.

The propagation delay from any input to the total NIM "OR" output is less than 11ns.

Alternate uses

According to the Boolean Equation:

$$/A + /B + /C + \ldots = /(A*B*C*\ldots).$$

Thus, the module can also be used as a Programmable “AND” Module, provided all of the differential input and output signals are reverse connected to the input and output connectors. This function can be used to make trigger decisions.