VME Memory Lookup Unit (MLU) Notes E.J. 4/99

When configured for front panel use, the module has the following modes of operation:

(1) Register Mode – Input data is stored in registers on the rising edge of *Input Enable*. The stored data is presented to the memory as a 16-bit address. The *Output Ready* signal is valid whenever no positive transitions of *Input Enable* take place. The rising edge of *Input Enable* negates *Output Ready* until valid output is driven from the module. When in register mode there are two data output modes that can be selected. These modes can be defined for the outputs in groups of four.

Normal – Programmed levels are driven out and remain valid until the next *Input Enable* rising edge.

Pulsed – Programmed levels are driven out for a time interval (10 – 100 ns adjustable) after which all outputs are negated (held low).

(2) Transparent Mode – Input data is presented directly to the memory as an address (no register store). Data out will be valid one memory access time after the input data (i.e. address) becomes stable. *Output Ready* will remain timed to the *Input Enable* signal as in the Register Mode. It will have no relationship to valid data out unless this is arranged by appropriate *Input Enable* timing. A pulsed mode of driving outputs is not relevant when in the transparent mode.

The individual locations of the memory can be programmed by VME write cycles only when front panel access has not been selected. Similarly, individual locations can be queried by VME read cycles only when front panel access has not been selected. However, the memory outputs can be sampled during front panel access when a VME read of the memory occurs. In this case the VME address is ignored - addressing any valid memory location returns the state of the memory outputs (latched) at the time of the read.

Addressing

The module has two independent addresses that are set with on-board multi-element switches. The first is the base address of memory. A24 (Supervisory or Non-privileged data) cycles are used to access the memory. The memory consists of 64K 16-bit words, or 128 Kbytes of VME address space. Requiring the memory base address to occur on a 128 Kbyte boundary allows switches to fix address bits A23 through A17.

The second address is that of the Control Register. A16 (Supervisory or Non-privileged data) cycles are used to access this single 16-bit register. Switches determine address bits A15-A1.

The advantage of the above scheme is that the memory arrays of multiple modules can be set up to be contiguous in VME address space. Address space is also

used most efficiently in contrast to schemes that place the Control Register adjacent to the memory array. The complications of having two addresses to manage on the module are somewhat abated by the information contained in the Control Register. The most significant byte of this register has the memory base offset (i.e. A23-A17 switch settings) as its data. This is of particular use in multi-module systems, as the Control Register of each module points to its associated memory.

Control Register (CR)

Bits 0-7 are read/write, while bits 8-15 are read only.

(0) Front Panel Access – setting this bit selects the memory to be addressed from front panel data. It also permits *Input Enable* strobes to enter the module. Clearing this bit allows properly addressed VME cycles to read and write individual memory locations.

(1) Transparent Mode – setting this bit in front panel mode (CR(0) = 1) causes input data to bypass the registers and be applied directly to the memory address lines. Clearing this bit enables the *Input Enable* signal (rising edge) to store the input data. This stored data serves as the memory address.

(2) Pulse Output Bits (0-3) – setting this bit in registered front panel mode (CR(0) = 1, CR(1) = 0) allows programmed memory levels of output bits (0-3) to be driven out for a time interval (10-100 ns, adjustable). After this interval these outputs are held not asserted (low). The pulse occurs shortly after the rising edge of the *Output Ready* signal. Clearing this bit allows these programmed levels to be driven out and held valid until the next *Input Enable* rising edge.

(3) Pulse Output Bits (4-7) – same as for CR(2), but controls output bits (4-7).

(4) Pulse Output Bits (8-11) – same as for CR(2), but controls output bits (8-11).

(5) Pulse Output Bits (12-15) – same as for CR(2), but controls output bits (12-15).

(6) Reserved - (for future use)

(7) Reserved - (for future use)

(8) Unused – (read as 0)

(9) – (15) Bit 17-23 Base Memory Address – (read only)