VME Latch Driver

Ed Jastrzembski, Shudi Gu
Data Acquisition Group
7/99

Introduction

In a trigger system it may be required to sample the status of digital signals at some precise time, and then perform logic using the stored values. The VME Latch Driver module can simultaneously sample and store data from 16 inputs. Two independent copies of the stored data are driven from the module for external use. Configuration of the module is done from the front panel - the module uses the VME chassis only for power.

There are three basic modes in which the module can be used. In Strobe Mode the state of the data inputs is sampled on the rising edge of the strobe control input (STBI). In Latch Mode with External Gate a coincidence (positive logic) between a common external gate signal (GTIN) and each data input is formed. If a data input is asserted at any time during the gating window, the corresponding data output bit will be set. Latch Mode with Internal Gate is similar to this, but circuitry on the board is used instead to generate the gating signal from the rising edge of the strobe input. The latch modes allow the flexibility of sampling the input data over a longer time period.

A front panel view of the module is shown in Figure 1. Tables 1 - 3 identify all I/O signals and their pin assignments. Input Data is applied to the module on Connector C. Identical copies of the latched data are independently driven out on Connectors A & B. Control for the latching action is through Connector D. A layout of the board is shown in Figure 2. Timing adjustment points are indicated there.

The Latch Driver module is compatible with the simple and elegant data flow protocol of the LeCroy ECLine series of CAMAC based trigger modules (Figure 3). In this system, a module accepts input data that is declared valid by an external input enable strobe signal (GTIN). When a module generates output data, it asserts an output ready status signal (RDY1, RDY2) to indicate that the data is valid. Upon receipt of a positive edge of the input enable signal, a module negates its output ready and begins processing the input data. Once valid output data is available, the module again asserts output ready. With this simple scheme modules can be linked sequentially by connecting output ready of one module to the input enable of the next module. Complex processing can be done in stages, and at hardware speed.

Detailed timing diagrams and specifications for the three operating modes of the Latch Driver are shown in Figures 4 to 6. In addition to the output ready status signal (RDY1, RDY2), the Latch Driver module generates an output ready strobe pulse (STO1, STO2) when the output data becomes valid. This allows the Latch Driver to couple directly with modules requiring a pulse for an input strobe. The width of the strobe pulse is adjustable (15 – 100 ns) by a potentiometer identified in Figure 2.

Configuring the Module

(A) Operating Modes – the module is configured from the front panel to be in one of the following modes:

(1) Strobe Mode – select by connecting an appropriate strobe signal to either of the two strobe inputs (STBI), and having NO connection to the gate input (GTIN). Note that, in particular, the gate input (GTIN) must NOT be tied to a gate output (GTO1 or GTO2). The output ready signals (RDY1, RDY2) are delayed from the strobe's leading edge by the internal

gate width (see Latch Mode with Internal Gate), so this should be set to its minimum (15 ns) for best performance.

(2) Latch Mode with External Gate – select by connecting an appropriate external gate signal to the gate input (GTIN), and having NO connection to either of the strobe inputs (STBI). The assertion of the output ready signals (RDY1, RDY2) is delayed until after the end of the external gate.

(3) Latch Mode with Internal Gate – select by connecting an appropriate strobe signal to either of the two strobe inputs (STBI), and connecting the gate output (GTO1) to the gate input (GTIN). A twisted-pair cable or shunts (jumpers) can be used to join these. If shunts are used, connect pin 7 to pin 9, and pin 8 to pin 10. The gate output width is adjustable by a potentiometer accessible through the front panel (see Figures 1 & 2). The nominal range is from 15 to 100 ns, but this can be extended with the addition of a capacitor (see DAQ group). The assertion of the output ready signals (RDY1, RDY2) is delayed until after the end of the gate. The other gate output signal (GTO2) may be connected to a second Latch Driver module (configured in Latch Mode with External Gate), allowing the two modules to use identical gates generated from a single strobe.

(B) Data Cable Termination - socketed SIP resistors are used to terminate the input data cable. The resistor locations are shown in Figure 2 and the values are listed below (assuming the cable has a characteristic impedance of 100 ohms). The resistors MUST be present if the Latch Driver is the last module along the cable. When daisy chained connections are desired and the Latch Driver is not the last module, the SIP resistors should be removed. Each SIP resistors is tied to 4 data lines, so the termination or non-termination of lines must be done in groups of 4 data inputs.

Data Inputs	Location	Package	Resistor
Data 0 - 3	R6	SIP8	100 ohm, isolated
Data 4 - 7	R7	SIP8	100 ohm, isolated
Data 8 - 11	R26	SIP8	100 ohm, isolated
Data 12 - 15	R27	SIP8	100 ohm, isolated

(C) Input Power - can be chosen to be -12V or +12V by installing jumpers in different locations (see Figure 2). The -5.2V power needed for ECL logic is derived from the +12V or - 12V supplied by the VME backplane. The option of +/- power input can be important if multiple Latch Driver Modules (or other boards that use 12V) are installed in the same VME chassis. The Latch Driver Module uses about 1 amp of the 12V rail, and the VME chassis may provide as little as 5 amps each of -12V and +12V. By mixing -12V and +12V modules in the same chassis, overloading of the power supply may be avoided. Please seek the advice of the DAQ group or Fast Electronics group if reconfiguration of the input power is desired.

Visual Indicators

An LED on the board indicates the powered status of the module (see Figure 2). When the LED is lit, -5.2V (derived from -12V or +12V) is present. A blown fuse on the board is the most likely cause of an unlighted condition. Fuses have a rating of 3 amps, and their locations are shown in Figure 2.

Table 1. Connector A, B signal definition - All signals are differential ECL.
A & B carry identical data but are independently driven.
(Pin 1 is the lower right pin on each connector.)

Signal name (Q)	Direction	Pin # (Q,/Q)
Latched Data_0	Output	1,2
Latched Data_1	Output	3,4
Latched Data_2	Output	5,6
Latched Data_3	Output	7,8
Latched Data_4	Output	9,10
Latched Data_5	Output	11,12
Latched Data_6	Output	13,14
Latched Data_7	Output	15,16
Latched Data_8	Output	17,18
Latched Data_9	Output	19,20
Latched Data_10	Output	21,22
Latched Data_11	Output	23,24
Latched Data_12	Output	25,26
Latched Data_13	Output	27,28
Latched Data_14	Output	29,30
Latched Data_15	Output	31,32
GND	------	33,34

Table 2. Connector C signal definition - All signals are differential ECL.
(Pin 1 is the lower right pin on the connector.)

Signal name (Q)	Direction	Pin # (Q,/Q)
Data_0	Input	1,2
Data_1	Input	3,4
Data_2	Input	5,6
Data_3	Input	7,8
Data_4	Input	9,10
Data_5	Input	11,12
Data_6	Input	13,14
Data_7	Input	15,16
Data_8	Input	17,18
Data_9	Input	19,20
Data_10	Input	21,22
Data_11	Input	23,24
Data_12	Input	25,26
Data_13	Input	27,28
Data_14	Input	29,30
Data_15	Input	31,32
GND	------	33,34

Table 3. Connector D signal definition - Signals are differential ECL (Q, /Q) or single-ended ECL (G, Q). Names in parentheses match those on the front panel. (Pin 1 is the lower right pin on the connector.)

Signal name (Q)	Direction	Pin #	Type
Strobe In (STBI)	Input	1,2	G, Q
-------	-------	3,4	------
Strobe In (STBI)	Input	5,6	Q, /Q
Gate In (GTIN)	Input	7,8	Q, /Q
Gate Out (GTO1)	Output	9,10	Q, /Q
Gate Out (GTO2)	Output	11,12	Q, /Q
Ready (RDY1)	Output	13,14	Q, /Q
Ready (RDY2)	Output	15,16	Q, /Q
Strobe Out (STO1)	Output	17,18	Q, /Q
Strobe Out (STO2)	Output	19,20	Q, /Q