A Flexible VME Input/Output Module

(preliminary)

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Introduction

It is often required in experiments to have a number of digital Input/Output (I/O) channels under computer control. The solution would be straightforward if the required I/O levels were always the same. However, individual applications may need different (and probably a mixture of) I/O types: NIM, differential ECL, single-ended ECL, TTL, RS-485, fiber optic, etc. One could construct I/O modules of all these types. The only differences among these would be the drivers/receivers and front panel connectors. The back end (i.e. VME Interface and registers) would be identical. This leads us to the idea of a modular I/O system: a base board that has the VME Interface and registers, and a set of distinct plug-in translator boards to give the desired I/O levels and connectors.

Our implementation of this concept is illustrated in Figure 1. This shows a single-slot 6U VME base board that supports two translator cards. These cards are defined to be either the Input or the Output type. Each translator card can have up to 16 channels. The base board can be loaded with any combination of Input or Output cards. An I/O card location on the baseboard is called a Port. Each Port has its own Data Register and Control/Status Register. The system is designed so that the base board recognizes the type (Input or Output) of plug-in card and configures itself to communicate with it. At minimum each plug-in card will perform the appropriate translation or signal driving function. However, we have built additional functionality into the baseboard that allows for such things as latching input data and interrupt generation on an external strobe, and pulsing of output data. The key feature is that most of the complexity is in the common baseboard. This makes the plug-in I/O cards straightforward to design and build. Although front panel space on the plug-in cards is somewhat limited, it can support up to 18 Lemo connectors if the vertically stacked type is used. Table 1 documents the Port signal definitions.

Input Card

This card translates the input signal levels to TTL levels required by the baseboard. It handles 16 channels, with an optional external strobe input. There are two basic modes of operation currently defined:

(1) Latch inputs on VME read - values of the inputs are latched into the appropriate Port Data Register on the baseboard when a VME read of this register is initiated.

(2) External latch mode - an external strobe signal latches the input values into the appropriate Port Data Register on the baseboard. A bit in the port's Control/Status Register is set to indicate that valid data is present. The Data Register can then be read. Once data has been latched, the latching action must be explicitly be re-activated by a write to the CSR. Optionally, a VME interrupt may be generated to signal the presence of valid data.

Output Card

This card translates the TTL levels of the baseboard to the required output levels. It handles 16 channels. An optional external strobe input may be used. There are three basic modes of operation currently defined:

(1) Direct VME output - data written to the appropriate Port Data Register by a VME write cycle is transmitted directly to the outputs. Output values remain held until the next VME write to this register, or until the board is reset.

(2) VME pulse output - data written to the appropriate Port Data Register by a VME write cycle sets a 16-bit enable mask. Enabled channels are pulsed when a bit in the port's Control/Status register is written to. Pulse width is controlled by an potentiometer on the baseboard. Each port has its own pulse width control.

(3) External strobe pulse - data written to the appropriate Port Data Register by a VME write cycle sets a 16-bit enable mask. Enabled channels can be pulsed with Port's Output Enable signal, which is a delayed copy of the external strobe input.

Module Registers

The VME I/O Module is programmed by the user through VMEbus protocols (ANSI/IEEE STD1014-1987). The device meets all VMEbus standards. The module is categorized as an A16 - D16 VMEbus slave. All storage locations can be accessed as both Short Supervisory and Short Non-privileged data. In terms of its interrupt capability the module is classified as an I(1-7), D08(O), ROAK VMEbus interrupter.

We now describe in detail the registers of the VME I/O Module. The local address of each register is given. The base address (A15 - A4) is selected by DIP switches on the board (see "Configuring The Module").

1. PORT 1 CONTROL/STATUS REGISTER (CSR1) [addr = 0]

CSR1 is used to configure the operating conditions of Port 1, as well as provide the current status of the port. The meaning of the individual bits depends on which type (Input or Output) card is plugged into the port. Bits are read/write unless otherwise indicated.

For an INPUT Card :

(0) ENABLE EXTERNAL STROBE - setting this bit permits the external strobe signal to affect the action of the input port. Clearing this bit means the signal is ignored.

(1) EXTERNAL LATCH MODE - setting this bit selects the external strobe signal to latch the input values into the Port Data Register. (The strobe must also be enabled (bit 0) for the latching action to occur.) Clearing this bit means that latching will occur on a VME read of the Port 1 Data Register.

(2) ENABLE INTERRUPT - setting this bit allows an enabled external strobe signal to initiate a VMEbus interrupt.

(3) RESERVED - a spare bit for future use.

(4) DATA AVAILABLE - (Read only) a set bit indicates that the external strobe has latched data into the Port Data Register.

(5) INTERRUPT REQUEST - (Read only) a set bit indicates that the external strobe from this Port has requested a VME interrupt.

(6) - (7) PORT ID - (Read only) Signal levels ID 1 and ID 2 on the Port connector. Provides identity of the plug-in card:

ID 2 bit (7)	ID 1 bit (6)	meaning
1	1	NO card installed
1	0	Input Card installed
0	1	Output Card installed
0	0	Reserved

(8) RE-ACTIVATE STROBE - (Write only) asserting this bit generates a pulse that allows the external strobe to latch data and/or generate interrupt requests again.

(9) - (14) UNUSED - (read as 1)

(15) RESET MODULE - (Write only) asserting this bit generates a pulse that clears CSR bits (0)-(5) of both Ports, clears both Data Registers, and clears the common Interrupt Register.

For an OUTPUT Card:

(0) - (1) MODE - selects the output mode of the Port:

bit (1)	bit (0)	meaning
0	0	Direct VME output
0	1	VME Pulse output
1	0	External Strobe pulse
1	1	Reserved

(2) ENABLE EXTERNAL STROBE - setting this bit permits the external strobe signal to affect the action of the output port. Clearing this bit means the signal is ignored.

(3) - (5) RESERVED - spare bits for future use.

(6) - (7) PORT ID - (Read only) Signal levels ID 1 and ID 2 on the Port connector. Provides identity of the plug-in card:

ID 2 bit (7)	ID 1 bit (6)	meaning
1	1	NO card installed
1	0	Input Card installed
0	1	Output Card installed
0	0	Reserved

(8) PULSE OUTPUT - (Write only) asserting this bit causes outputs that have been enabled to pulse.

(9) - (14) UNUSED - (read as 1)

(15) RESET MODULE - (Write only) asserting this bit generates a pulse that clears CSR bits (0)-(5) of both Ports, clears both Data Registers, and clears the common Interrupt Register.

2. PORT 1 DATA REGISTER (DATA1) [addr = 2]

Each of the 16 data bits maps to an input or output channel. The meaning of the register depends on which type of card is plugged into the port.

For an INPUT Card :

A VME Read of this register will yield input values that are either current (Latch on VME read) or that have been latched by the external strobe (External latch mode). A VME Write to this register has no effect.

For an OUTPUT Card :

A VME Write to this register will set values to be output, either immediately (Direct mode) or by pulse (CSR write or external strobe). A VME Read of this register will give back the set values.

3. PORT 2 CONTROL/STATUS REGISTER (CSR2) [addr = 4]

(same as for Port 1)

4. PORT 2 DATA REGISTER (DATA2) [addr = 6]

(same as for Port 1)

5. INTERRUPT REGISTER [addr = 8]

The Interrupt Register is programmed with the 8-bit interrupt ID. During the interrupt acknowledge cycle the reading of this register allows the interrupt handler to identify the VME I/O Module as the source of the interrupt request.

All bits are Read/Write.

(0) - (7) INTERRUPT ID

(8) - (15) UNUSED - (read as 1)

Multiple Interrupt Sources

Because input cards can be installed in both Ports A and B, two independent interrupt sources for the module are possible. First we describe how a single interrupt source behaves, and then consider two independent sources.

If a single input card is present and enabled for interrupt generation from its external strobe, the arrival of a strobe (positive asserted at Port input) will initiate a VME Interrupt Request (IRQ). The strobe is disabled from further latching or generation of interrupts. An Interrupt Acknowledge cycle (IACK cycle - transparent to the user) will occur. During this cycle the module identifies itself to the interrupt handler (i.e. single board computer) as the source of the interrupt by providing its Interrupt ID (contents of Interrupt Register). The Port's CSR bit 5 (Interrupt Request) is set. The user's Interrupt Service Routine (ISR) will execute. This may involve reading the Port's Data Register. At the end of this routine the Port's external strobe

must be explicitly re-enabled by writing to the Port's CSR bit 8. This also clears the Port's CSR bit 5. A subsequent strobe can now generate another interrupt.

We now consider input cards installed in both Ports A and B. Assuming that both are enabled to generate interrupts, the Port with the first occurrence of an external strobe will initiate a VME IRQ. At the end of the subsequent IACK cycle the module will latch the value of each Port's Interrupt Request bit (CSR bit 5). If an external strobe on the other Port arrives before this latching takes place, both interrupts can be handled by the same call to the user's ISR. If the external strobe on the other Port arrives later than this, the ISR will not see this Port's Interrupt Request bit asserted. The ISR will only re-enable the single Port's strobe, and module will issue another IRQ corresponding to the later strobe.

I/O Timing

With an Input card configured for external latch mode, the data to be latched should be valid and stable during the period 7 - 20 ns *after* the rising edge of the external strobe to guarantee capture. This time is specified at the Port connector, and should be adjusted for propagation delay *differences* between the data and strobe on the Input card itself. Minimum pulse width for the external strobe signal is 10 ns.

With an Output card configured for external strobe pulse mode, the Port's Output Enable signal is delayed from the external strobe by less than 10 ns. This time is specified at the Port connector. On the Output card a coincidence between the Output Enable signal (positive asserted TTL) and the Port's Data word (previously set) determines the output pattern driven. Propagation delays on the Output card must be added to get the total *external strobe to data output* time. Minimum pulse width for the external strobe signal is 10 ns.

Configuring The Module

(a) VMEbus Base Address - this is set using the 12 element DIP switch identified in Figure 2. Switch element 1 is A15, ..., Switch element 12 is A4. An open switch defines a '1'.

(b) VMEbus Interrupt Level - this is set using the 3 element DIP switch identified in Figure 2. The level is binary encoded - Switch element 1 is bit 2, ..., Switch element 3 is bit 0. An open switch defines a '1'.

2 LEDs on the board indicate the powered status of the Module (see Figure 2). The LED near the center of the board indicates that +5V is present when it is lit. The LED in the lower portion of the board indicates that -5.2V (derived from +/-12V) is present when it is lit. A blown fuse on the board is the most likely cause of either of these LEDs not to be lit. All fuses have a rating of 3 amps, and their locations are shown in Figure 2.

ECL Power for I/O Cards

Under normal circumstances the -5.2V power for ECL logic on the I/O cards can be provided by a baseboard mounted voltage regulator (+ heat sink) using the -12V VME input supply. For high drive currents on output cards, the regulator may not be able to provide

adequate current without overheating (resulting in shutdown). The maximum current that the regulator/heat sink combination can supply is about 1.5A. When more current is required the regulator can be replaced with a DC-DC converter powered by either the -12V or +12V VME supply. Up to 4A is then available for use. The DC-DC converter option is also useful to reduce loading on the -12V VME supply when multiple cards of this type (or others that use -12V to generate -5.2V) are installed in the same chassis. One can balance -12V and +12V usage to prevent exceeding the power supply limits.

Consult the Data Acquisition Group or Fast Electronics Group for advice on I/O card loading, and to reconfigure the -5.2V power source.

Table 1. I/O Port Connector pin definition. All signal levels are positive asserted TTL. The location of Pin 1 is shown in Figure 2.

Pin	Signal Name	Direction
1	GND	-------
2	GND	-------
3	External Strobe	Input
4	Spare	-------
5	GND	-------
6	GND	-------
7	Data 0	I/O
8	Data 1	I/O
9	Data 2	I/O
10	Data 3	I/O
11	Data 4	I/O
12	Data 5	I/O
13	Data 6	I/O
14	Data 7	I/O
15	GND	-------
16	GND	-------
17	Data 8	I/O
18	Data 9	I/O
19	Data 10	I/O
20	Data 11	I/O
21	Data 12	I/O
22	Data 13	I/O
23	Data 14	I/O
24	Data 15	I/O
25	GND	-------
26	GND	-------
27	ID 1	Input
28	ID 2	Input
29	+5V	-------
30	-5.2V	-------
31	+5V	-------
32	-5.2V	-------
33	+5V	-------
34	-5.2V	-------
35	Output Enable	Output
36	+12V	-------
37	Spare	-------
38	-12V	-------
39	GND	-------
40	GND	-------