VME Latch FIFO

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Introduction

In a data acquisition system it is often required to sample the status of digital signals at some precise time (e.g. at the time of a trigger). Because the data acquisition systems at JLAB support hardware buffering in their front ends, the latching module must also include buffering to be compatible. The VME Latch FIFO module has been designed to meet these basic needs. It also has additional features that may make it useful in other applications.

The module can simultaneously sample and store up to 16 data inputs. Data inputs are differential ECL levels, while control inputs are duplicated in single-ended ECL and differential ECL for flexibility. The buffer is organized as a FIFO and has a depth of 32K 16-bit words. The module can be configured to automatically buffer data after sampling, or wait for an input control signal (BUFFER) to initiate storage. Use of the BUFFER signal is important when the system has multiple levels of triggering. In this case promptly latched data needs to be stored only when the event later passes the criteria of the highest level trigger.

There are two basic modes in which the data from the inputs can be sampled. In STROBE mode the data inputs are simply sampled on the rising edge of the STROBE control input. In LATCH mode a coincidence between a common GATE IN control signal and each data input is formed. If a data input is asserted at any time during the GATE IN window, the corresponding data bit will be set. The LATCH mode allows the flexibility of sampling over a longer time period. In the limit that the GATE IN signal window goes to zero width, the LATCH mode becomes equivalent to the STROBE mode. Circuitry on the board allows the user to generate a gating signal from the rising edge of the STROBE input. The output signals GATE OUT have an adjustable width (see "Configuring the Module"). This GATE OUT signal may be connected to the GATE IN input by a cable (to adjust delay) or with two shunts (jumpers) at the control port's connector pins.

When the module is configured to buffer data only on the assertion of the BUFFER external control input, operation in the above two modes differs slightly. In STROBE mode, sampled data that is not to be buffered is simply written over by the next sampling. In LATCH mode, the sampled data that is not to be buffered must be explicitly cleared using the CLEAR control input. Thus in LATCH mode, sampled data must always be followed by the assertion of either the BUFFER or the CLEAR signal (when buffering is not automatic).

The number of words currently stored in the FIFO buffer is available to the user. The module can also be configured to generate a VMEbus interrupt when the number of data words stored in the buffer is equal to a value programmed by the user. A multitude of LEDs indicate the current operations of the module.

A front panel view of the module is shown in Figure 1. Tables 1 - 3 identify all I/O signals and their pin assignments. Connectors A & B are both tied to the same data inputs. This simplifies daisy chaining to the module, and also accommodates inputs from more than one source.

Table 1. Connector A, B signal definition - All signals are differential ECL (Pin 1 is the lower right pin on each connector.)

Signal name (Q)	Direction	Pin # (Q,/Q)
Data_0	Input	1,2
Data_1	Input	3,4
Data_2	Input	5,6
Data_3	Input	7,8
Data_4	Input	9,10
Data_5	Input	11,12
Data_6	Input	13,14
Data_7	Input	15,16
Data_8	Input	17,18
Data_9	Input	19,20
Data_10	Input	21,22
Data_11	Input	23,24
Data_12	Input	25,26
Data_13	Input	27,28
Data_14	Input	29,30
Data_15	Input	31,32
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Table 2. Connector C signal definition - Signals are single-ended ECL (G, Q) or differential ECL (Q, /Q). (Pin 1 is the lower right pin on the connector.)

Signal name (Q)	Direction	Pin #	Type
Strobe (STB)	Input	1,2	G, Q
Buffer (BUF)	Input	3,4	G, Q
Clear (CLR)	Input	5,6	G, Q
-------	-------	7,8	------
Strobe (STB)	Input	9,10	Q, /Q
Buffer (BUF)	Input	11,12	Q, /Q
Clear (CLR)	Input	13,14	Q, /Q
Gate_In (GTI)	Input	15,16	Q, /Q
Gate_Out (GTO)	Output	17,18	Q, /Q
Gate_Out (GTO)	Output	19,20	Q, /Q

Table 3. Connector D, E, F signal definition - All signals are single-ended ECL on LEMO connectors.

Signal name	Direction	Connector
Strobe (STB)	Input	D
Buffer (BUF)	Input	E
Clear (CLR)	Input	F

VME Latch FIFO Registers

The VME Latch FIFO is programmed by the user through VMEbus protocols (ANSI/IEEE STD1014-1987). The device meets all VMEbus standards. The VME Latch FIFO is categorized as an A24 - D16 VMEbus slave. All storage locations can be accessed as both Supervisory and Non-privileged data. In terms of its interrupt capability the module is classified as an I(1-7), D08(O), ROAK VMEbus interrupter.

We now describe in detail the registers of the VME Latch FIFO. The local address of each register is given. The base address (A23 - A4) is selected by DIP switches on the board (see "Configuring The Module").

1. CONTROL/STATUS REGISTER (CSR) [addr = 0]

The CSR is used to configure the operating conditions of the VME Latch FIFO, as well as provide the current status of the device.

Bits are read/write unless otherwise indicated.

(0) MODE - 0 - STROBE
1 - LATCH

(1) ENABLE FRONT PANEL - setting this bit enables STROBES or GATES to enter the module and record data patterns.

(2) USE BUFFER SIGNAL - setting this bit causes buffering of data only on the assertion of the external BUFFER signal (e.g. Trigger Supervisor Level 3 Accept). Clearing this bit causes buffering to occur on the STROBE or GATE input, depending on the chosen mode (CSR bit 0).

(3) ENABLE INTERRUPT - setting this bit allows a VME interrupt to be generated whenever the data buffer word count is equal to the value stored in the Word Count Register.

(4) - (6) RESERVED

(7) RESET - (Write only) asserting this bit generates a pulse that clears CSR bits (0)-(3), (11)-(15), clears the Interrupt Register, Word Count Level Register, and Word Count Register.

The following are Read only STATUS bits unless otherwise indicated.

(8) - (10) INTERRUPT LEVEL - binary encoded value of the VMEbus interrupt level LEVEL (0) - (3) that has been selected for the interface by the DIP switches on the module.

(11) INTERRUPT CYCLE ACTIVE - when set it indicates that a VME interrupt has been generated but not yet been acknowledged.

(12) FIFO WRITE ERROR FLAG - when set it indicates that a write to a FULL memory has been attempted. This results in a loss of data. Writing a ‘1’ to this bit will clear the error flag.

(13) FIFO READ ERROR FLAG - when set it indicates that a read of an EMPTY memory has been attempted. Non-valid data is returned. Writing a '1' to this bit will clear the error flag.

(14) COUNT MARK FLAG - when set it indicates that the number of data words in the memory is greater than or equal to the programmed count (Word Count Level Register).

(15) DATA AVAILABLE - when set it indicates that the memory has at least one valid data word available to be read out.

2. INTERRUPT REGISTER [addr = 2]

The Interrupt Register is programmed with the 8-bit interrupt ID. During the interrupt acknowledge cycle the reading of this register allows the interrupt handler to identify the VME Latch FIFO as the source of the interrupt request.

All bits are Read/Write.

(0) - (7) INTERRUPT ID

(8) - (15) UNUSED - (read as 1)

3. WORD COUNT LEVEL REGISTER [addr = 4]

The Word Count Level Register contains a stored value which is compared to the value of the Word Count Register. When the word count is greater than or equal to the stored level, bit 14 in the CSR is set. A VME interrupt is generated in addition if CSR bit 3 is set.

Bits of the register are Read/Write.

(0) - (15) COUNT LEVEL

4. WORD COUNT REGISTER [addr = 6]

The Word Count Register contains the current number of data words stored in the memory. (15-bit counter - maximum 32K words)

Bits of the register are Read only.

(0) - (14) WORD COUNT

5. DATA REGISTER [addr = 8]

The DATA REGISTER contains the 16-bit latched input pattern.

Bits (0)-(14) of the register are Read only. Writing a 1 to bit 15 re-enables the module to generate interrupts (requires CSR bit 3 to be set also).

(0) - (15) LATCHED DATA PATTERN from inputs Data_0 - Data_15.

Configuring The Module

(a) VMEbus Base Address - this is set using the 20 elements of DIP switches identified in Figure 2. Switch element 1 is A4, ..., Switch element 20 is A23. An open switch defines a '1'.

(b) VMEbus Interrupt Level - this is set using the 3 element DIP switch identified in Figure 2. The level is binary encoded - Switch element 1 is bit 0, ..., Switch element 3 is bit 2. An open switch defines a '1'.

(c) Data Cable Termination - socketed SIP resistors are used to terminate the data cable. The resistor locations are shown in Figure 2 and the values are listed below (assuming the cable has a characteristic impedance of 100 ohms). The resistors MUST be present if the Latch FIFO is the last module along the cable. When daisy chained connections are desired and the Latch FIFO is not the last module, the SIP resistors should be removed. Each set of 3 SIP resistors is tied to 4 data lines, so the termination or non-termination of lines must be done in groups of 4 data inputs.

Data Inputs	Location	Package	Resistor	Comment
Data 0 - 3	R22	SIP8	100 ohm, isolated	
	R21	SIP8	1.8K ohm, bussed	NOTE PIN 1
	R23	SIP8	3.9K ohm, bussed	NOTE PIN 1
Data 4 - 7	R16	SIP8	100 ohm, isolated	
	R15	SIP8	1.8K ohm, bussed	NOTE PIN 1
	R17	SIP8	3.9K ohm, bussed	NOTE PIN 1
Data 8 - 11	R12	SIP8	100 ohm, isolated	
	R11	SIP8	1.8K ohm, bussed	NOTE PIN 1
	R13	SIP8	3.9K ohm, bussed	NOTE PIN 1
Data 12 - 15	R6	SIP8	100 ohm, isolated	
	R5	SIP8	1.8K ohm, bussed	NOTE PIN 1
	R7	SIP8	3.9K ohm, bussed	NOTE PIN 1

(The 1.8K and 3.9K ohm resistors serve to bias the differential inputs. The biasing of the input receivers is necessary to assure that unconnected channels do not oscillate, a condition that may inject noise into adjacent channels that are used. This biasing causes an unconnected input channel to be read as ‘0’.)

(d) GATE OUT / GATE IN - a twisted-pair cable or shunts (jumpers) can join GATE OUT to GATE IN at the control port connector when an internally generated gating signal is desired. If shunts are used, connect pin 15 to pin 17, and pin 16 to pin 18. The GATE OUT width is adjustable by a potentiometer (see Figure 2). The nominal range is from 10 to 70 ns, but can be extended with the addition of a capacitor (see DAQ group).

(e) Input Power - can be chosen to be -12V or +12V by installing the DC-DC converter in different locations (see Figure 2). The -5.2V power needed for ECL logic is derived from the +12V or - 12V supplied by the VME backplane. The option of +/- power input can be important if multiple Latch Modules (or other boards that use 12V) are installed in the same VME chassis. The Latch Module uses about 1 amp of the 12V rail, and the VME chassis may provide as little as 5 amps each of -12V and +12V. By mixing -12V and +12V modules in the same chassis, overloading of the power supply may be avoided. Please contact the DAQ group if reconfiguration of the 12V input power is necessary.

Visual Indicators

7 LEDs visible through the front panel indicate the operating condition and status of the module (see Figure 1). From top (1) to bottom (7) the LEDs, when lit, convey the following information:

(1) STROBE or GATE present at front panel.

(2) STROBE mode selected.

(3) LATCH mode selected

(4) WRITE memory.

(5) READ memory.

(6) FULL Memory.

(7) EMPTY memory.

2 LEDs on the board indicate the powered status of the module (see Figure 2). The LED at the bottom of the board indicates that +5V is present when it is lit. The LED at the middle of the board indicates that -5.2V (derived from -12V or +12V) is present when it is lit. A blown fuse on the board is the most likely cause of either of these LEDs not to be lit. All fuses have a rating of 3 amps, and their locations are shown in Figure 2.