16-Channel Discriminator/Scaler VME Module

Manual

(DRAFT)

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Overview

The 16-Channel Discriminator/Scaler contains 16 non-updating discriminators with programmable digital delay and two 32-bit scalers per channel. The discriminator pulses are output as differential ECL logic levels through a front-panel header. An analog multiplexer permits monitoring of any one of 16 discriminator inputs (after gain).

The discriminators reside on four 4-channel socketed modules. Each channel contains a 4x gain amplifier, buffered monitor, comparator, and a non-updating pulser. All discriminator thresholds and pulse widths are voltage-programmable with a potentiometer or 12-bit DAC.

The digital delay circuit delays each discriminator pulse up to 248nS in 8nS steps. It is implemented with one 32-bit 125MHz shift register per channel. For each channel, software selects which shift location is output to the scalers.

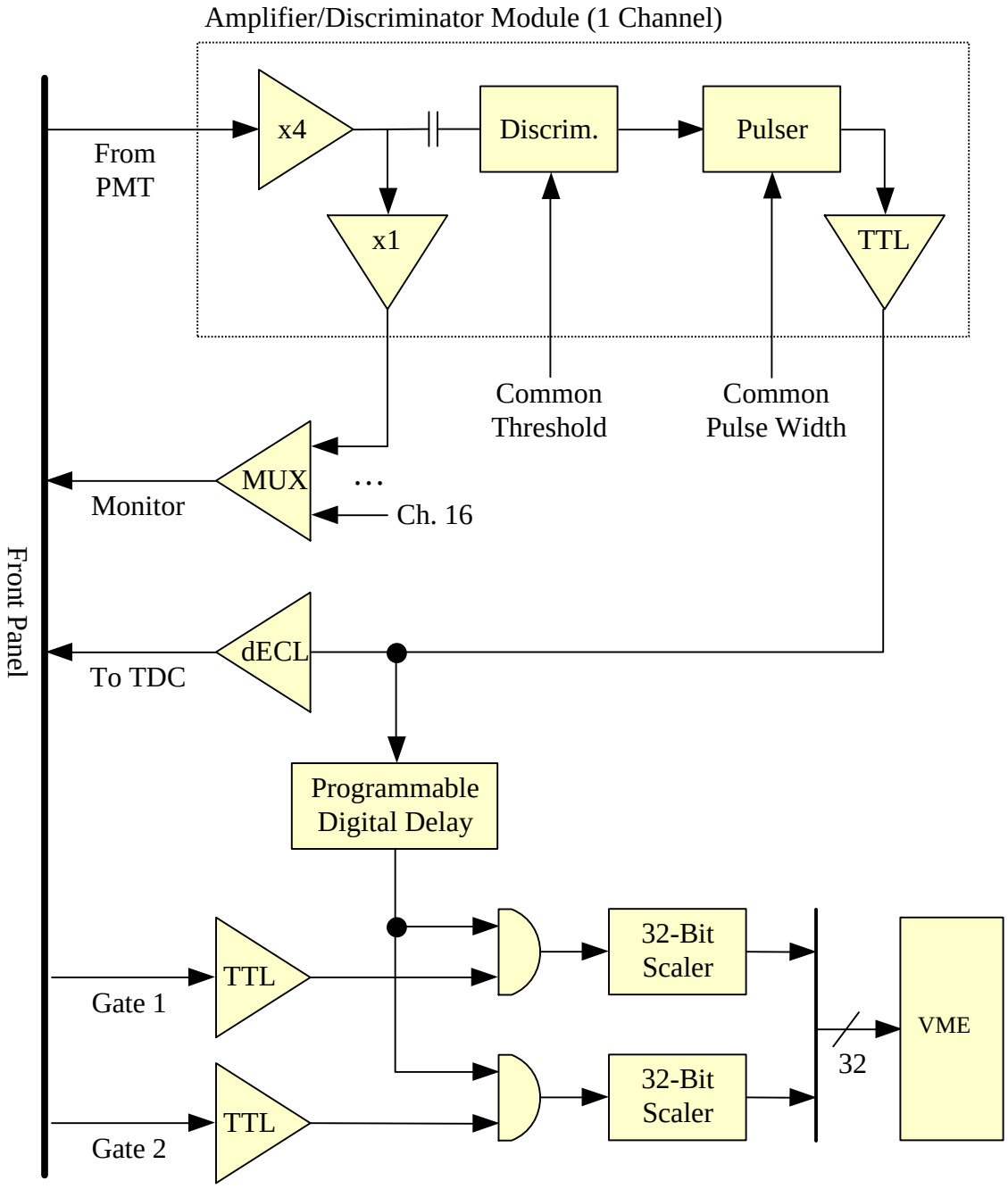
There are two 32-bit scalers for each discriminator. One scaler is gated with the Gate1 (NIM) input and the other scaler is gated with the Gate2 (NIM) input. Scalers can be latched, read, and cleared by software.

All discriminator inputs are buffered (after gain) and multiplexed. Dual buffered multiplexer outputs are provided on the front panel. A front-panel toggle switch selects the channel and an LED indicates the channel selected. Selection can also be made through software.

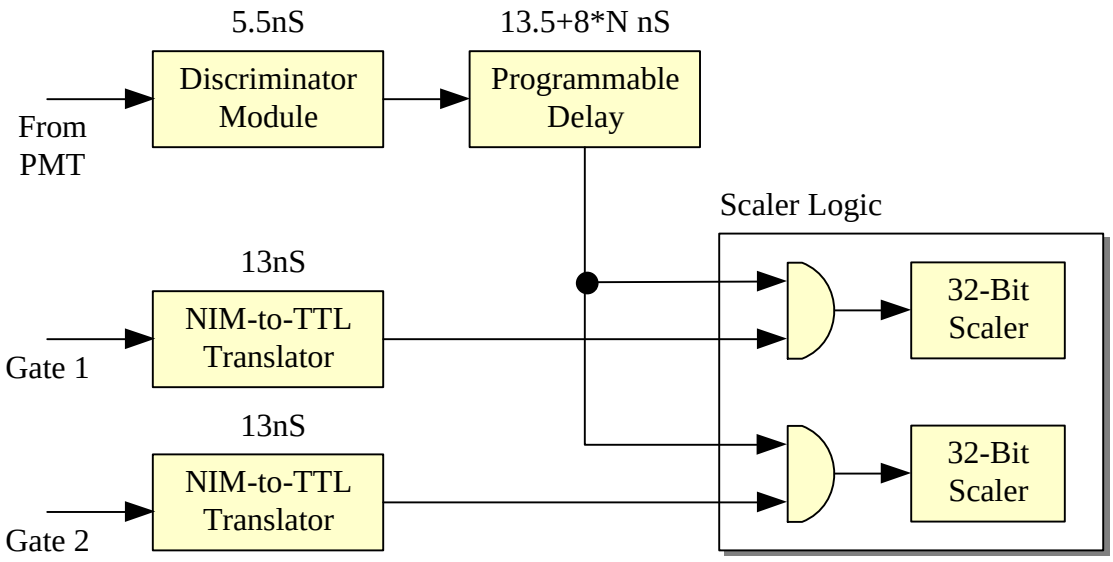
Discriminator outputs are provided as dECL levels on the front panel for interfacing with TDCs.

The VME interface is A32/D32 only with support for interrupts.

Discriminator/Scaler Block Diagram
Single Channel



On-Board Signal Delays (1 Channel)

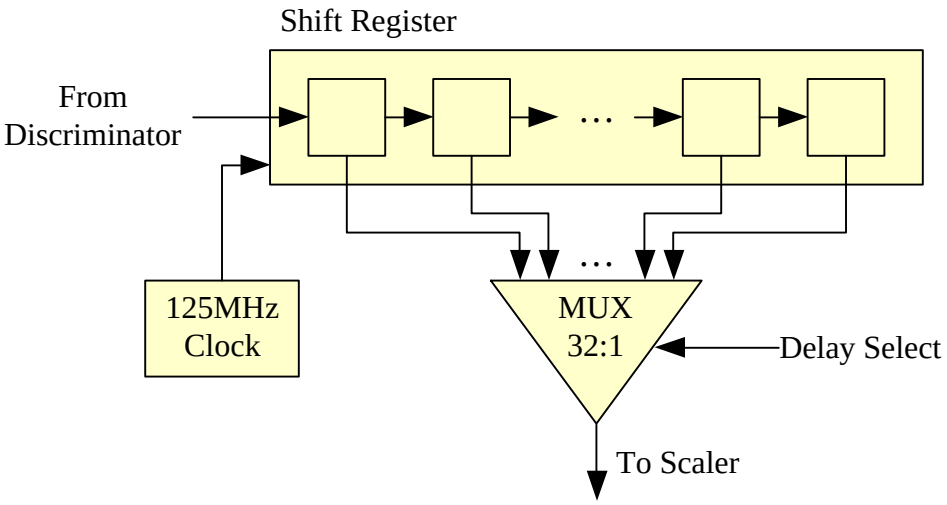


E-Counter Delay at Scaler Logic = 19+8*N nS
Differential Delay at Scaler Logic = E-Counter Delay – Gate Translator Delay
= 6 + 8*N nS (Gate leads discriminator)

Where N = 0 to 32 (integer)

Differential delay in Scaler Logic assumed to be less than 1nS.

Digital Delay Circuit (1 Channel)



Specifications

General		
Power consumption (no load)	+12V, 0.65A; -12V, 0.65A; +5V, 1.5A	
Fuses	+12V, 1A; -12V, 1A; +5V, 4A	
On-board power	-5V, 2.54A; +2.5V, 0.12A; +3.3V, 0.09A	
Dimensions	6U VME, single-wide	
I/O connectors	MUX Output:	2 LEMO
	PMT Input:	16 LEMO
	Gate Input:	2 LEMO
	dECL Output:	34-pin Header
On-board connectors	JTAG:	10-Pin header for Altera ByteBlaster programmer
	AUX:	Dual 72-pin connectors for future upgrade
LEDs	Green (2):	+2.5V, +3.3V
	Yellow (18):	Status A, Status B, MUX channel select (1-16)
	All yellow LEDs and MUX are disabled on voltage error.	
Jumpers	JP1:	C-P = Threshold set by potentiometer
	JP2:	C-D = Threshold set by DAC
Analog Inputs	From PMT	
Channels	16	
Signal level	<±800mV with gain = +4, diode-clamped to ±1.5V, DC-Coupled	
Termination	50-Ohm	
Gate Inputs	Gates scalers	
Channels	2	
Signal Level	NIM	
Analog Monitor Outputs		
Channels	2, buffered	
Signal level	± 3.5V, DC-Coupled	
Termination	50-Ohm, source-terminated	
Amplifier/Discriminator Module		
Channels per module	4	
Voltage gain	+4	
Min rise time (input-to-discriminator)	1.5nS	
Min rise time (input-to-buffer)	1.5nS	
Threshold control	0V ? - 4.5V control voltage = 0V ? -1V threshold	
Minimum useful threshold	10mV	
Pulser type	Non-updating	
Pulser control	-2.0V ? -4.5V control voltage = 8nS ? 90nS pulse width	
Pulser output level	TTL	
Channel-to-channel crosstalk	<1mV for rise time = 1nS and Vin = -200mV	
Discriminator baseline noise	<±2.5mV	
Amplifier output offset (Av = +4)	12±3 mV	
Pulser dead-time	<5nS	
Monitor buffer	Gain = +1; located after gain stage (Gain=+4)	
Monitor buffer output range	±0.7V with Gain=+4	

dECL Outputs

Channels	16
Connector	34-pin header in LeCroy TDC format.
Signal	Discriminator pulser

Common Discriminator Control

Threshold	Set by potentiometer or DAC (jumper selectable).
Pulse width	Set by potentiometer or DAC (jumper selectable).
Signal distribution	All channels have individually buffered threshold pulse width.
DAC	12-Bit; Set to zero by logic after reset.
Threshold control	DAC/Potentiometer: zero-scale = 0V, full-scale = -1V
Pulse width control	DAC/Potentiometer: zero-scale = NO PULSE, full-scale = 90nS
Minimum pulse width	8nS with DAC setting of 5mV

Analog Multiplexer

Configuration	1:16
Control	Front-panel toggle switch cycles through channels; VME control
Outputs	2, buffered, front-panel
Gain from MUX in to buffer out	+0.25 (with 50-ohm termination)
Gain from discr. in to buffer out	+1 (with discriminator gain = +4)
Coupling between input modules	<1mV for Vin = -200mV and rise times = 1.5 nS
Coupling due to:	
Channel 1 trigger only	4.5mV zero-to-peak
Channel 2 trigger only	2.5mV
All other channels (single trigger)	= 1.7mV

Digital Delay

Delay step size	8nS, VME controlled
Delay range	0nS ? 248nS
Uncertainty	0nS ? +8nS due to synchronization of discriminator pulse.
Maximum effective rate	62.5MHz with discriminator set to 8nS. This is the maximum rate to produce a high-low pattern at delay output for scalers.
Delay from discriminator input to	
Digital delay input:	5.5nS
Scaler input:	19nS with delay setting = 0
Delay from gate input to scaler logic	13nS

Scalers

Quantity	2 per discriminator channel (32 total)
Width	32-bit
Input source	Logical AND of digital delay output and gate.
Gating	GATE1 gates scaler 1 of all channels, GATE2 gates scaler 2 of all channels.
Maximum rate	140Mhz
Readout dead-time	None
Control	VME latch, read, clear, scaler overflow status

VME Interface

Compliance	A32/D32 only; D16/D08/unaligned not supported
Registers	53
Address space used	128 32-bit words (A08..A02) in A32 or A24;

Misc.

Voltage monitor	Monitors +5V, -5V, +3.3V, +2.5V; Error reported for 5% droop. All yellow LEDs and MUX are disabled on voltage error.
Temperature sensor	Monitors discriminator module temperature (next revision)
EEPROM	Optional – Stores configuration parameters

Specifications to be improved in production boards

Large signal isolation leakage within amp/discriminator module measured input-to-monitor out.	|Vin| = 200mV : None detectable |Vin| = 300mV : = 2.5mV |Vin| = 400mV : = 13mV |Vin| = 500mV : = 40mV |Vin| = 600mV : = 75mV |Vin| = 800mV : = 140mV
Crosstalk within amp/discriminator module measured input-to-monitor out Vin = -200mV Discriminator-in to monitor-out, Within input module, No trigger, 0-to-peak measurement	Rise time = 1nS : = 3mV Rise time = 10nS : = 2mV Rise time = 40nS : = 3mV Rise time = 50nS : = 0.3mV Rise time = 70nS : = 0.1mV

Registers

Register	Description	Read Function	Write Function
00	CSR	Read CSR	Write CSR
01	Threshold	Read Threshold	Write Threshold
02	Pulse Width	Read Pulse Width	Write Pulse Width
03	Gate1 Counter	Read Counter	Latch Gate1 Counter
04	Gate2 Counter	Read Counter	Latch Gate2 Counter
05..1F	UNUSED	0x00000000	N/A
20	Channel 1, Scaler1	Read scaler	Latch all scalers
21	Channel 2, Scaler1	Read scaler	Latch all scalers
22	Channel 3, Scaler1	Read scaler	Latch all scalers
23	Channel 4, Scaler1	Read scaler	Latch all scalers
24	Channel 5, Scaler1	Read scaler	Latch all scalers
25	Channel 6, Scaler1	Read scaler	Latch all scalers
26	Channel 7, Scaler1	Read scaler	Latch all scalers
27	Channel 8, Scaler1	Read scaler	Latch all scalers
28	Channel 9, Scaler1	Read scaler	Latch all scalers
29	Channel 10, Scaler1	Read scaler	Latch all scalers
2A	Channel 11, Scaler1	Read scaler	Latch all scalers
2B	Channel 12, Scaler1	Read scaler	Latch all scalers
2C	Channel 13, Scaler1	Read scaler	Latch all scalers
2D	Channel 14, Scaler1	Read scaler	Latch all scalers
2E	Channel 15, Scaler1	Read scaler	Latch all scalers
2F	Channel 16, Scaler1	Read scaler	Latch all scalers
30	Channel 1, Scaler2	Read scaler	Latch all scalers
31	Channel 2, Scaler2	Read scaler	Latch all scalers
32	Channel 3, Scaler2	Read scaler	Latch all scalers
33	Channel 4, Scaler2	Read scaler	Latch all scalers
34	Channel 5, Scaler2	Read scaler	Latch all scalers
35	Channel 6, Scaler2	Read scaler	Latch all scalers
36	Channel 7, Scaler2	Read scaler	Latch all scalers
37	Channel 8, Scaler2	Read scaler	Latch all scalers
38	Channel 9, Scaler2	Read scaler	Latch all scalers
39	Channel 10, Scaler2	Read scaler	Latch all scalers
3A	Channel 11, Scaler2	Read scaler	Latch all scalers
3B	Channel 12, Scaler2	Read scaler	Latch all scalers
3C	Channel 13, Scaler2	Read scaler	Latch all scalers
3D	Channel 14, Scaler2	Read scaler	Latch all scalers
3E	Channel 15, Scaler2	Read scaler	Latch all scalers

Register	Description	Read Function	Write Function
3F	Channel 16, Scaler2	Read scaler	Latch all scalers
40	Channel 1 Delay	Read delay	Write delay
41	Channel 2 Delay	Read delay	Write delay
42	Channel 3 Delay	Read delay	Write delay
43	Channel 4 Delay	Read delay	Write delay
44	Channel 5 Delay	Read delay	Write delay
45	Channel 6 Delay	Read delay	Write delay
46	Channel 7 Delay	Read delay	Write delay
47	Channel 8 Delay	Read delay	Write delay
48	Channel 9 Delay	Read delay	Write delay
49	Channel 10 Delay	Read delay	Write delay
4A	Channel 11 Delay	Read delay	Write delay
4B	Channel 12 Delay	Read delay	Write delay
4C	Channel 13 Delay	Read delay	Write delay
4D	Channel 14 Delay	Read delay	Write delay
4E	Channel 15 Delay	Read delay	Write delay
4F	Channel 16 Delay	Read delay	Write delay
50..7F	UNUSED	Error (BERR)	Error (BERR)

Register Format

Register	Bit	Function	Notes
00	31..24	Interrupt Vector	
	23..20	UNUSED	Read = 0, Write = N/A
	19..17	Interrupt Level	000 = Disable Interrupts
	16	Interrupt Status	
	15	+5V Status	
	14	+3.3V Status	
	13	+2.5V Status	
	12	-5V Status	
	11	Monitor Disable	
	10	Monitor Select 3	
	9	Monitor Select 2	
	8	Monitor Select 1	
	7	Monitor Select 0	
	6	Gate 2 On	1 = Force Gate 2 On Also clears Gate 2 counter
	5	Gate 1 On	1 = Force Gate 1 On Also clears Gate 1 counter
	4	Clear Gate 2 Counter	Level (not pulsed)
	3	Clear Gate 1 Counter	Level (not pulsed)
	2	Clear Scaler Overflow	Level (not pulsed)
	1	Scaler Overflow	
	0	Clear Scalers	Level (not pulsed)
01	31..12	UNUSED	Read = 0, Write = N/A
	11..0	Threshold DAC	Range = 0V ? -1V Threshold
02	31..12	UNUSED	Read = 0, Write = N/A
	11..0	Pulse Width DAC	Range = 0V ? 90nS Pulse Width
03	31..0	Gate 1 Counter	
04	31..0	Gate 2 Counter	
20..3F	31..0	Scaler Count	Write = Latch scaler values Read = Get data since last latch
40..4F	31..8	UNUSED	Read = 0, Write = N/A
	4..0	Delay	

dECL Output Connector J1

Pin	Function	Pin	Function
1	Ch 1 +	2	Ch 1 -
3	Ch 2 +	4	Ch 2 -
5	Ch 3 +	6	Ch 3 -
7	Ch 4 +	80	Ch 4 -
9	Ch 5 +	10	Ch 5 -
11	Ch 6 +	12	Ch 6 -
13	Ch 7 +	14	Ch 7 -
15	Ch 8 +	16	Ch 8 -
17	Ch 9 +	18	Ch 9 -
19	Ch 10 +	20	Ch 10 -
21	Ch 11 +	22	Ch 11 -
23	Ch 12 +	24	Ch 12 -
25	Ch 13 +	26	Ch 13 -
27	Ch 14 +	28	Ch 14 -
29	Ch 15 +	30	Ch 15 -
31	Ch 16 +	32	Ch 16 -
33	No Connect	34	No Connect

JTAG Connector J2

Pin	Function	Pin	Function
1	TCK	2	GND
3	TDO	4	+3.3V
5	TMS	6	N/C
7	N/C	8	N/C
9	TDI	10	GND

NOTES

- JTAG connector is compatible with Altera ByteBlaster serial download cable.
- +3.3V and GND pins are driven on board.
- TCK is pulled to ground with 1K resistor.
- TDI, TMS are pulled to +3.3V with 1K resistor.

JTAG Device Chain
Device 1: EP4QC100
Device 2: EPM3064ATC100

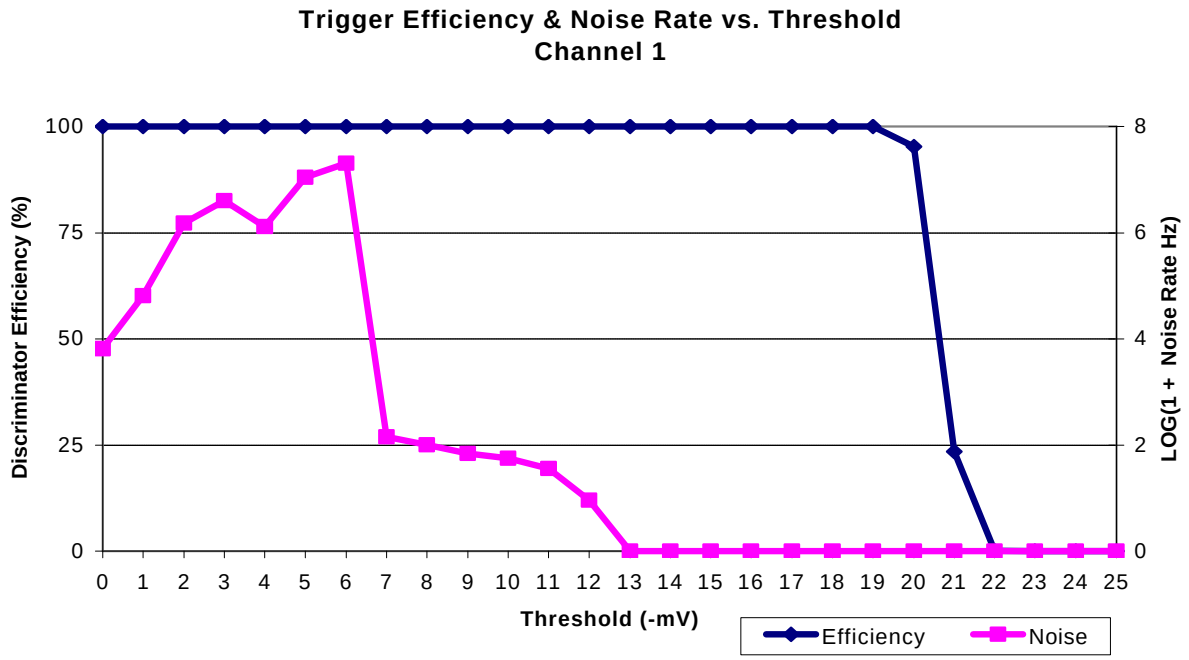
Aux. Connectors J3/J4

J3			
Pin	**Function**	**Pin**	**Function**
1	A09	2	D15
3	A08	4	D14
5	GND	6	D13
7	A07	8	D12
9	A06	10	D11
11	GND	12	D10
13	A05	14	D09
15	A04	16	D08
17	GND	18	GND
19	A03	20	D07
21	A02	22	D06
23	GND	24	D05
25	DISCR1	26	D04
27	DISCR2	28	D03
29	GND	30	D02
31	DISCR3	32	D01
33	DISCR4	34	D00
35	GND	36	GND
37	DISCR5	38	D16
39	DISCR6	40	D17
41	GND	42	D18
43	DISCR7	44	D19
45	DISCR8	46	D20
47	GND	48	D21
49	DISCR9	50	D22
51	DISCR10	52	D23
53	GND	54	GND
55	DISCR11	56	D24
57	DISCR12	58	D25
59	GND	60	D26
61	DISCR13	62	D27
63	DISCR14	64	D28
65	GND	66	D29
67	DISCR15	68	D30
69	DISCR16	70	D31
71	GND	72	GND

J4			
Pin	**Function**	**Pin**	**Function**
1	GND	2	GND
3	+5V	4	PLD1
5	+5V	6	PLD2
7	+5V	8	PLD3
9	GND	10	GND
11	+3.3V	12	PLD4
13	+3.3V	14	PLD5
15	+3.3V	16	PLD6
17	GND	18	GND
19	+2.5V	20	PLD7
21	+2.5V	22	PLD8
23	+2.5V	24	PLD9
25	GND	26	GND
27	-5V	28	PLD10
29	-5V	30	PLD11
31	-5V	32	PLD12
33	GND	34	GND
35	P2:C1	36	P2:A1
37	P2:C2	38	P2:A2
39	P2:C3	40	P2:A3
41	P2:C4	42	P2:A4
43	GND	44	GND
45	P2:C5	46	P2:A5
47	P2:C6	48	P2:A6
49	P2:C7	50	P2:A7
51	P2:C8	52	P2:A8
53	GND	54	GND
55	P2:C9	56	P2:A9
57	P2:C10	58	P2:A10
59	P2:C11	60	P2:A11
61	P2:C12	62	P2:A11
63	GND	64	GND
65	P2:C13	66	P2:A13
67	P2:C14	68	P2:A14
69	P2:C15	70	P2:A15
71	P2:C16	72	P2:A16

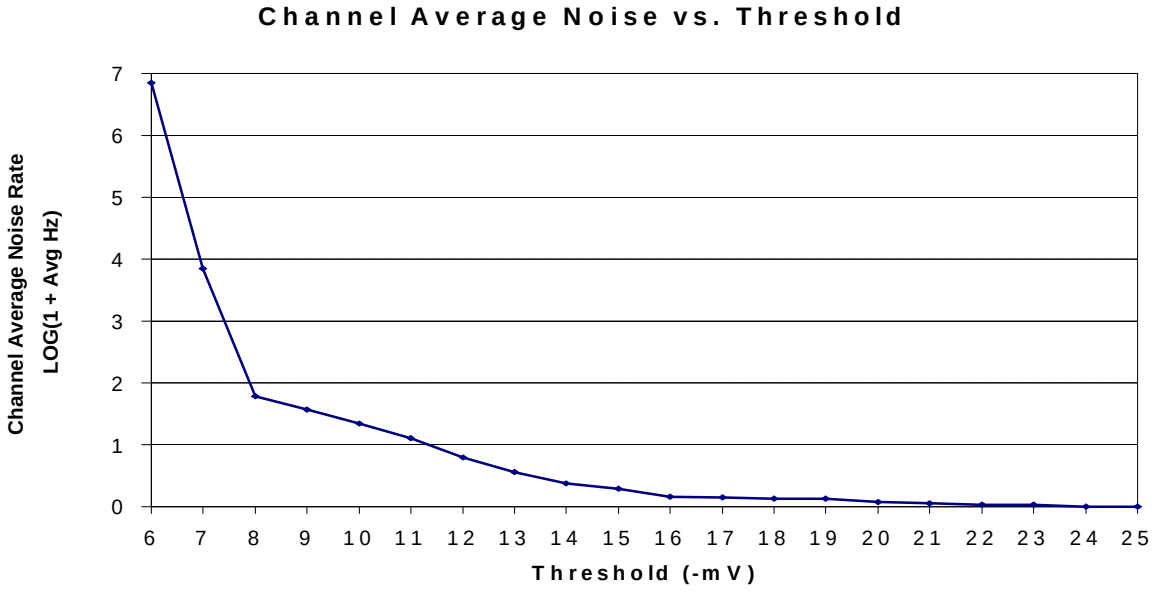
Amplifier/Discriminator Module Pin Assignments

Pin	Function	Pin	Function
1	Ch1 In	50	Ch1 Pulse Out
2	GND	49	GND
3	Ch1 Monitor	48	Ch1 Pulse Width
4	GND	47	Ch1 Threshold
5	EN1	46	+5V
6	-5V	45	-5V
7	+5V	44	GND
8	Ch2 In	43	Ch2 Pulse Out
9	GND	42	GND
10	Ch2 Monitor	41	Ch2 Pulse Width
11	GND	40	Ch2 Threshold
12	EN2	39	+5V
13	EN3	38	-5V
14	GND	37	GND
15	Ch3 In	36	Ch3 Pulse Out
16	GND	35	GND
17	Ch3 Monitor	34	Ch3 Pulse Width
18	GND	33	Ch3 Threshold
19	EN4	32	+5V
20	-5V	31	-5V
21	+5V	30	GND
22	Ch4 In	29	Ch4 Pulse Out
23	GND	28	GND
24	Ch4 Monitor	27	Ch4 Pulse Width
25	GND	26	Ch4 Threshold



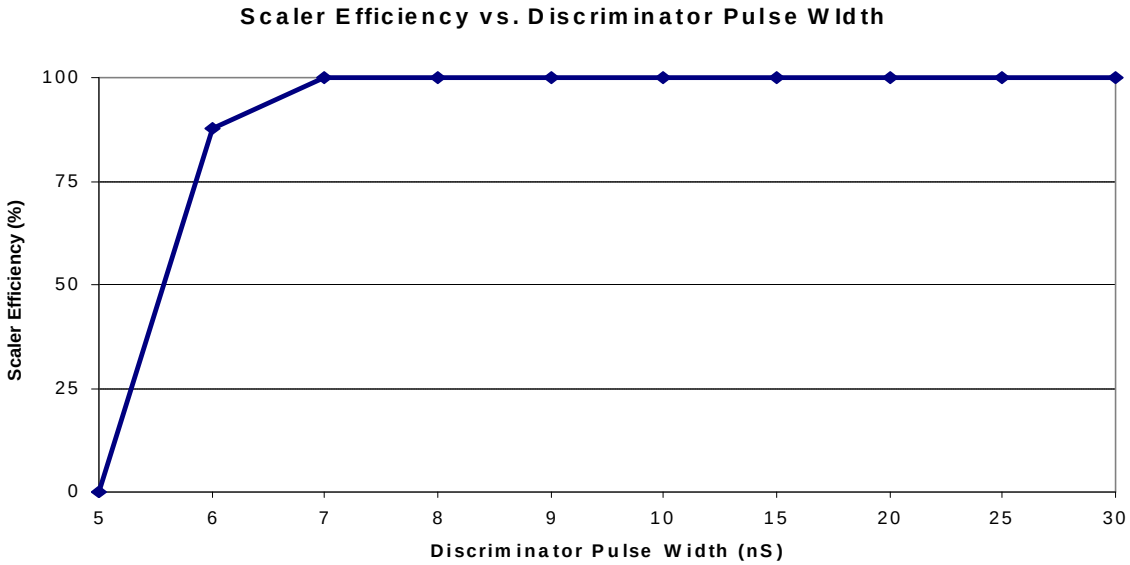
Threshold range for 100% efficiency:
Without noise: 13mV = Vth = 18mV
<100Hz noise: 8mV = Vth = 18mV

Test Conditions
Discriminator Input = 5mV, 5nS
Discriminator Output = 20nS

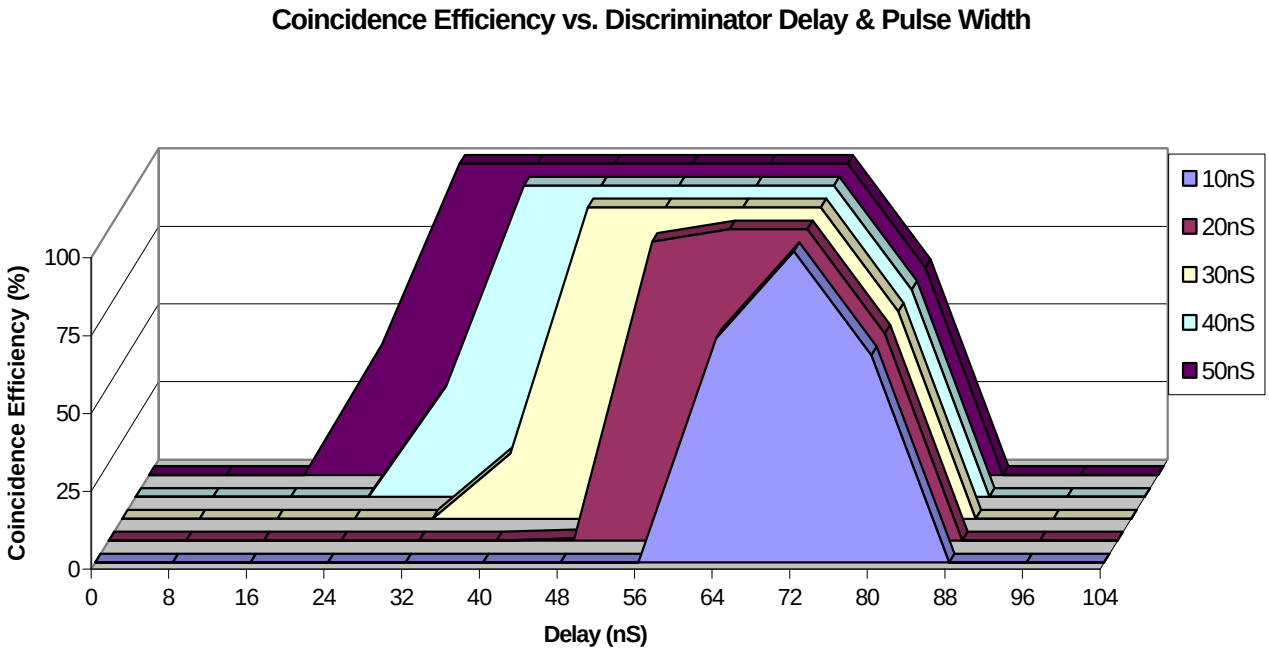


Note: Minimum useful threshold for < 100Hz Noise is 10mV

Test Conditions
Discriminator Input = -5mV, 5nS
Discriminator Output = 20nS



Note: Minimum useful Pulse Width = 8nS



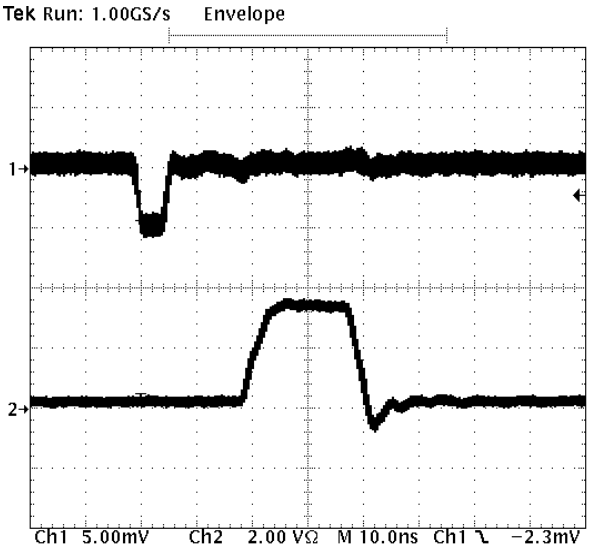
Notes

- Coincidence between input and gate can be achieved with proper delay settings.
- A discriminator pulse width of ≥25nS should be sufficient to detect coincidence with an 8nS gate.

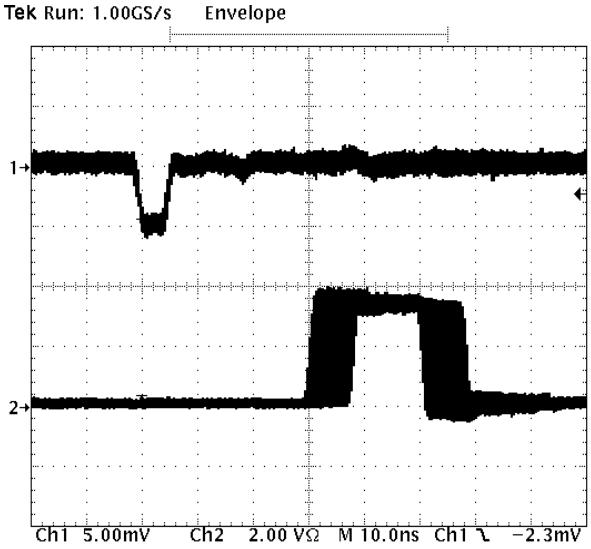
Test Conditions

Discriminator Input = -5mV, 5nS
Gate = 8nS
Gate lags discriminator input by 90nS
Simulates E-counter delay.

Graph 1: Digital Delay Input
20nS Pulse



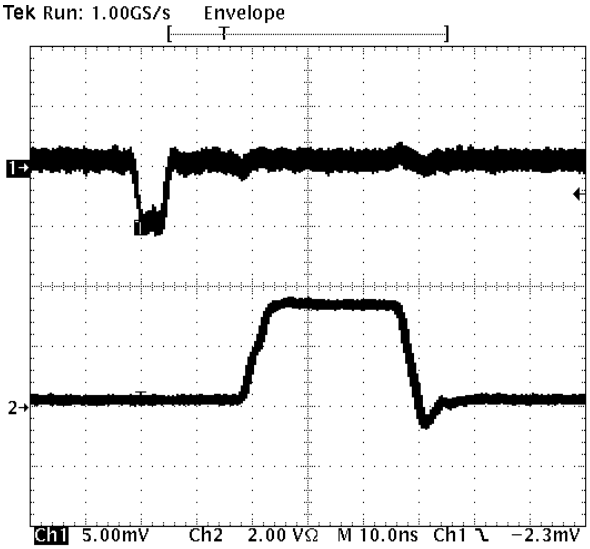
Graph 2: Digital Delay Output
20nS Pulse



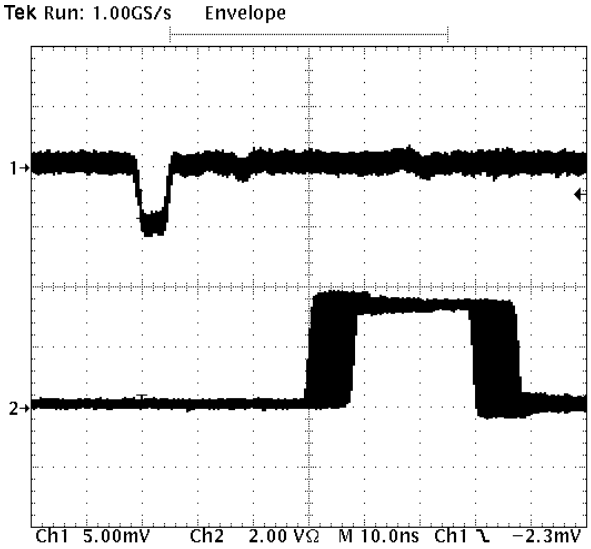
Digital delay circuit samples pulse shown on left at 125MHz.
Delay output synchronization jitter and reshaping is indicated on right.
Jitter is always 8nS on independent of pulse width.

Top Right: Delay should be set for coincidence within the 12nS center of delayed pulse.
Bottom Right: Delay should be set for coincidence within the 24nS center of delayed pulse

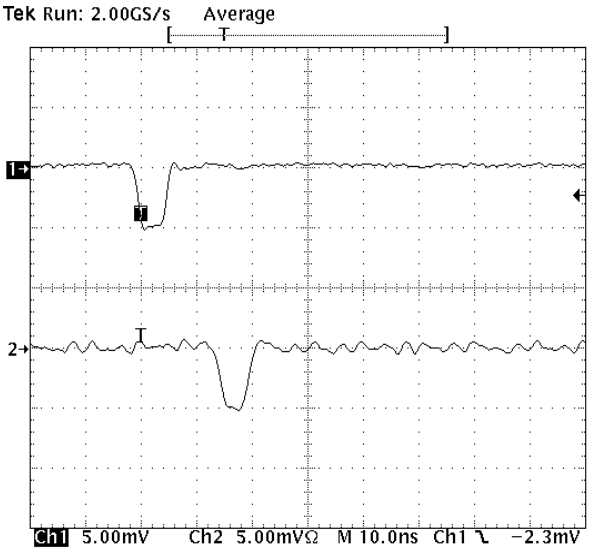
Graph 3: Digital Delay Input
30nS Pulse



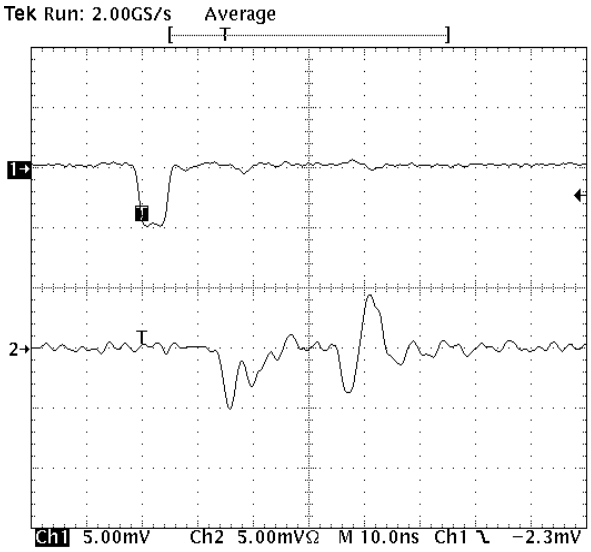
Graph 4: Digital Delay Output
30nS Pulse



Graph 5: Monitor Output, Pulser Off
5mV Input



Graph 6: Monitor Output, Pulser On
5mV Input

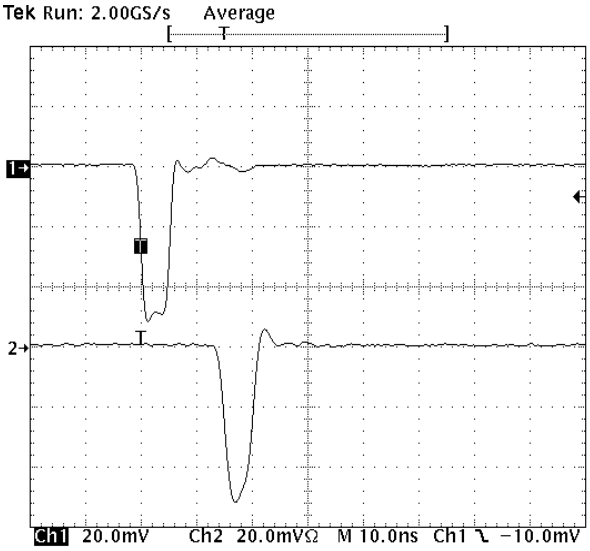


The discriminator pulser introduces 5mV noise in the monitor multiplexer. This noise:

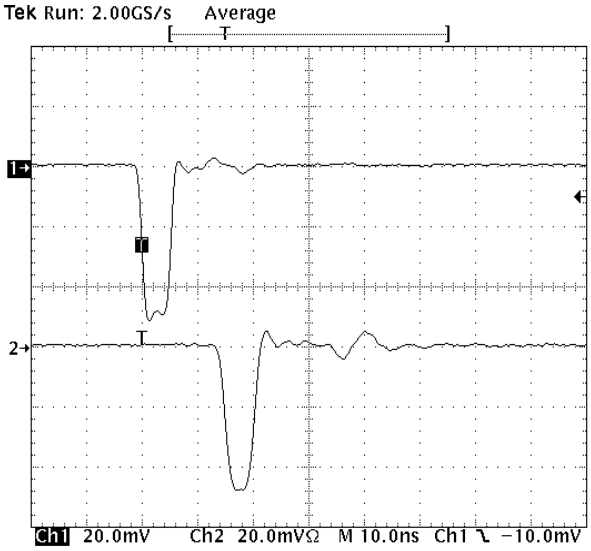
- Appears on both rising and falling edges of discriminator pulse.
- Is constant in magnitude and shape.
- Is additive at mux for all channels.
- Couples through board power.
- Couples <2mV to discriminator threshold noise.

Top Graphs: Noise is additive to signal at monitor and is a large component of small signals.
Bottom Graphs: Noise is additive but is a much smaller contribution to large signals.

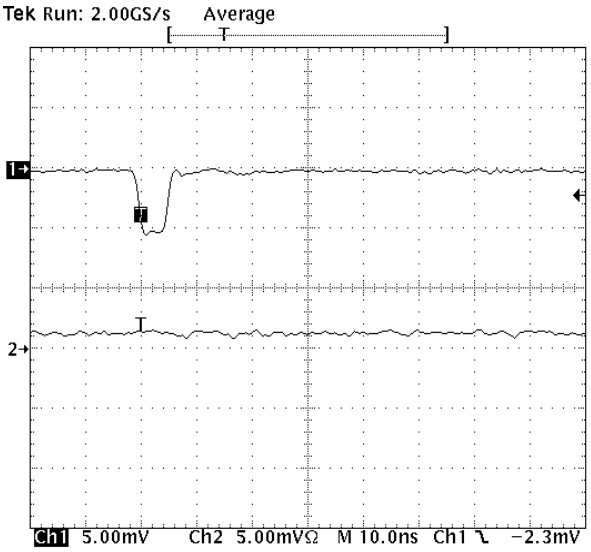
Graph 7: Monitor Output, Pulser Off
50mV Input



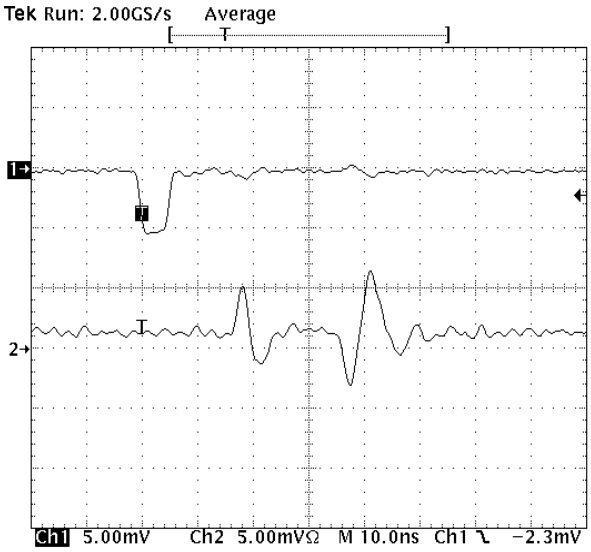
Graph 8: Monitor Output, Pulser On
50mV Input



Graph 9: Channel 2 Monitor
No Trigger

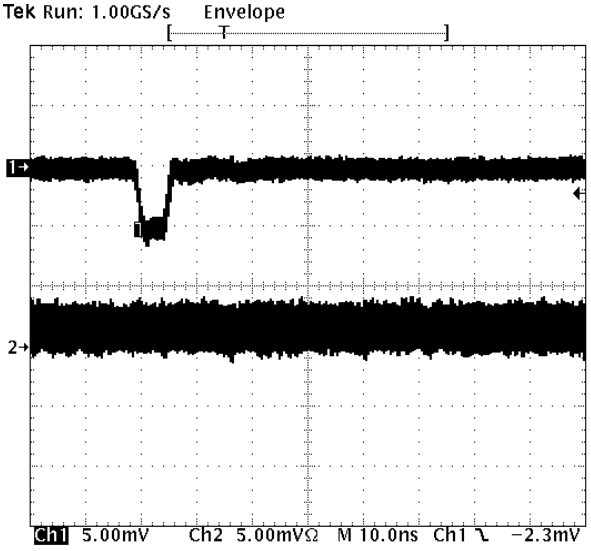


Graph 10: Channel 2 Monitor
Channel 1 Trigger

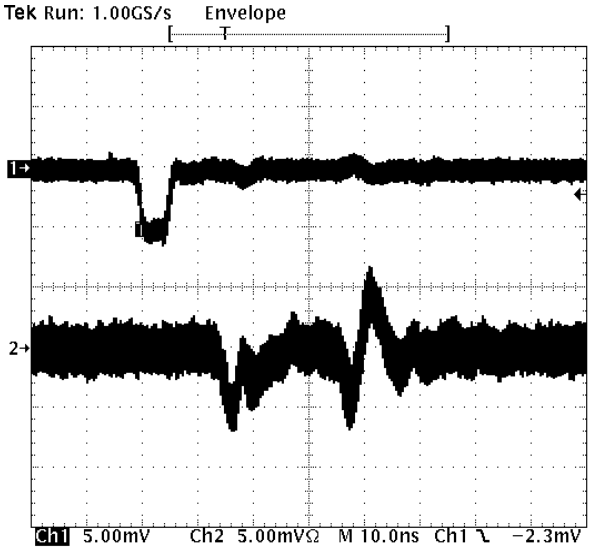


Top Graphs:	Discriminator pulse noise shown with and without triggers on channel being monitored
Bottom Graphs:	Envelope indicates fraction of discriminator pulse noise over baseline noise. Contribution is approx. ±4mV above baseline or approx 2.4 times baseline noise.

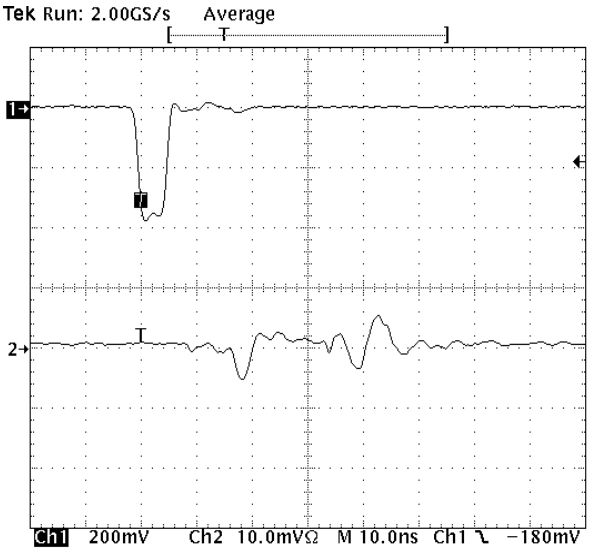
Graph 11: Channel 2 Monitor Noise
No Trigger



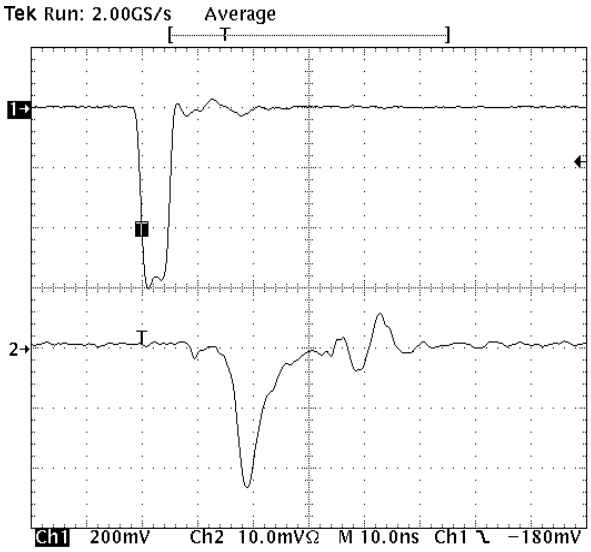
Graph 12: Channel 2 Monitor Noise
Channel 1 Trigger



Graph 13: Monitor - Next to Active Channel
200mV Input



Graph 14: Monitor - Next to Active Channel
600mV Input



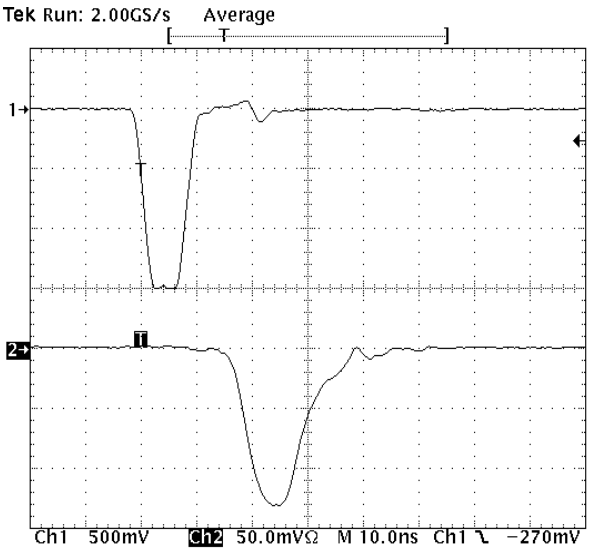
The monitor mux provides double-buffer isolation on 12 disabled channels but only single-buffer isolation on the three disabled channels that share the discriminator module with the selected channel.

It was discovered that large-signal isolation "leakage" appears on the single-isolated channels and adds to the monitor signal at the mux. Note that this effects the monitor only – not the discriminator.

This problem will be solved on the production boards by double isolating all channels.

Top Left:	400mV on discriminator channel 1 (upper trace) does not leak to channel 2 (lower trace).
Top Right:	Leakage from ch.1 to ch.2 shows up at 600mV but contribution is small (20mV).
Bottom Left:	Leakage is at maximum at 1.5V due to gain amplifier (x4) saturation. Contribution is 130mV.
Bottom Right:	No leakage is shown when monitoring a different module through double isolation.

Graph 15: Monitor - Next to Active Channel
1500mV Input



Graph 16: Monitor - Different Module
1500mV Input (Double Isolation)