PCI Trigger Interface card (PCITi)

Overview

The PCI Trigger Interface (PCITI) is a general purpose PCI interface which will receive the trigger information form Trigger supervisor (TS), and distribute this to a PCI board front-end crate. It can communicate with the TS on a branch that allows up to eight Readout Controllers (ROC). The general function will be the same as VME Trigger interface which give the access to a VME read out controller card about the trigger information. The PCI Trigger Interface will also have an option to accept the trigger from its front panel. In this case it maintains system busy until data from the trigger is read out.

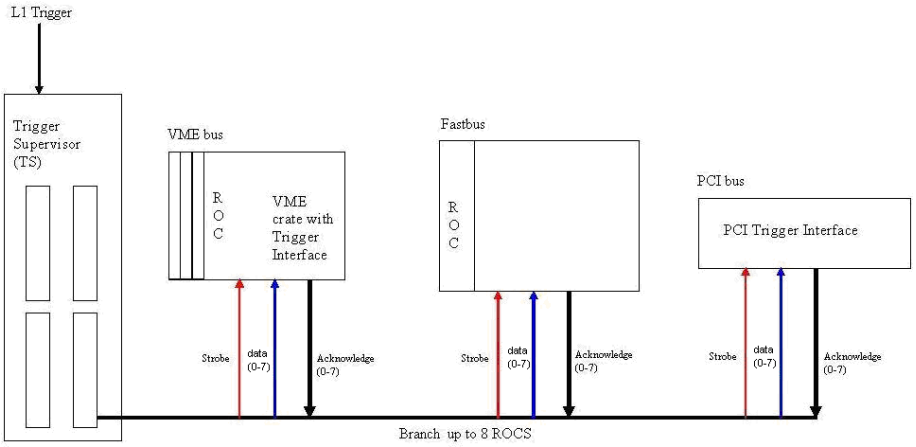

Figure 1 Data acquisition System

The PCI Trigger Interface may be placed in the middle or at the end of the TS Branch cable. The module has a socket where termination resistors can be installed in the case this is used at the far end of the branch cable. Onboard jumpers determine which ACK bit is used to send acknowledgements to the TS. The PCI Trigger board is shown in Figure 2, identifying the various ports on the module.

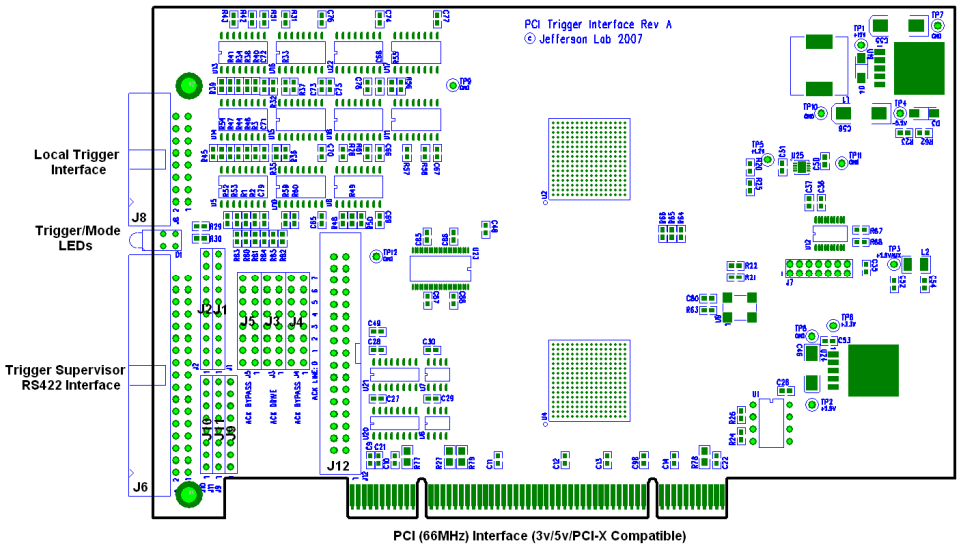

Figure 2: PCI Trigger Interface board

Hardware Description

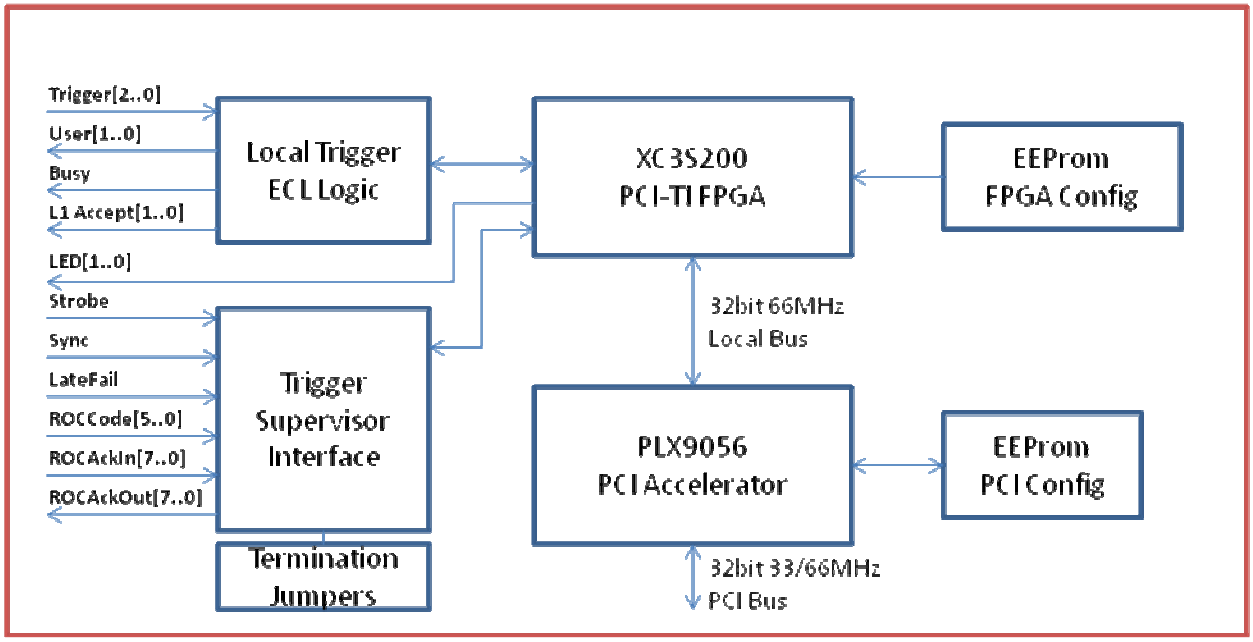

Figure 3: PCI Trigger Block Diagram

PCI Trigger Interface card features

- Enables PC based readout controller to have access to trigger information
- Input from Trigger Supervisor or external Trigger
- 66MHz 32bit PCI rev 3.0 interface (+3v/+5v signaling, PCI-X compatibility)
- LEDs (TS mode – off = TS Mode, On = Local Trigger Mode, Trigger - Pulsed)
- 2x user programmable outputs
- Expansion board supplies 34pin ROC interface on separate connector to extend 422 communication link (a front-panel PCI adapter can be made to make this more convenient).

PCI Target Interface

The PCI interface is a PLX 9056 from PLX Technology. It runs in a 32Bit, 66MHz PCI slave mode interface with a local bus that runs at 66MHz connected to FPGA. The PLX9056 bridges the PCI bus to the FPGA local bus. While the PLX9056 supports many options, currently the FPGA only supports 32bit burst/non-burst read and write transactions. Basic interrupts are supports to provide an interrupt on receipt of a trigger or TS strobe. The TS and local trigger interface signals are accessed through PCI PORT I/O registers.

Trigger Inputs

Trigger inputs are differential ECL signals with L1 assertion logic implemented in ECL to minimize L1Accept propagation delay and jitter. Trigger sources are maskable (via PCI bus registers).

Interface/Packaging PCI

Power Requirement (Max Dissipated Power <10W)

Voltage	Max Current	Derived From
+3.3v	500mA	PCI Bus
+5.0v	500mA	PCI Bus
+12v	400mA	PCI Bus
-5.2v	500mA	+12v
+2.5v	100mA	+3.3v
+1.2v	100mA	+3.3v

Interface & Signal Definitions

J6, J12 Pinouts

-All signals are differential RS-485

Signal name (Q)	Direction	Pin (Q, $\overline{Q}$)
Strobe	Input	1, 2
Sync	Input	3, 4
Late Fail	Input	5, 6
ROC Code Bit 0	Input	7, 8
ROC Code Bit 1	Input	9, 10
ROC Code Bit 2	Input	11, 12
ROC Code Bit 3	Input	13, 14
ROC Code Bit 4*	Input	15, 16
ROC Code Bit 5*	Input	17, 18
ROC 0 Acknowledge	Input/Output	19, 20
ROC 1 Acknowledge	Input/Output	21, 22
ROC 2 Acknowledge	Input/Output	23, 24
ROC 3 Acknowledge	Input/Output	25, 26
ROC 4 Acknowledge	Input/Output	27, 28
ROC 5 Acknowledge	Input/Output	29, 30
ROC 6 Acknowledge	Input/Output	31, 32
ROC 7 Acknowledge	Input/Output	33, 34

J8 Pinouts

-All signals are differential ECL

Signal name (Q)	Direction	Pin (Q, $\overline{Q}$)
Trigger 0	Input	1, 2
Trigger 1	Input	3, 4
Trigger 2	Intput	5, 6
User1	Output	7, 8
User2	Output	9, 10
Busy	Output	11, 12
L1 Accept (1)	Output	13, 14
L1 Accept (2)	Output	15, 16

Termination Jumpers

Position	Part#	Notes
J9, J10, J11	CTS Part# 77083101P	Install if last module on TS ROC branch.
J1, J2	CTS Part# 770101181P	Install if last module on TS ROC branch.

Registers

VER (Version Register)

Base Address: BAR2
Offset: 0x0000
Size: 32bits

Bits	Type	Desc
7:0	RO	Firmware Minor revision
15:8	RO	Firmware Major revision
31:16	x	unused

Version should be read as bits(15:8).bits(7:0)
For example: 0x0123 should be read as Version 1.35)

CSR (Control Status Register)

Base Address: BAR2
Offset: 0x0004
Size: 32bits
Reset State: 0x00000000

Bits	Type	Desc
0	RW	Trigger Mode (0-TS ROC, 1-EXT, LED Outputs a copy of this bit)
1	RW	Enable Triggers
2	RW	Enable Interrupts
3	RW	Test Mode
6:4	x	Reserved
7	WO	Reset Module
13:8	x	Reserved
14	RO	Interrupt Active (state of interrupt output, 1=interrupt)
15	RO	Trigger Latched (use in polling mode)
31:16	x	Reserved

TDR (Trigger Data Register)

Base Address: BAR2
Offset: 0x0008
Size: 32bits

Bits	Type	Desc
7:0	RO	Trigger Input Data
8	RO	Trigger Mode (identical to CSR b0)
9	x	Reserved
10	RO	User Output 0 Pin Status
11	RO	User Output 1 Pin Status
12	x	Reserved
13	WO	Software Trigger (Mode 1 only)
14	WO	Acknowledge Interrupt
15	WO	Acknowledge Trigger
31:16	x	Reserved

Note: Interrupt becomes active on a rising edge of a “Trigger Latched” condition. Interrupt will remain active after writing a ‘1’ to Acknowledging Trigger. A ‘1’ must be written to the Acknowledge Interrupt bit to clear interrupt.

ODR (Output Data Register)

Base Address: BAR2
Offset: 0x000C
Size: 32bits

Bits	Type	Desc
0	WO	Set Ouput 0
1	WO	Set Output 1
15:2	x	Reserved
16	WO	Clear Output 0
17	WO	Clear Output 1
31:18	x	Reserved

TSR (Trigger Scaler Register)

Base Address: BAR2
Offset: 0x0010
Size: 32bits
Reset State: 0x00000000

Bits	Type	Desc
31:0	RO	32bit Trigger Strobe Scaler
31	WO	Clear Trigger Scaler

OCR (Output Control Register)

Base Address: BAR2
Offset: 0x0014
Size: 32bits
Reset State: 0x00000000

Bits	Type	Desc
15:0	RW	Ouput 0 Pulse Width (in 16ns steps)
31:16	RW	Ouput 1 Pulse Width (in 16ns steps)

Note: For a width setting of 0, the outputs are under full control of Set/Clear bits in ODR.

LCR (Level 1 Control Register)

Base Address: BAR2
Offset: 0x0018
Size: 32bits
Reset State: 0x00000000

Bits	Type	Desc
15:0	RW	Level 1 Accept Ouput Pulse Width (in 16ns steps)
31:16	RW	Busy Pulse Extension (in 16ns steps)

Note: A setting of 0 for the Level 1 Accept will force output high permanently.
The Busy Pulse Extension is the length in 16ns steps that the BUSY output stays high beyond trigger acknowlege cycle (useful as a trigger holdoff).

Prototype Test Status:

Board#	1	2	3	4	5
FPGA					
FPGA EEProm					
PLX9056 PCI					
PLX9056 LBus					
PLX9056 EEProm					
LEDs					
Power Supplies					
User Ouputs					
TS ROC Branch					
Trigger Inputs					
Busy Output					
L1 Accept					

Status Legend:

Function Tested and Passed	
Function Tested and Failed	
Function Not Tested	