Jefferson Science Associates, LLC

Helicity Control Board User's Guide (Draft 3)

Programming and Hardware

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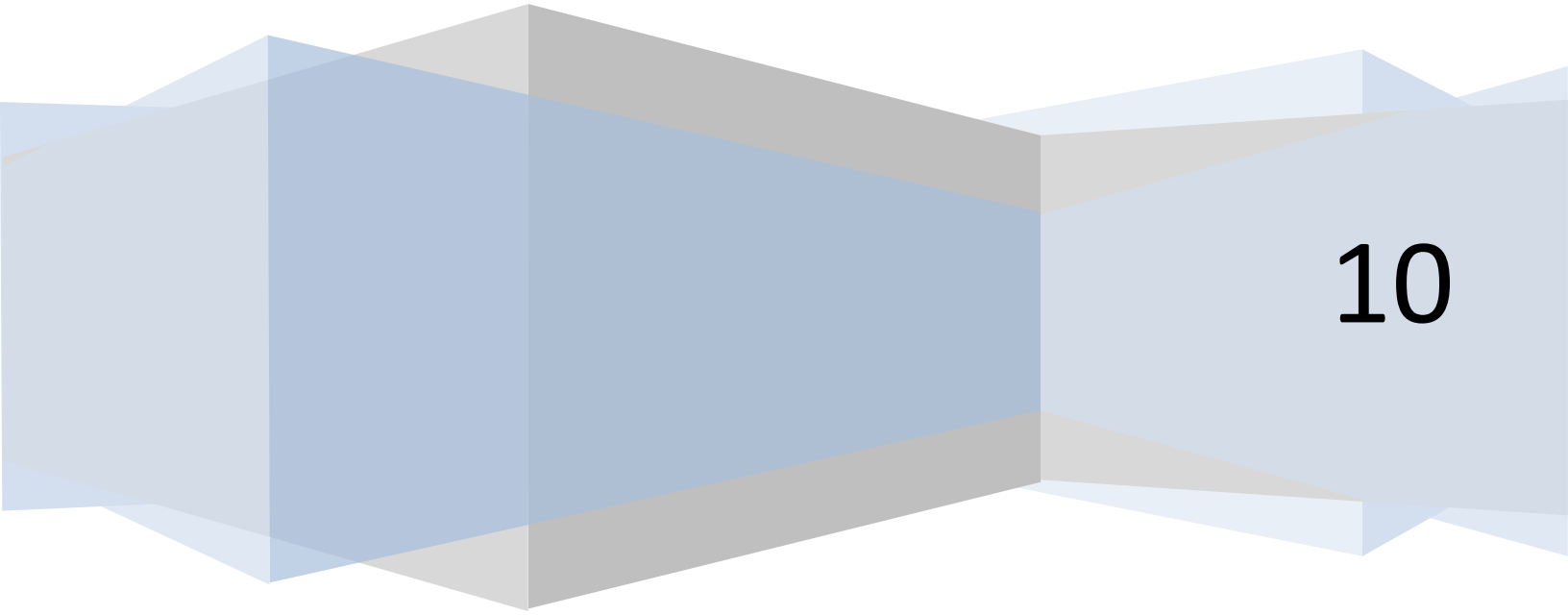

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Introduction

A new Helicity Control Board was installed in November 2009. The new board provides more outputs and easier to re-program than the old one. The initial programming was chosen to meet the requirements of the current experiments. Changes are very easy to make and there is no limitation on the outputs. However, there are two main issues to keep in mind when selecting the outputs: first, the Pockels Cell response to the high voltage (HV) switching and, second, the Data Acquisition systems (DAQ) of the Halls. In specific, the choice of the T_Settle has to be long enough to allow for the Pockels Cell to "settle" and the choice of the helicity reversal frequency has to be matched with the speed of the DAQ.

The Helicity Board is an "Advanced Programmable Logic Generator". One of its outputs (Helicity Flip signal) is used to control the high voltage (+3 kV or -3 kV) of the Pockels Cell on the Laser Table in CEBAF Injector. This change in Pockels Cell HV changes the circular polarization (left-handed or right-handed) of the laser light which in turn changes the direction of spin of the photo-emitted electrons relative to its momentum. The electron spin is either aligned parallel or anti parallel to the electron momentum; this is called electron helicity. Thus one signal from this logic generator changes the helicity of the electron beam and hence this board is called the Helicity Board.

The Helicity Board will operate at one of four timing selections. Three are fixed-frequencies of 30 Hz, 120 Hz, and 240 Hz triggered by "Beam Sync". The phase locking is forced during the last T_Stable period. The T_Settle time period may be chosen from the T_Settle Register values. The T_Stable selection is disabled in this mode.

The fourth mode of operation allows the board to operate in free-running mode, where T_Settle and T_Stable values are selected from the values in the registers.

The Reporting Delay is selected from a register and determines how many windows there are between the real time Helicity Flip signal and the Delayed Helicity signal.

The Helicity Pattern may be selected to provide three pseudo-random patterns: Pair, Quartet, and Octet. In these patterns, the first window is chosen using the pseudo-random bit Shift Register. The forth pattern is pair Toggle.

Note that when talking about frequency: it is the frequency of the T_Settle signal (f) and this will be labeled as the Helicity Board Frequency. Note that the Pair Sync signal will have $f/2$ frequency. The Pattern Sync signal will have $f/4$ when the Helicity Pattern is Quartet. The Delayed Helicity will have $f/2, f/4, f/8$... depending on the pattern.

In this document, there are three ways to indicate a helicity state: either 0, 1 $(+, -)$ or $\sqcap\!\!\sqcup$. Each helicity state is called a window.

Why a New Helicity Board?

It was time to upgrade the Helicity Board for the following reasons:

I. Clean up leftovers from G0. Drop the “MPS” label.

II. Make it easy to program and easy to choose any reversal rate and any T_Settle time.

III. Change the Shift Register to 30-Bit. The old one is 24-Bit and would repeat in a shorter time (1 day compared to 50 days in the case when the Helicity Board frequency is 1 kHz).

IV. Add a new pattern: Octet (+ − − + − + + − or − + + − + − − +).

V. Add new fiber output signals:

1. 2 additional outputs for 4-way Intensity Attenuator (IA) feedback scheme where the applied IA voltage is determined not only from the current helicity state but also from the current and previous helicity patterns.
2. Output of the Helicity Board 20 MHz Clock signal.

Helicity Board Modes

There are two modes of the Helicity Board:

Beam Sync Mode

There are three line synced fixed-frequencies of 30 Hz, 120 Hz, and 240 Hz triggered by "Beam Sync". The phase locking is forced during the last T_Stable period. The T_Settle time period may be chosen from the T_Settle Register. You cannot choose T_Stable in this mode only T_Settle. Once you select Beam Sync Mode, the T_Stable menu bar is disabled.

Free Clock Mode

This mode of operation allows the board to operate in free-running mode, where the T_Settle and T_Stable values are selected from the tables below. In this mode, you can select any T_Settle and any T_Stable.

Helicity Board Registers

These registers have the listed values. We can choose whatever we want to fill them.

T_Settle Register

There is a Five-bit R/W register that determines the "T_Settle" portion of the helicity period. The settle time selections are as follows:

> 10 µs, 20 µs, 30 µs, 40 µs, 50 µs, 60 µs, 70 µs, 80 µs, 90 µs, 100 µs, 110 µs, 120 µs, 130 µs, 140 µs, 150 µs, 160 µs, 170 µs, 180 µs, 190 µs, 200 µs, 250 µs, 300 µs, 350 µs, 400 µs, 450 µs, 500 µs (DEFAULT), 550 µs, 600 µs, 700 µs, 800 µs, 900 µs, 1000 µs.

T_Stable Register

There is a Five-bit R/W register that determines the "T_Stable" portion of the helicity period. The stable time selections are as follows:

> 400 µs, 500 µs, 600 µs, 700 µs, 800 µs, 900 µs, 1000 µs, 1500 µs, 2000 µs, 2500 µs, 3000 µs, 3500 µs, 4067 µs, 4500 µs, 5000 µs, 5500 µs, 6000 µs, 6500 µs, 7000 µs, 7500 µs, 8230 µs, 8500 µs, 9000 µs, 33230 µs, 33330 µs (DEFAULT), 50000 µs, 75000 µs, 100000 µs, 250000 µs, 500000 µs, 750000 µs, 1000000 µs.

Helicity Pattern Register

There is a Two-bit R/W register that determines the Helicity Pattern. The pattern selections are as follow:

> Pair (+ − or − +), Quartet (− + + − or + − − +) (DEFAULT),
>
> Octet (+ − − + − + + − or − + + − + − − +), and Toggle (+ − + − + − + − + − ⋯).

Reporting Delay Register

There is a three-bit R/W register that determines the delay of the Delayed Helicity signal relative to the real time Helicity Flip signal. The delay time in units of helicity windows is selected as follows:

No Delay, 1 window, 2 windows, 4, 8 (DEFAULT), 12, 16, 24, 32, 40, 48, 64, 72, 96, 112, and 128 windows.

For example a Quartet has 4 helicity windows.

Software

EPICS Channels

These are the old channels:

Table 1: A list of the EPICS Channels used with the old Helicity Board.

Channel	Name	Value
G0 Helicity Settle Set	HELG0TSETTLEs	500 µs
G0 Helicity Delay Set	HELG0DELAYs	8 windows
G0 Helicity Pattern Set	HELG0PATTERNs	Quartet
G0 Helicity Random/Toggle Set	HELG0ORDERs	Random
G0 Helicity Settle Read	HELG0TSETTLEd	500 µs
G0 Helicity Delay Read	HELG0DELAYd	8 windows
G0 Helicity Pattern Read	HELG0PATTERNd	Quartet
G0 Helicity Random/Toggle Read	HELG0ORDERd	Random

These are the new channels:

Table 2: A list of the EPICS Channels used with the new Helicity Board. These are the settings used during the PVDIS experiment.

Channel	Name	Default Value
Helicity Clock Set	HELCLOCKs	Free Clock
Helicity Reporting Delay Set	HELDELAYs	8 windows
Helicity Pattern Set	HELPATTERNs	Quartet
Helicity Clock Read	HELCLOCKd	Free Clock
Helicity T_Settle Read	HELTSETTLEd	500 µs
Helicity T_Stable Read	HELTSTABLEd	33330 µs
Helicity Reporting Delay Read	HELDELAYd	8 windows
Helicity Pattern Read	HELPATTERNd	Quartet
Helicity Board Frequency	HELFREQ	(calculated frequency, not a readback) 29.5596 Hz

Below is the relation between the Numeric Value and Text for the Mode (**HELCLOCKd**). Type "caget -n" to get the numeric value instead of the string:

0 = 30 Hz Line Sync

1 = 120 Hz Line Sync

2 = 240 Hz Line Sync

3 = Free Clock

Below is the relation between the Numeric Value and Text for the Helicity Pattern (**HELPATTERNd**). Type "caget -n" to get the numeric value instead of the string:

0 = Pair 1 = Quartet 2 = Octet 3 = Toggle

Below is the relation between Numeric Value and Text for the Reporting Delay (**HELDELAYd**). Type "caget -n" to get the numeric value instead of the string:

0 = No delay	1 = 1 window	2 = 2 windows	3 = 4 windows
4 = 8 windows	5 = 12 windows	6 = 16 windows	7 = 24 windows
8 = 32 windows	9 = 40 windows	10 = 48 windows	11 = 64 windows
12 = 72 windows	13 = 96 windows	14 = 112 windows	15 = 128 windows

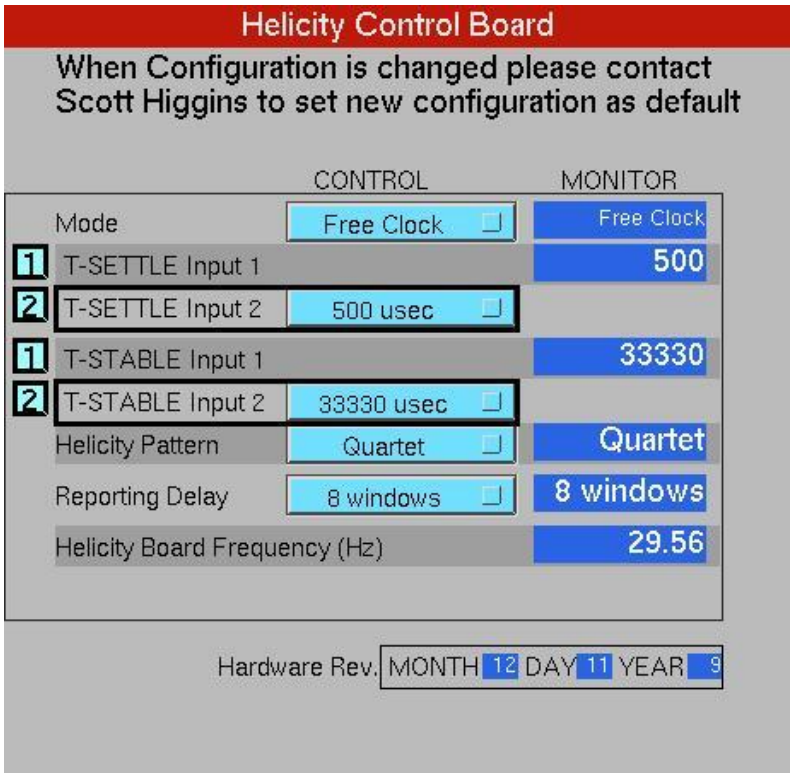

Figure 1: Helicity Board Control Screen. There are two pull-down menus for T_Settle and two menus for T_Stable. In Free Clock Mode, all menus are available. In Line Synced Mode, only the menus of T_Settle are active; T_Stable menus are inactive.

Programming

Figure 1 shows the control screen for the new Helicity Board. The following shows how to use the board.

1. Select Mode:

    I. Beam Sync (Force phase-locking during last T_Stable):

    - Select Helicity Board Frequency f: 30 , 120, or 240 Hz Line Sync
    - Select T_Settle value between 10 µs – 1,000 µs
    - Display T_Stable (T_Stable selection is disabled):

$$T_{\_Stable} = \frac{1}{f} - T_{\_Settle}$$

The Beam Sync jitter will show up in the last window of the pattern. For example with "240 Hz Line Sync" and Octet Pattern, the first 7 windows will have a length of 4,167 µs and the 8th window will be

4167 µs ± Beam sync jitter. The length of this last window can be used to monitor the jitter in the 60 Hz line frequency.

II. Free Clock:

- Select T_Settle value between 10 µs – 1,000 µs
- Select T_Stable value between 400 µs – 1,000,000 µs
- Display Helicity Board Frequency (Reversal Rate):

$$f = \frac{1}{T_{\_Settle} + T_{\_Stable}}$$

2. Select Helicity Pattern:

   Pair ($+-$ or $-+$), Quartet ($-++-$ or $+--+$),

   Octet ($+--+-++-$ or $-++-+--+$), or Toggle ($+-+-+-+-\cdots$)

3. Select Reporting Delay: n Windows, n = 0 … 128 windows

Pseudo-random Helicity Generator

A 30-Bit Shift Register is used to generate the pseudo-random bits: 0, 1 (or $+, -$) which determines the first window of a pattern. This removes any correlation between the helicity of the beam and any other device in the accelerator or in the Hall. It is a pseudo-random bit, not "random", because it is deterministic, once a sequence of 30 bits is known, the next bits can be predicted, and it repeats after the maximal length. For any initial register value, there are $2^{30} - 1$ = 1,073,741,823 (maximal length) random bits before the sequence repeats, 50 days for 1000 Hz helicity reversal rate and a Quartet Pattern. Figure 2 shows the 30-Bit shift register.

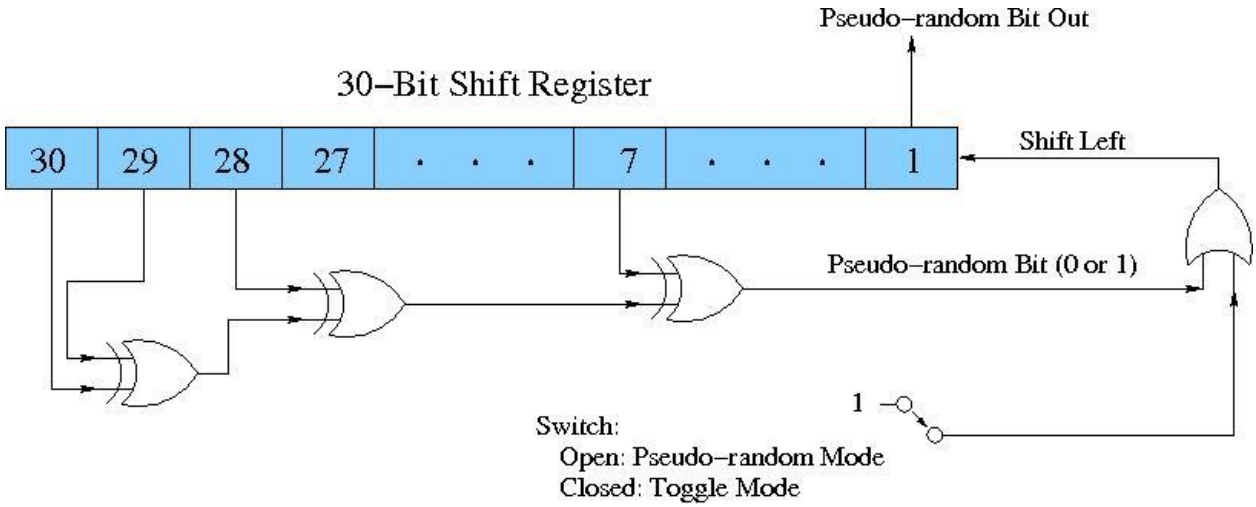

Figure 2: The 30 Bit Shift Register used to generate the pseudo-random bit. This bit is an XOR of bits 30, 29, 28, and 7.

The following C++ code can be used to initially fill the Shift Register and to predict the helicity bit:

```
UInt_t RanBit(UInt_t hRead)
{
        UInt_t bit7   = (fgShreg & 0x00000040) != 0;
        UInt_t bit28  = (fgShreg & 0x08000000) != 0;
        UInt_t bit29  = (fgShreg & 0x10000000) != 0;
        UInt_t bit30  = (fgShreg & 0x20000000) != 0;
        UInt_t newbit = (bit30 ^ bit29 ^ bit28 ^ bit7) & 0x1;
        fgShreg = ( (hRead == 2 ? newbit : hRead) | (fgShreg << 1 )) & 0x3FFFFFFF;
        return newbit;
}
```

During analysis of the parity data, the first 30 patterns of each typically 1 hour long data runs are used to initialize the Shift Register (these data patterns are thrown away). After the initialization, the analysis code can predict what the next pseudo-random bit will be. This prediction is compared to the actual helicity of the first window of each pattern in the data to make sure things are fine. Polarimeters and non-parity experiments usually do not perform this check.

Hardware Description

The Helicity Control Board is located in an isolated crate in the Injector Service Building, see Figure 3. This crate is powered by an Isolation Transformer and is floating at 65 VAC. Follow instruction posted on the rack when working there.

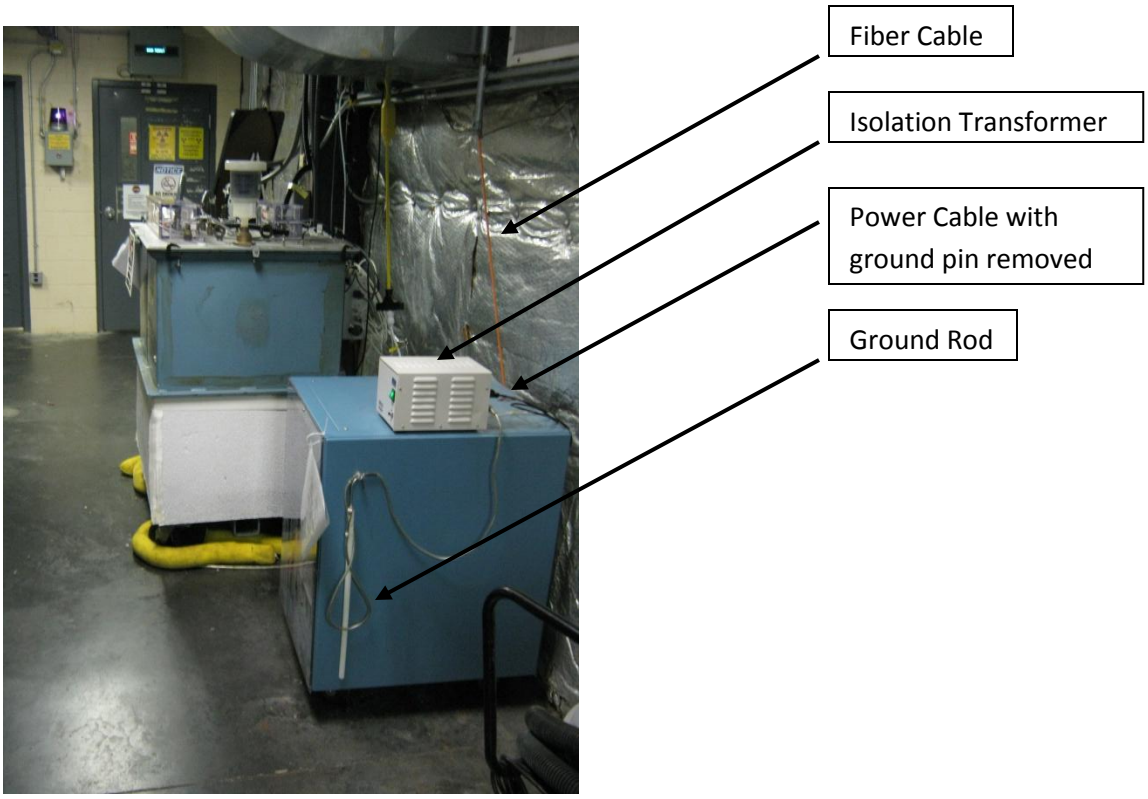

Figure 3: Rack that houses the Helicity Control Board. The crate inside is powered by an Isolation Transformer and is floating at 65 VAC. Please follow safety procedure when working in this rack. The ground pin of power cable from the Isolation Transformer is removed.

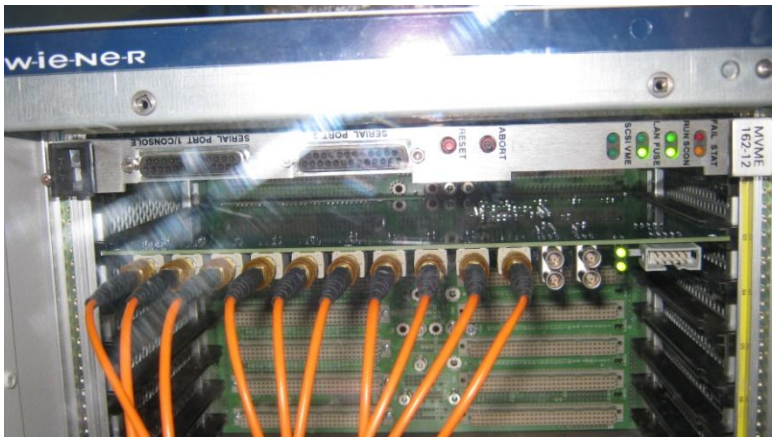

Figure 4: Helicity Control Board and its crate. The name of the crate is "iochelgen". There are 12 fibers connected to this crate. The first 10 fibers carry signals to (Beam Sync) and from (9 signals) the Helicity Board. Fiber 11 is iochelgen TX and Fiber 12 is iochelgen RX.

Helicity Board Inputs and Outputs

Figure 4 shows the new Helicity Control Board. The following describes the new board front panel.

LED Signals

1. HEL REQ BIT/8 (Left): (?)
2. HEL REQ BIT (Right): (?)

LEMO Signals

Upper left to lower right:

1. NC (Input): (?)
2. Hel REQ Bit (Output): (?)
3. Pattern Sync (Output): TTL signal
4. T_Settle (Output): TTL signal

Fiber-Optic Inputs

1. Beam Sync: This is the standard accelerator 60 Hz Beam Sync signal. It is generated from the Virginia Power line signal inside the 60 Hz Line Synchronization chassis in rack IN03B21. It is commonly used in the accelerator to …. The 60 Hz power line frequency is known to be relatively stable to about 60.00±0.05 Hz. This gives an average period of 16,666±15 µs.

Fiber-Optic Outputs

1. Patter Sync (old name QRT): Indicates the start of each pattern. If the pattern is Pair, then it is identical to Pair Sync, see Figure 7. This signal goes to the users.
2. T_Settle (old name MPS): Indicates the time the DAQs will not collect data allowing for the Pockels Cell to settle. This signal goes to the users and the Helicity Magnets crate. This signal can also be called T_Stable since when it is not true the Pockels Cell is stable.
3. Helicity Flip: This is the signal that goes to the Pockels Cell and IAs. The Pockels Cell changes its voltage with this signal thus changes the circular polarization of the laser light, see Figure 27. Its

length is T_Settle + T_Stable. This is the real time helicity and goes only to the Laser Hut in CEBAF Injector. The IAs used to implement helicity-correlated charge feedback receive this signal, too. For one helicity, 0 voltage is applied to the IA and for the other helicity a voltage of up to ±60 V is applied.

4. nHelicity Flip: Complementary to the Helicity Flip signal. This way the board always draws the same current regardless of the helicity being 0 or 1 and further protects against any electrical pickup from the Helicity Board. This real time helicity signal goes to the crate that controls the Helicity Magnets. This is a floating crate located in the 5 MeV region in CEBAF Injector and powered by an isolation transformer with its power cable ground pin removed, see Figure 5.

5. Delayed Helicity: This signal is delayed by n windows, where n is chosen from Reporting Delay Register. It tells what the helicity was n windows before. This way no devices on the beamline or in the Halls know what the real time helicity is. In analysis, the data are shifted to match it with its helicity. This signal goes to the users, iocse9 and iocse14 in BSY.

   Note that the last n windows of data in each DAQ run are thrown away because the DAQ does not receive the actual helicity of these data (although it is known from helicity prediction).

6. Pair Sync: This signal toggle between 0 and 1, otherwise it looks like the helicity signal. Some DAQs used this signal to construct T_Stable (the integration window). It goes to the users.

7. IA0: This is an IA Control signal that indicates the current pattern. It goes to the Laser Hut in CEBAF Injector.

8. IA1: This is an IA Control signal that indicates the previous pattern. It goes to the Laser Hut in CEBAF Injector.

9. 20 MHz Clock: This is the internal Helicity Control Board clock. It goes to the Qweak ADCs in Injector and Hall C as external clock. It will be used as the reference clock for the ADCs. It will ensure that all the crates are sampling the same times.

The Halls only receive the following signals: T_Settle, Pair Sync, Pattern Sync, and Delayed Helicity. Hall C also receives the 20 MHz Clock signal. Only the Parity DAQs make use of the four signals and data are analyzed according to the pattern generated by the Helicity Board. Other DAQs use some of them. For example:

I. Accelerator FFB Measurement of Charge Asymmetry and Position Differences: This measurement uses the BPMs in Hall A Arc (iocse9) and the BPMs in Hall C Arc (iocse14). The only signal these iocs receive is the Delayed Helicity. The analysis software is hard-coded to drop the first part of each helicity window that corresponds to T_Settle (assumes T_Settle is 500 μs). Also a Reporting Delay of 8 windows is hard-coded. The data are analyzed in pairs.
II. 100 keV/500 keV and 5 MeV Injector Mott Polarimeter DAQ: Uses only T_Settle and Delayed Helicity with Reporting Delay set to No Delay and the data are analyzed in pairs regardless of the Helicity Pattern.

III. Hall A Spectrometer DAQ, Parity DAQ, Moller Polarimeter DAQ, and Compton Polarimeter DAQ: All use the four signals and analyze the data according to the pattern generated by the Helicity Board.

IV. (?) Hall B CLAS DAQ and Moller Polarimeter DAQ: Only uses Delayed Helicity and T_Settle. Data are analyzed in pairs.

V. Hall C QWeak Parity DAQ and Moller Polarimeter DAQ: Hall C does not receive Pair Sync signal. Data are analyzed according to the pattern generated by the Helicity Board.

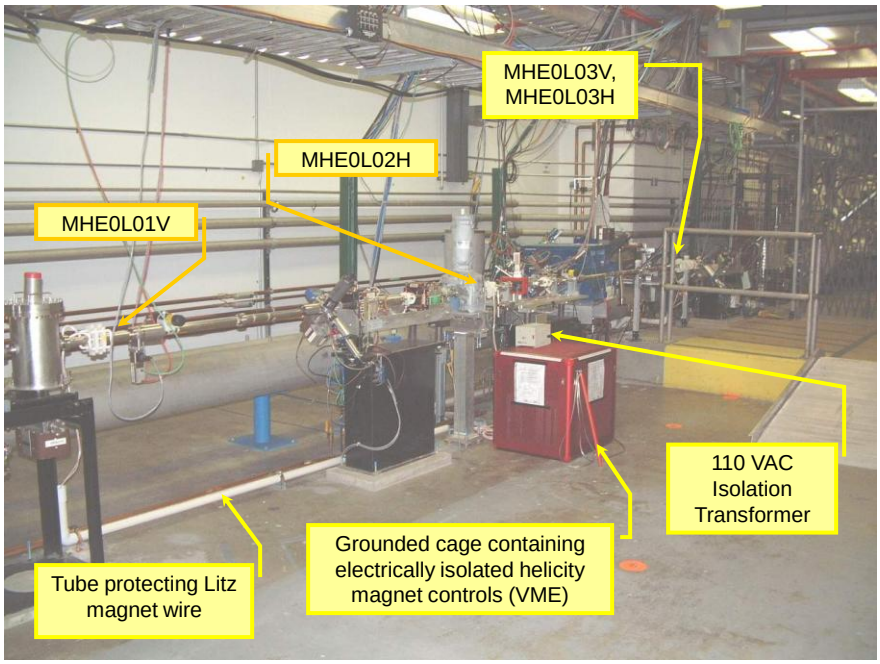

Figure 5: Rack that houses the Helicity Magnets Controller. The crate inside is powered by an Isolation Transformer with the ground pin of the power cable from the Isolation Transformer is removed. This crate receives two signals: nHelicity Flip and T_Settle.

Figure 6 - Figure 24 show the outputs of the helicity board using a scope.

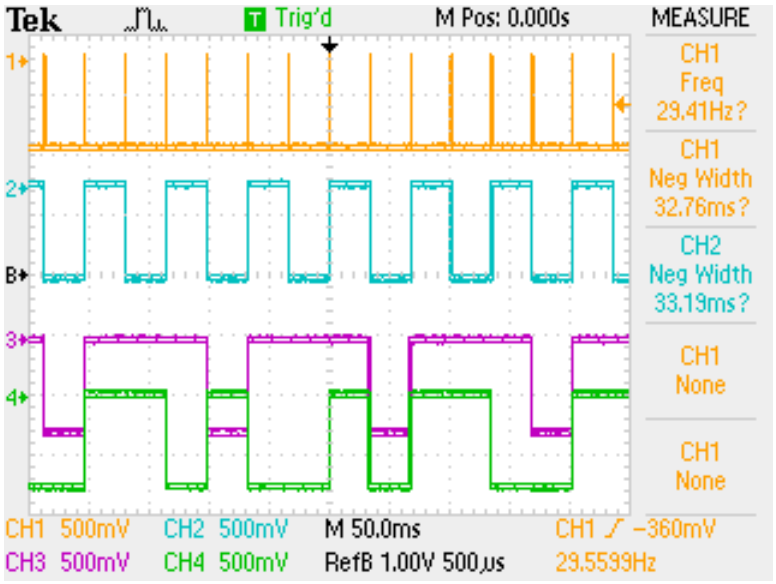

Figure 6: CH1: T_Settle, CH2: Pair Sync, CH3: Pattern Sync, CH4: Delayed Helicity. This was the configuration for Hall A PVDIS experiment.

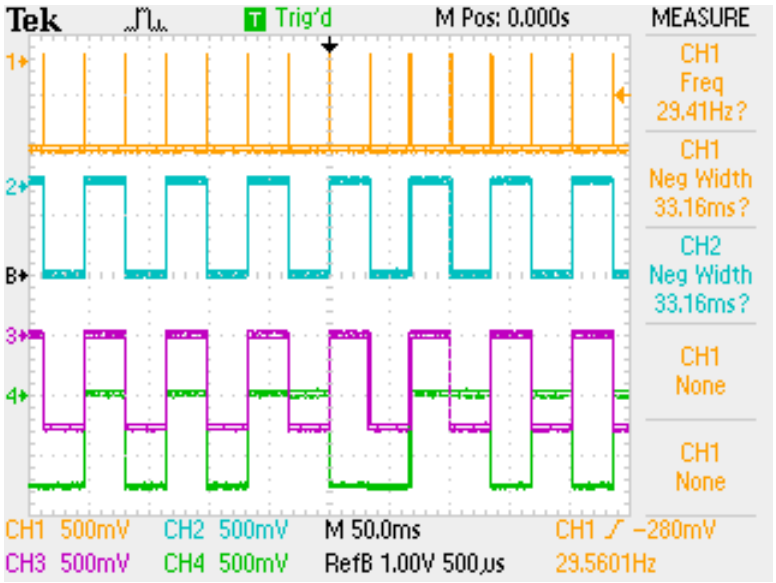

Figure 7: CH1: T_Settle, CH2: Pair Sync, CH3: Pattern Sync, CH4: Delayed Helicity. The Helicity Board settings are: Pair Pattern.

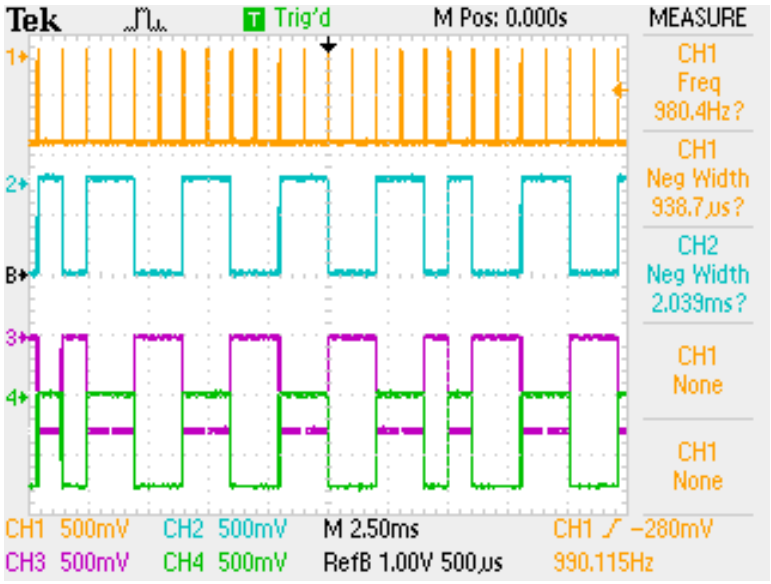

Figure 8: CH1: T_Settle, CH2: Helicity Flip, CH3: nHelicity Flip, CH4: Delayed Helicity. The Helicity Board settings are: No Delay.

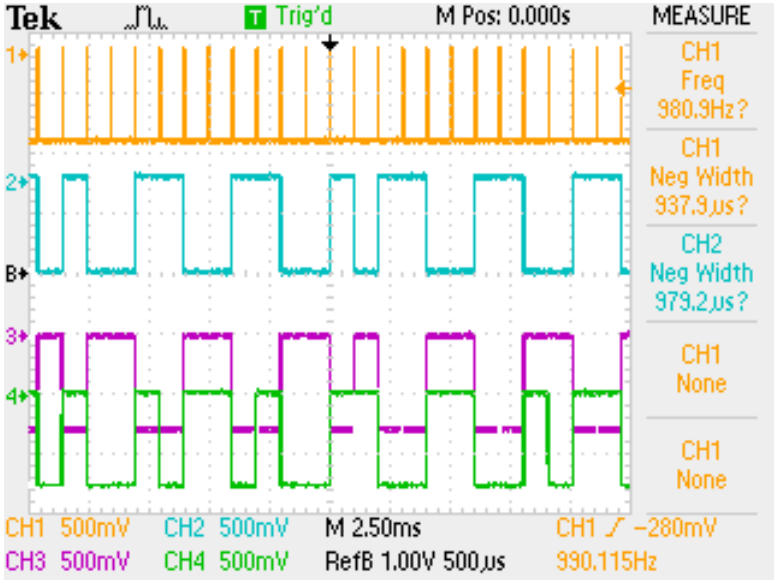

Figure 9: CH1: T_Settle, CH2: Helicity Flip, CH3: nHelicity Flip, CH4: Delayed Helicity. The Helicity Board settings are: Reporting Delay is 8 windows.

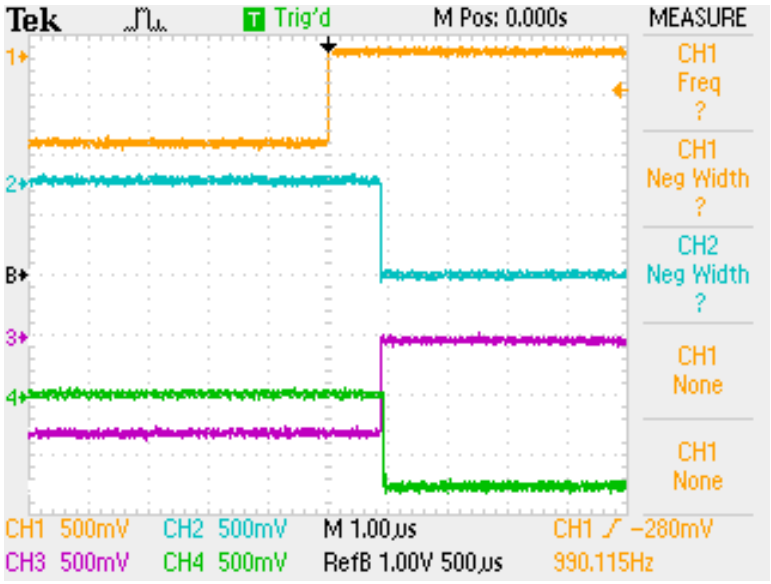

Figure 10: CH1: T_Settle, CH2: Helicity Flip, CH3: nHelicity Flip, CH4: Delayed Helicity. The delay is 8 windows.

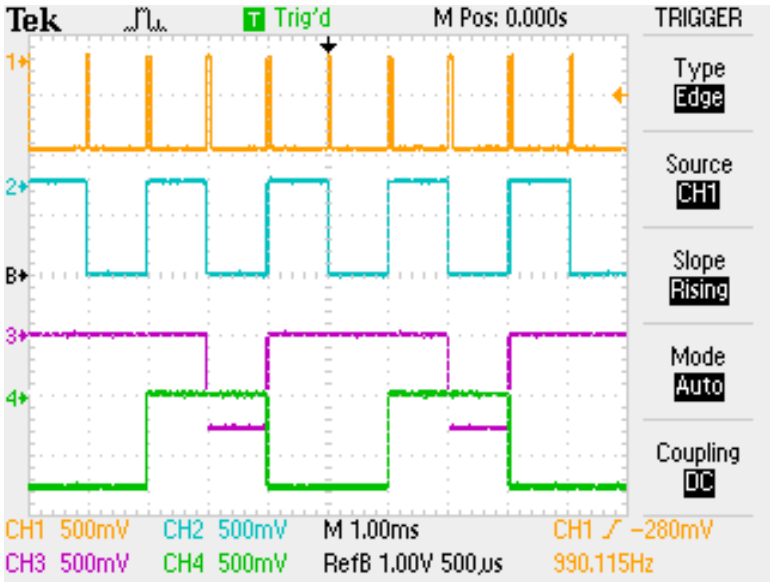

Figure 11: CH1: T_Settle, CH2: Pair Sync, CH3: Pattern Sync, CH4: Delayed Helicity. The Helicity Board settings are: T_Settle = 60 µs, T_Stable = 900 µs.

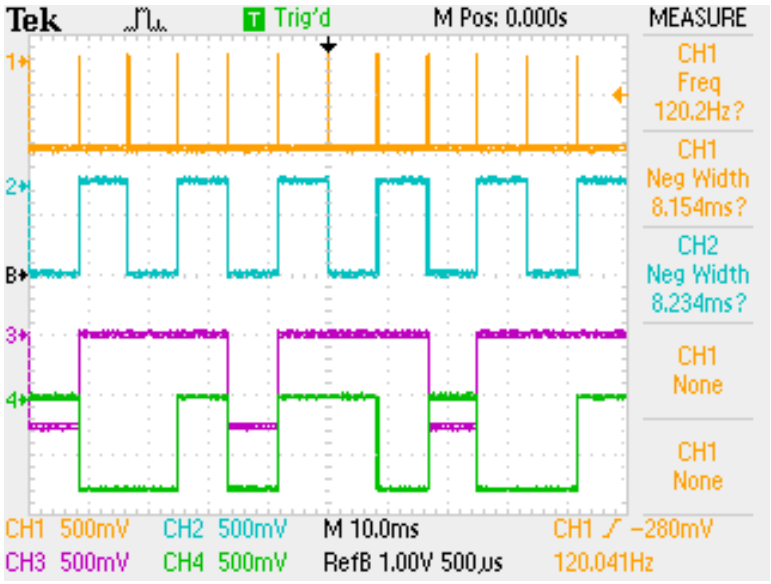

Figure 12: CH1: T_Settle, CH2: Pair Sync, CH3: Pattern Sync, CH4: Delayed Helicity. The Helicity Board settings are: 120 Hz Line Sync Mode and Quartet Pattern. The helicity widow was measured to be T_Settle + T_Stable = 8.300 ms.

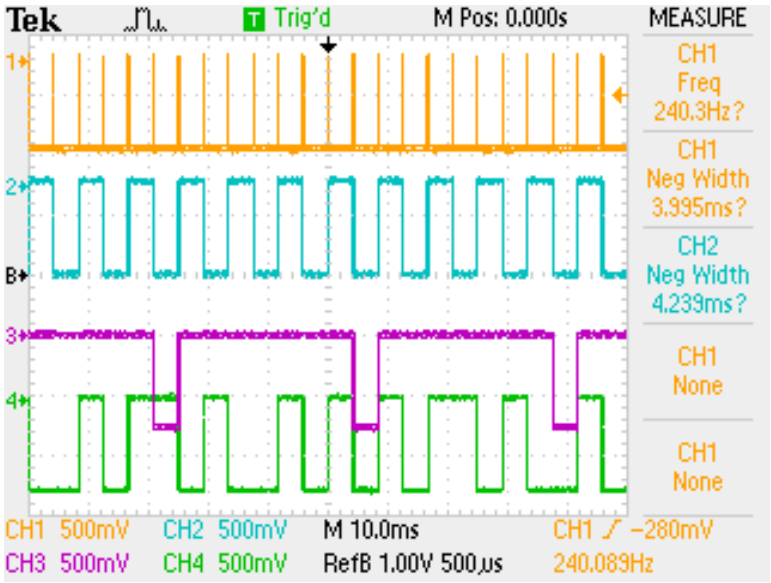

Figure 13: CH1: T_Settle, CH2: Pair Sync, CH3: Pattern Sync, CH4: Delayed Helicity. The Helicity Board settings are: 240 Hz Line Sync Mode and Octet Pattern. The helicity widow was measured to be T_Settle + T_Stable = 4.150 ms.

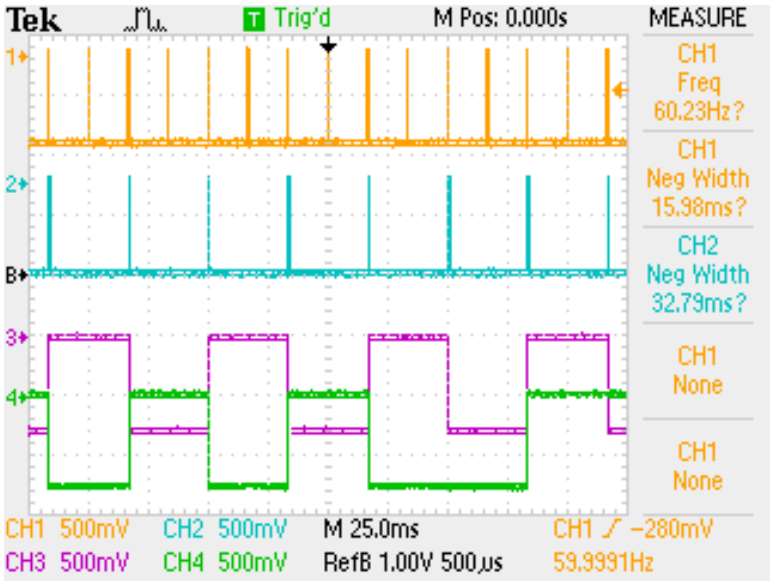

Figure 14: CH1: Beam Sync, CH2: T_Settle, CH3: Pattern Sync, CH4: Delayed Helicity. The Helicity Board settings are: 30 Hz Line Sync Mode and Pair Pattern.

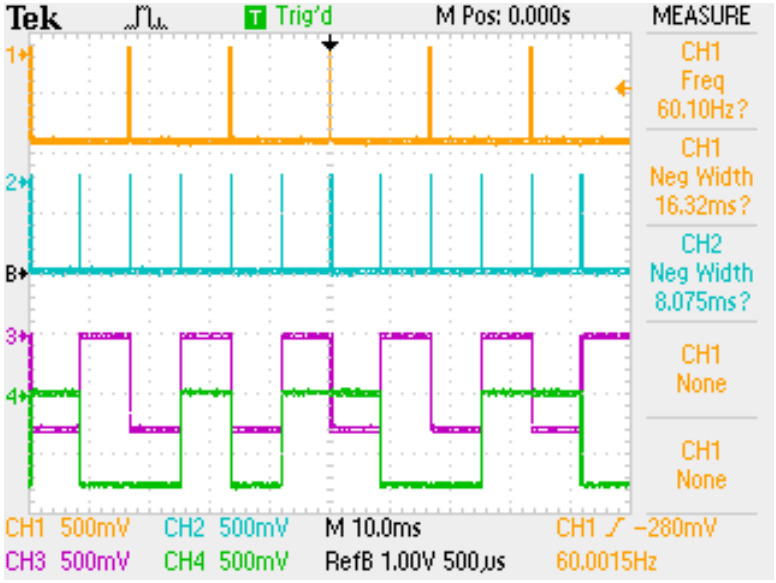

Figure 15: CH1: Beam Sync, CH2: T_Settle, CH3: Pattern Sync, CH4: Delayed Helicity. The Helicity Board settings are: 120 Hz Line Sync Mode and Quartet Pattern.

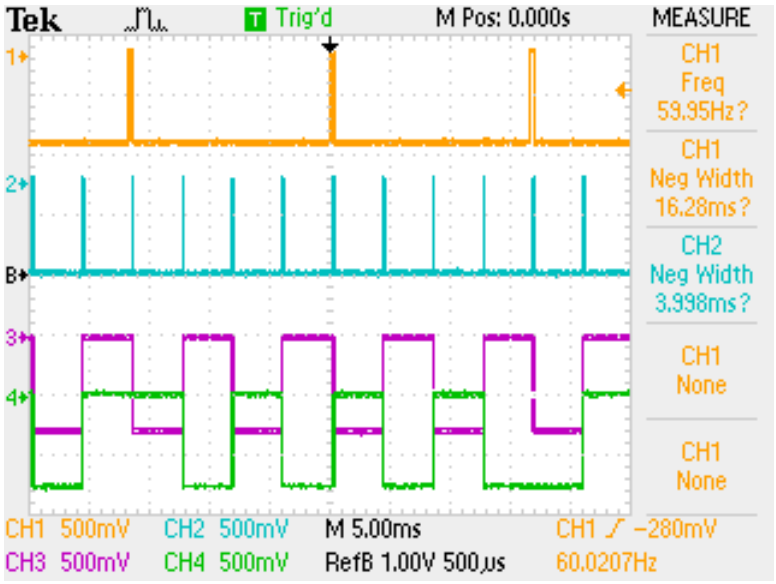

Figure 16: CH1: Beam Sync, CH2: T_Settle, CH3: Pattern Sync, CH4: Delayed Helicity. The Helicity Board settings are: 240 Hz Line Sync Mode and Octet Pattern.

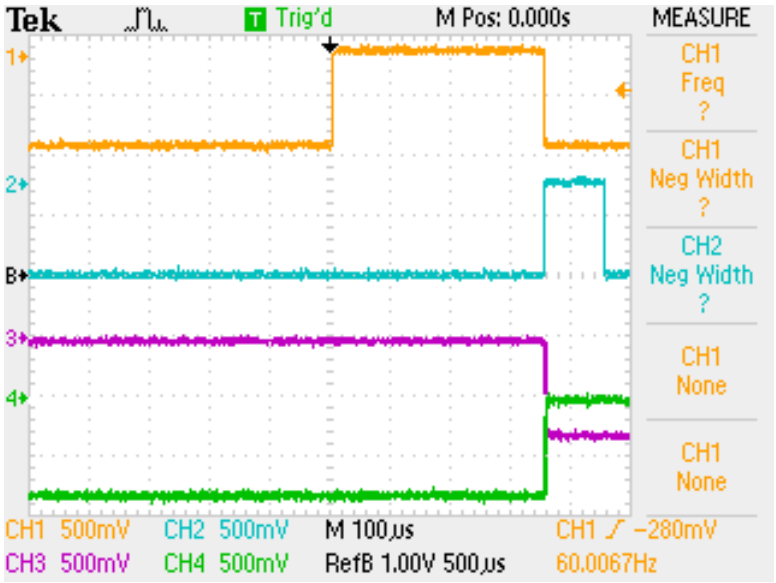

Figure 17: CH1: Beam Sync, CH2: T_Settle, CH3: Pattern Sync, CH4: Delayed Helicity. The Helicity Board settings are: 240 Hz Line Sync Mode and Octet Pattern.

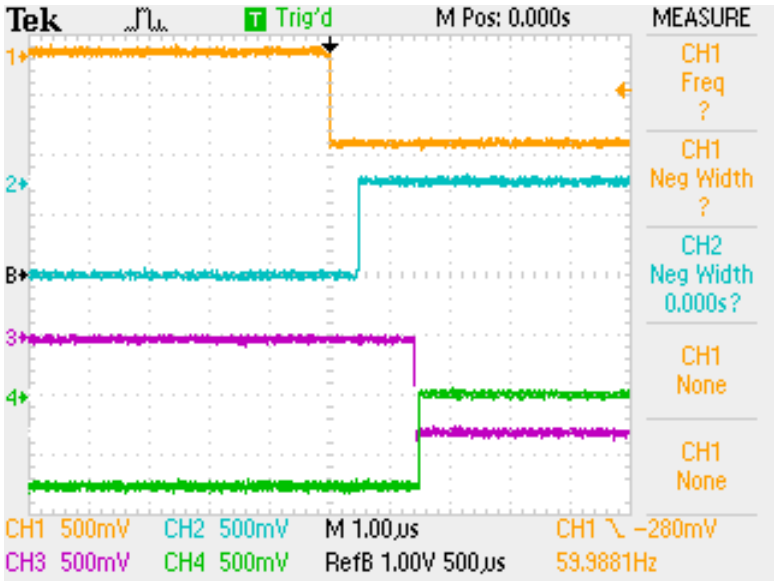

Figure 18: CH1: Beam Sync, CH2: T_Settle, CH3: Pattern Sync, CH4: Delayed Helicity. The Helicity Board settings are: 240 Hz Line Sync Mode and Octet Pattern.

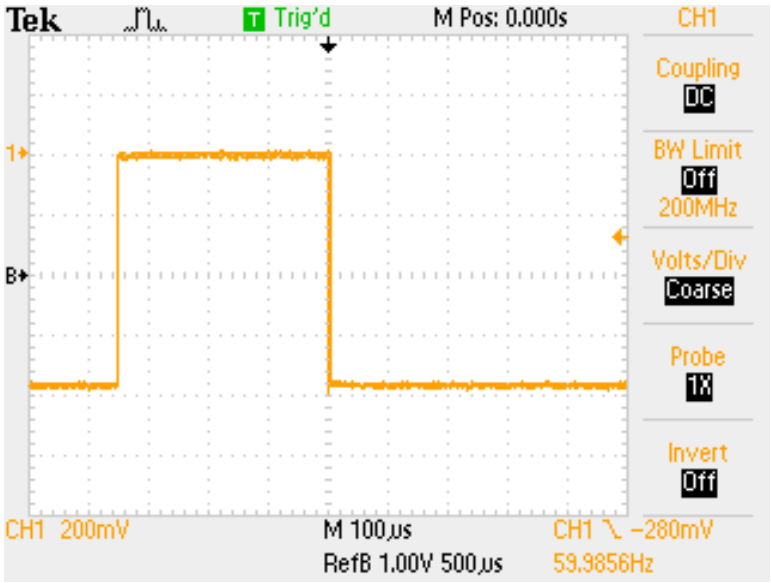

Figure 19: CH1: Beam Sync.

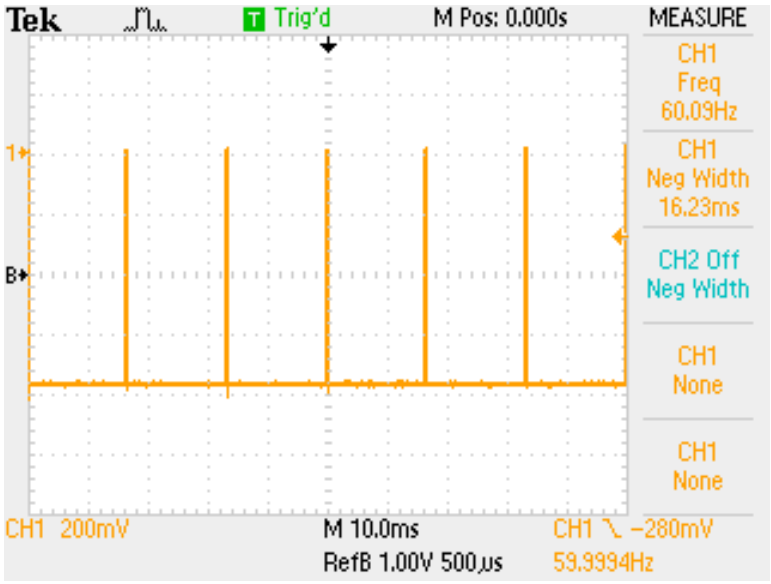

Figure 20: CH1: Beam Sync.

Figure 21: CH1: 20 MHz Clock.

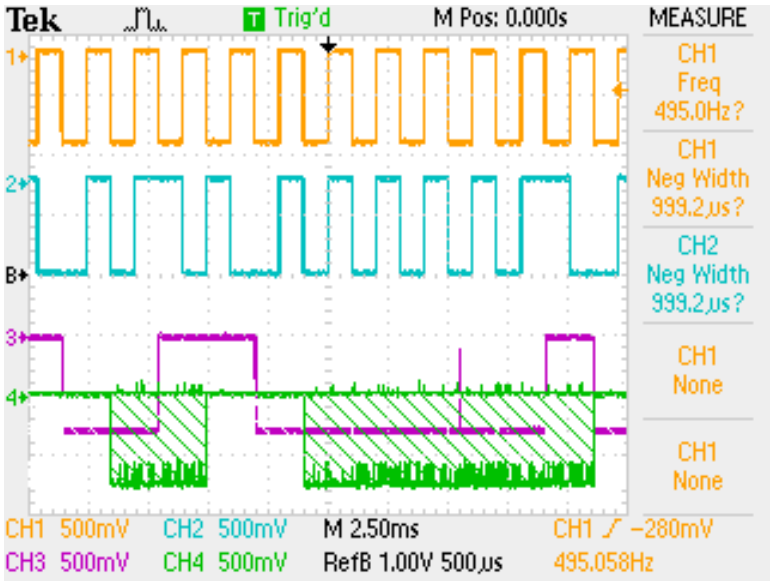

Figure 22: CH1: Pattern Sync, CH2: Helicity Flip, CH3: IA0, CH4: IA1. The Helicity Board settings are: Pair Pattern.

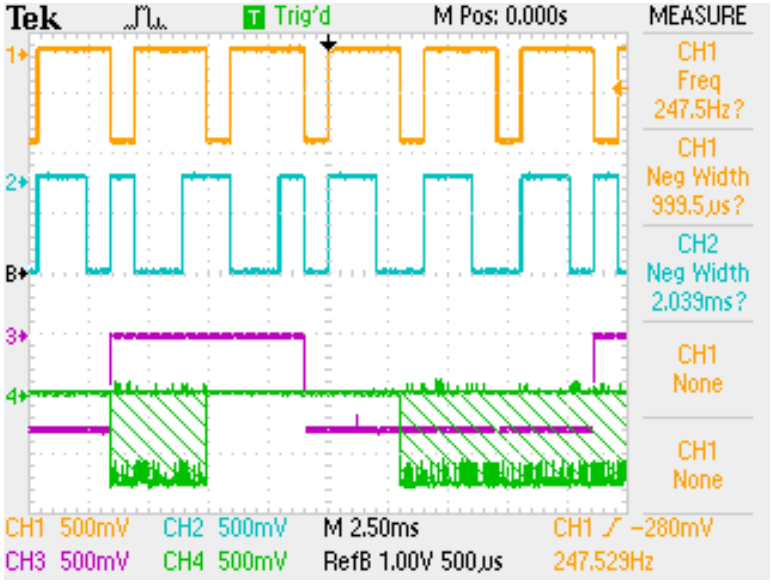

Figure 23: CH1: Pattern Sync, CH2: Helicity Flip, CH3: IA0, CH4: IA1. The Helicity Board settings are: Quartet Pattern.

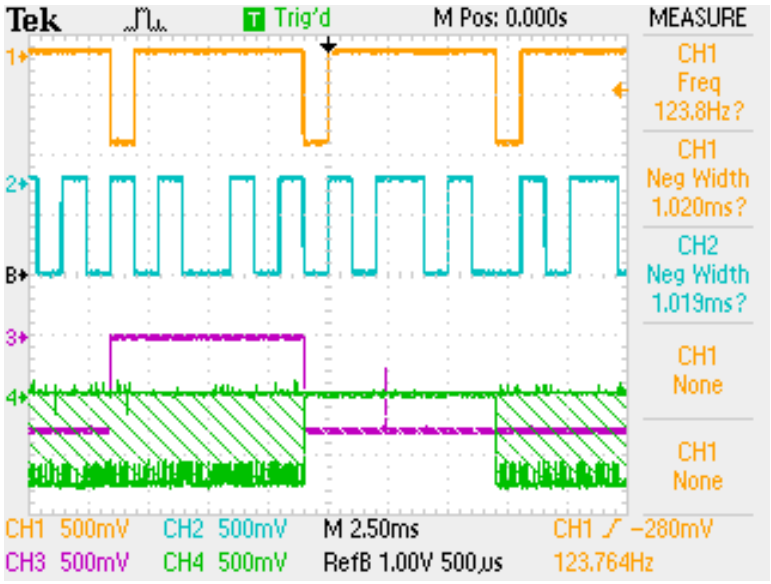

Figure 24: CH1: Pattern Sync, CH2: Helicity Flip, CH3: IA0, CH4: IA1. The Helicity Board settings are: Octet Pattern.

Relative Timing of Helicity Board Outputs

With the old helicity board, all the signals were in time. Looking at these signals in the injector or hall would show roughly 100 ns delays between them. This is mainly due to the Fiber FAN IN/OUT and to the Fiber Transducer and NIM FAN IN/OUT internal delays. For the new board, the transition to T_Settle starts 1.0 µs before all other signals, see Figure 25 and Figure 26. This is long enough to make sure the Halls know that the helicity is going to change beforehand. Actually this is not absolutely required because it takes the beam about 4.3 µs per pass to reach the Hall.

If T_Settle is of order of 10s µs, then we should account for the time the beam reaches the hall and for the time it takes for the helicity board signals to propagate to the Laser Table and to the Halls.

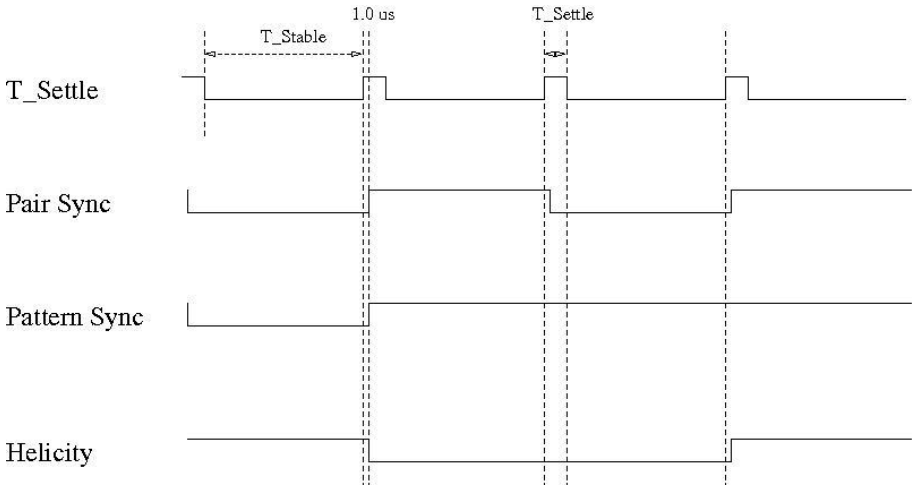

Figure 25: Helicity Board output signals timing relative to T_Settle. All the signals: Pair Sync, Pattern Sync, Helicity Flip, nHelicity Flip, Delayed Helicity, IA0, and IA1 start 1.0 µs after T_Settle.

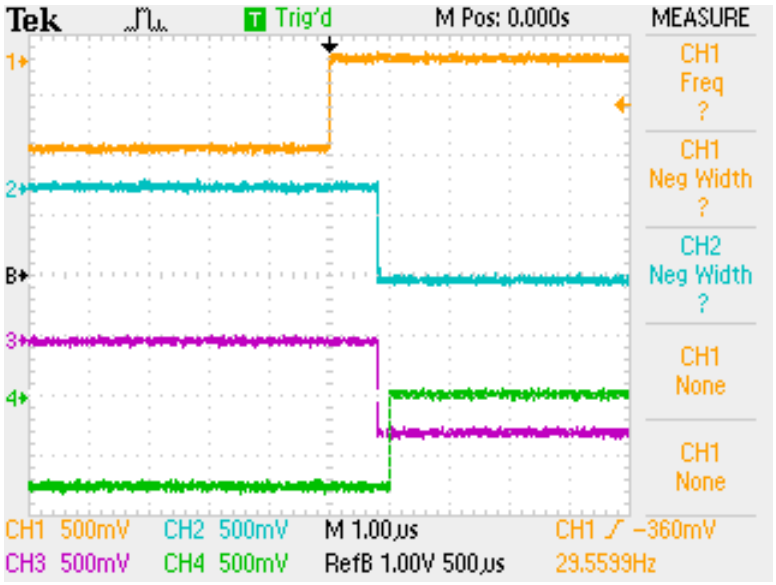

Figure 26: CH1: T_Settle, CH2: Pair Sync, CH3: Pattern Sync, CH4: Delayed Helicity. T_Settle starts 1.0 µs earlier than all other signals.

Helicity Flip and Pockels Cell High Voltage

Figure 27 shows the Pockels Cell (PC) high voltage (HV) while the helicity is flipping. The Pockels Cell HV changes between +3 kV to -3 kV.

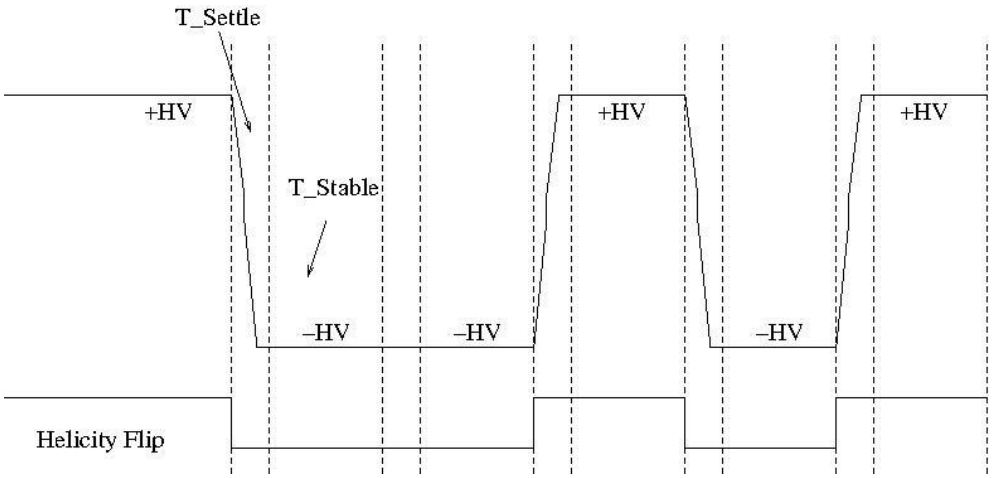

Figure 27: Pockels Cell HV showing the Helicity Flip.

IA Control Signals

To be able to do charge feedback with Intensity Attenuator (IA) and cancel the electro-optical hysteresis of the Pockels Cell, the Helicity Board has two output signals indentifying the current and the previous patterns. Figure 28 shows the IA0 and IA1 signals when the Pair pattern is selected. Figure 29 shows the same when the Quartet pattern is selected. Similarly for the Octet pattern.

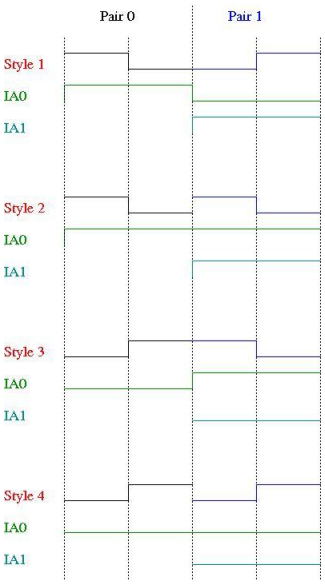

Figure 28: IA control signal IA0 and IA1 with the Pair pattern in relation to the Helicity Flip signal.

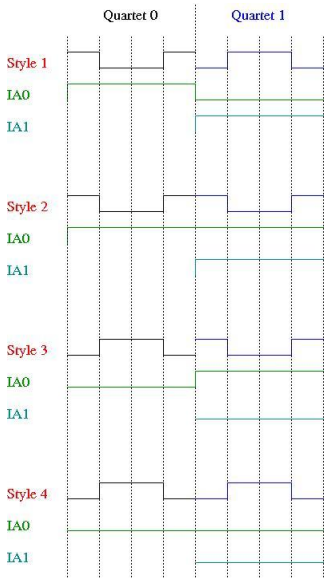

Figure 29: IA control signal IA0 and IA1 with the Quartet pattern in relation to the Helicity Flip signal.

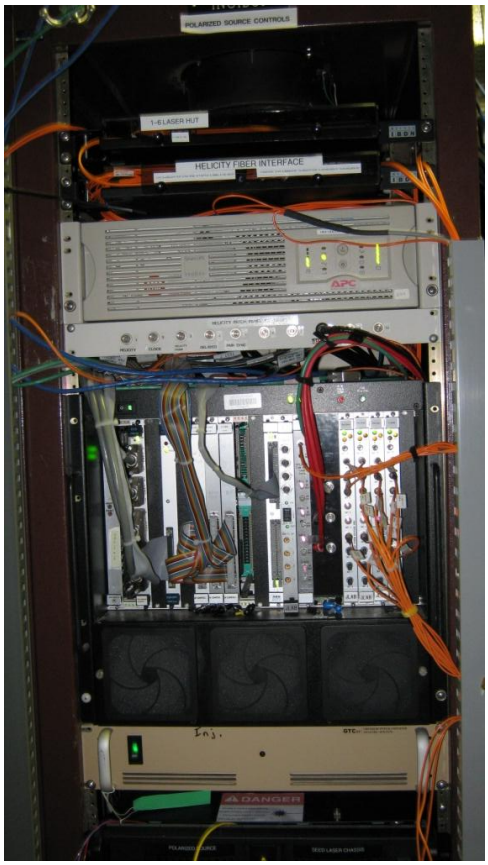

Figure 30: This is rack IN01B05. The fiber cable from the Helicity Board comes to the "Helicity Fiber Interface" patch panel in top of this rack. Five signals make it to the crate (iocin6) under the patch panel. The four FAN IN/OUT cards in this crate distribute Pair Sync, Delayed Helicity, T_Settle, and Pattern Sync to the Halls and Injector DAQ. This crate is only used to provide power to the cards. There is also an FT card to be able to look at these signals on a scope. This crate also has the 20 MHz FAN IN/OUT card.

Fibers Distribution in Injector

We used the existing T120 fibers to carry the 20 MHz Clock signal from IN01B05 to the Injector Parity DAQ in IN02B24 and to the Parity DAQ in Hall C. The old name of T_Settle is “MPS” and the old name of Pattern Sync is “QRT”.

There are four fibers FAN IN/OUT cards in iocin6 crate, see Figure 30. We still need special 1 Fiber FAN IN/OUT for the 20 MHz Clock signal.

Now we have also a Fiber Transducer (FT) in this crate to change the signals from fiber to analog.

The fiber cable from the isolated rack to rack IN01B05 has 12 fibers. The first 10 are shown in Figure 31. Fiber 11 is iochelgen TX and Fiber 12 is iochelgen RX.

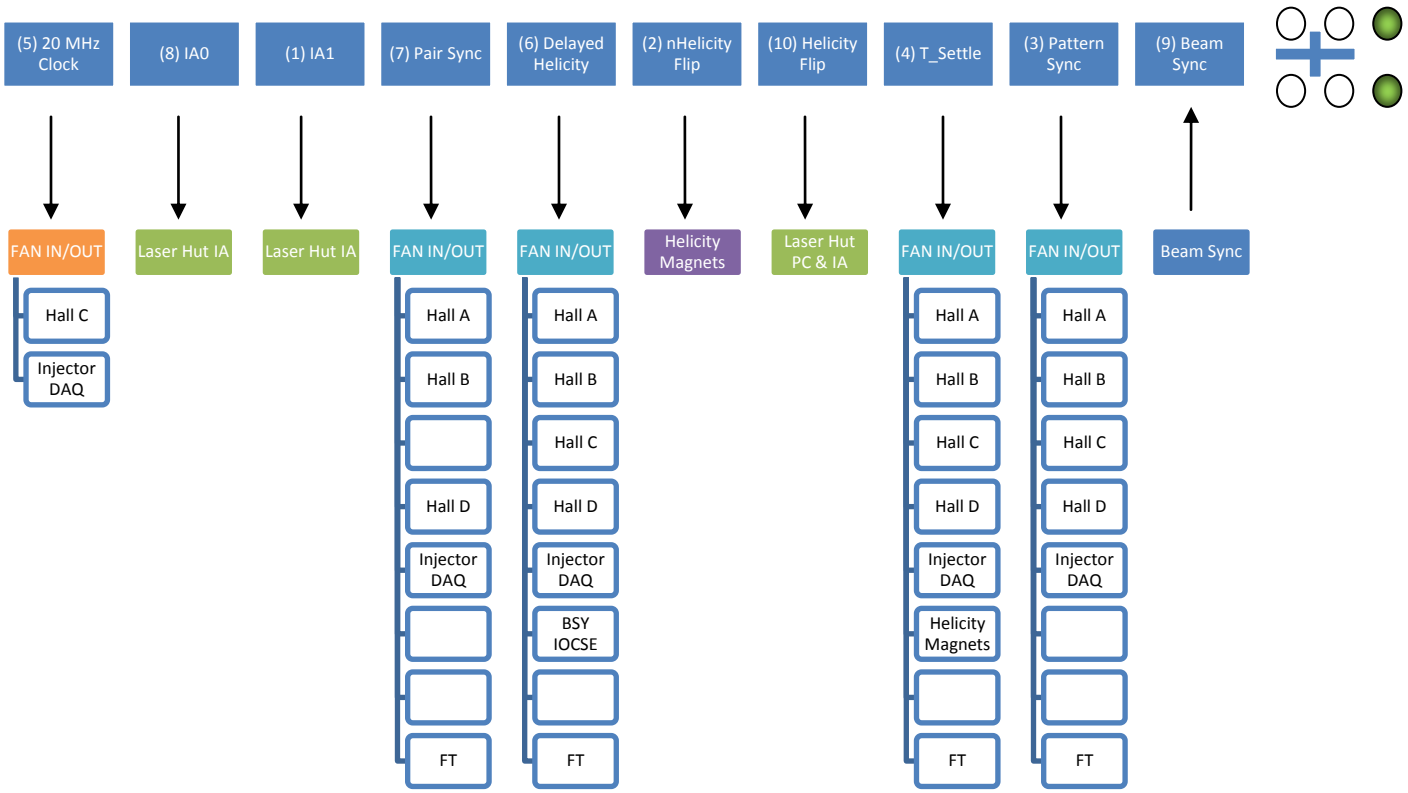

Figure 31: Helicity Control Board signals. Note that Hall C does not receive Pair Sync signal.

Fibers Distribution to the Halls

The following diagram shows the fiber distribution from the Injector to the Halls.

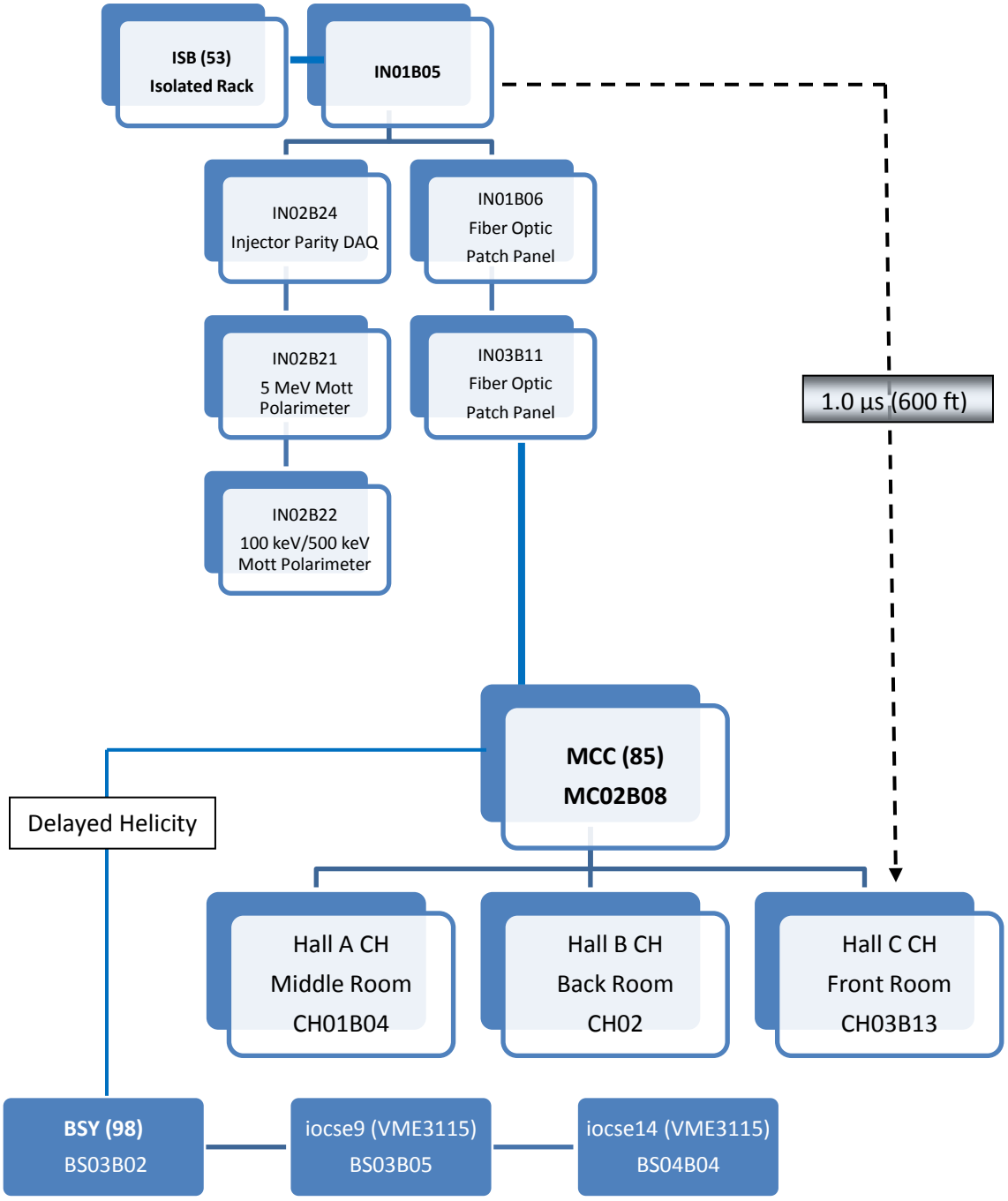

Figure 32: The distribution of the Helicity Board signals to the Halls.

How to Reduce 60 Hz Line Noise?

There are three ways to reduce 60 Hz line noise.

1. Select T_Stable such that: f>1 kHz (Free Clock Mode). This way the contribution of the 60 Hz line noise does not change by much from one window to the next and thus cancels when calculating the asymmetries (A). Even a better cancellation is achieved when using Quartet or Octet patterns. The data will still have full information about the 60 Hz line noise.

2. Integrate over 60 Hz noise per helicity window (Free Clock Mode): Select T_Stable = 33,330 μs (exactly two 60 Hz cycles). This is an exact cancellation and the data collected will have no information about 60 Hz line noise.

3. Cancel 60 Hz line noise using patterns (it does not cancel per window; however it cancels when the differences are calculated). Use the Beam Sync Mode:

    - Select 30 Hz Line Sync: Select a T_Settle, then $T\_Stable = 33{,}333\ \mu s - T\_Settle$

      Select Pair Pattern. Then, $A = \frac{+1-2}{+1+2}$

    - Select120 Hz Line Sync: Select a T_Settle, then $T\_Stable = 8{,}333\ \mu s - T\_Settle$

      Select Quartet Pattern. Then,

      $$A = \frac{+1-2-3+4}{+1+2+3+4}$$

    - Select 240 Hz Line Sync: Select a T_Settle, then $T\_Stable = 4{,}167\ \mu s - T\_Settle$

      Select Octet Pattern. Then,

      $$A = \frac{+1-2-3+4-5+6+7-8}{+1+2+3+4+5+6+7+8}$$

What about other noises? Choice (1) will work as well for other low frequency noises including the noise from target density fluctuation which is peaked at low frequency because it is a mechanical noise due to gas bubbles in the Hall cryogenic liquid target. Choices (2) and (3) are geared for 60 Hz noise; other noises will remain in the data. These noises will increase the width of the helicity correlated distributions like the target density fluctuations. While prominent single low frequency noise will cause double-horned peaked distributions. For more details see (Ramsay, 2009).

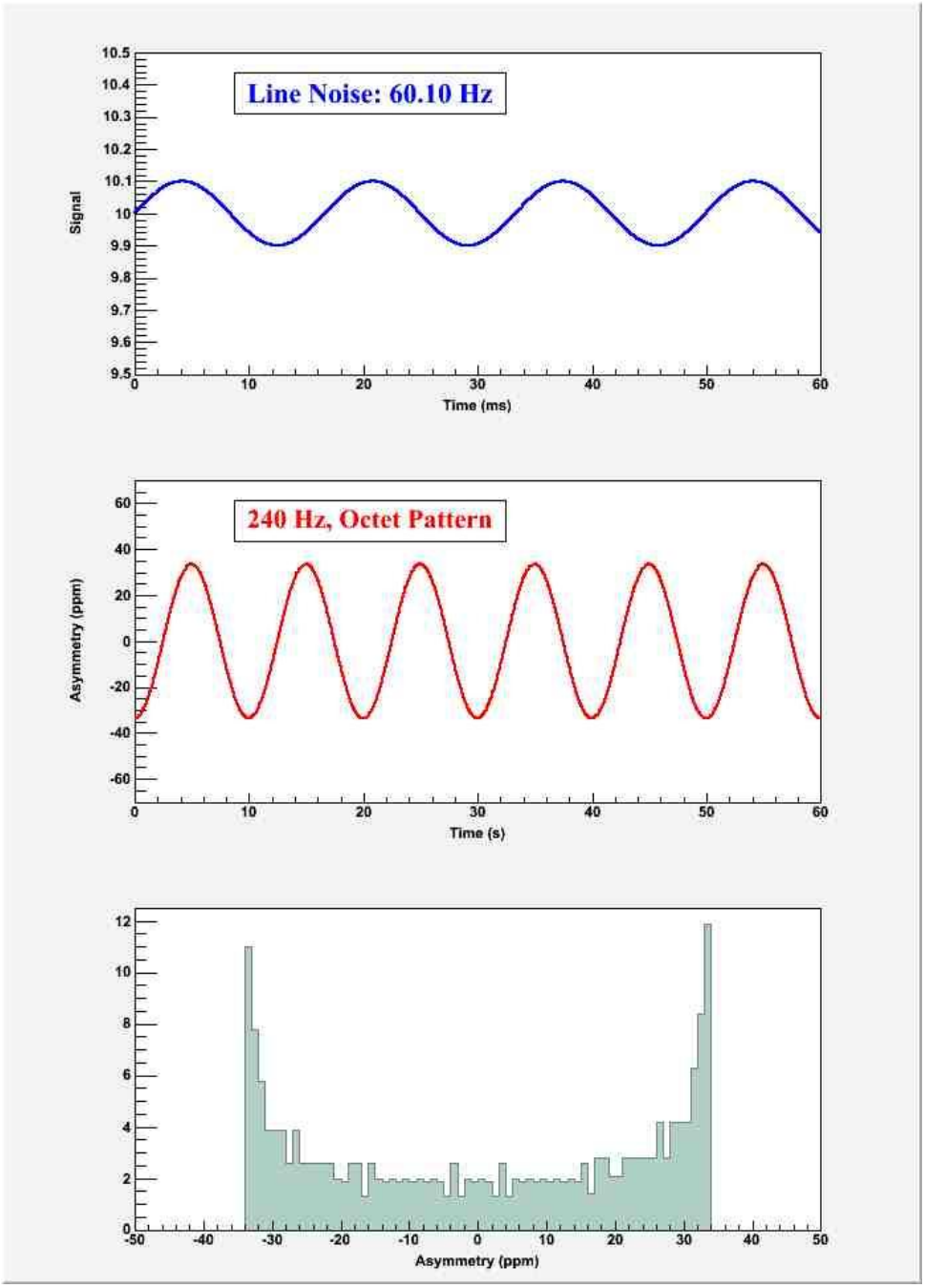

Figure 33: Line noise and its cancellation. If the frequency is not exactly 60 Hz, then there is double peaked.

Helicity Board Tentative Configuration for PREx and Qweak

The tentative Helicity Board configuration for PREx is shown in Figure 34 and for QWeak is shown in Figure 35. Table 3 shows the Helicity Board configuration.

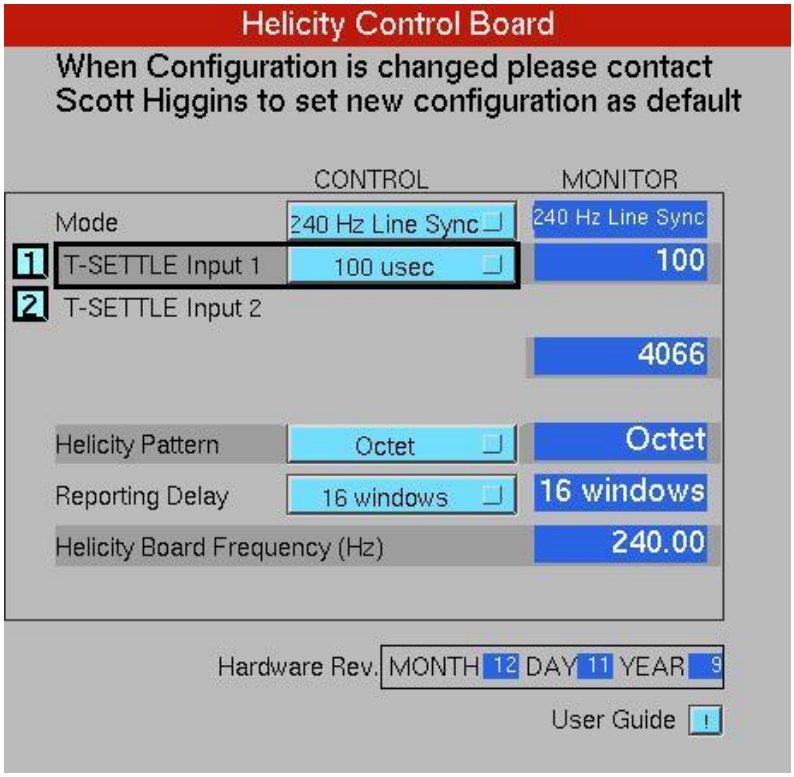

Figure 34: Helicity Board Control Screen with PREx settings.

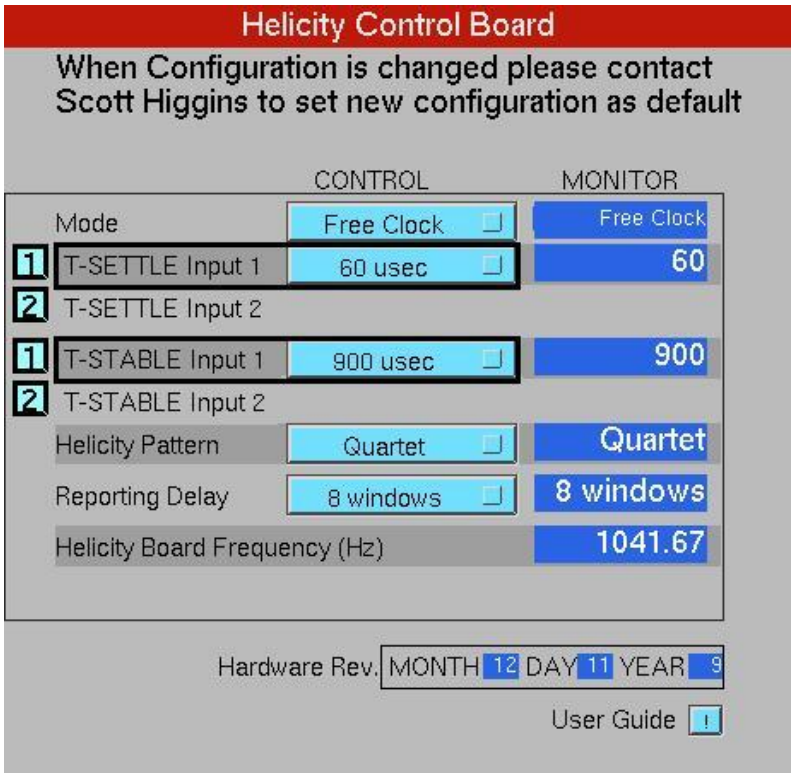

Figure 35: Helicity Board Control Screen with QWeak settings.

Table 3: The Helicity Board tentative configuration for PREx and QWeak.

Helicity Board Setting	PREx	QWeak
Mode	240 Hz Line Sync	Free Clock
T_Settle	100 µs	60 µs
T_Stable	4,050 µs	900 µs
Helicity Pattern	Octet	Quartet
Reporting Delay	16 windows	8 windows
Helicity Board Frequency	240 Hz	1042 Hz

Sign of Physics Asymmetry

One may wonder how could we tell the actual helicity of the electrons when they interact with the target in the Hall. Parity Experiments measure very small asymmetries that can easily be positive or negative. There is standard theoretical prediction of the magnitude and sign of the physics asymmetry. However, the new physics that the experiment is trying to measure may be big enough to change the sing of the asymmetry.

This is easy: no need to keep track of all these conventions about helicity and how it is treated at each junction. This is simply done using the Moller Polarimeter in the Hall. The sign of the asymmetry measured in the Hall is decided using the Moller Polarimeter. Moller asymmetry is well understood in theory and the sign of the measured polarization is well known. To check the relative sign between the Moller Polarimeter DAQ and the Parity DAQ, a large charge asymmetry is introduced in the injector by changing the Pockels Cell HV (PITA) and both DAQs measure this charge asymmetry at the same time to find out the relative sign.

Helicity Board Circuit Diagram and Description

Electronic Cross-talk and Ground Loop Elimination in the Injector

Extra effort was spent to make sure the real time helicity signal is isolated. These include:

I. The crate that houses the Helicity control board is floating and also powered with an Isolation transformer.
II. The Helicity Board generates two real time helicity signals: Helicity Flip and nHelicity Flip, so the current drawn by the board does not depend on the helicity state.
III. The outside world receives only the Delayed Helicity signal. This signal tells what the helicity was in the past so there is no knowledge of the real time helicity.
IV. The Helicity Magnets Crate which receives on e of the two real time helicity signal (nHelicity Flip) is also floating and powered by an isolation transformer.
V. The real time helicity signal (Helicity Flip) that goes to the Laser Hut is isolated.

All information for programming and readback of signals related to helicity components (Pockels Cell and IA's) passes through a new isolator card. This card uses the ISO-124 chip to isolate signals from -10 V to +10 V with a bandwidth of up to 50 kHz. The card we have designed will isolate 8 channels from the service building down to the laser room, and 4 channels from the laser room back up to the service building. We will have 3 of these cards in place. We will need to ensure that any signal that is placed on

a channel from tunnel to service building is heavily filtered with at least a 100ms time constant filter to ensure there is no real time helicity information being passed.

All circuits seeing real time helicity are floating with respect to earth ground. The option remains to connect a single point ground if requested by the researchers.

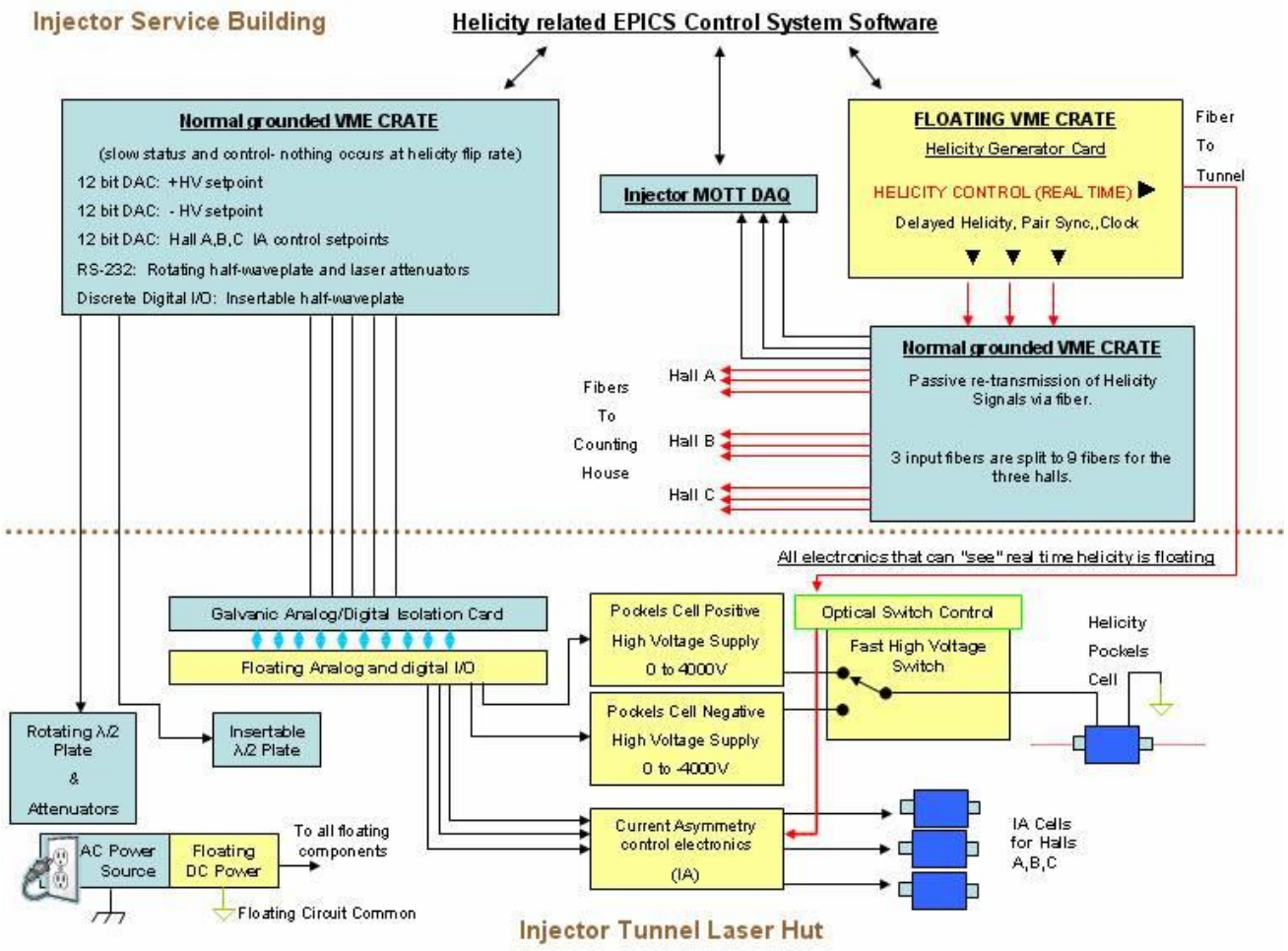

Figure 36: Ground loop elimination in the Injector.

Bibliography

Ramsay, D. (2009, February 20). *False Asymmetry from Fixed-Frequency Noise in the Qweak DAQ*. Retrieved from http://qweak.jlab.org/doc-private/ShowDocument?docid=906