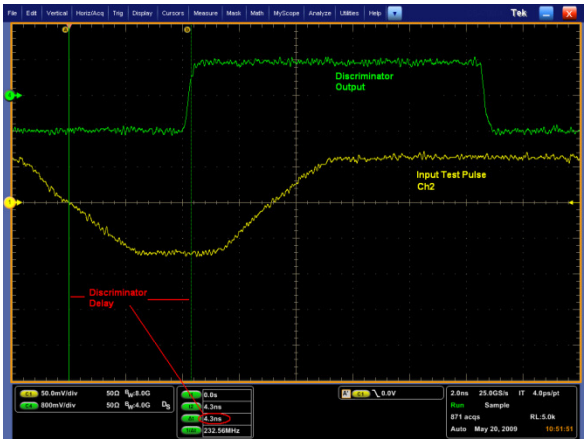
JLab 16 Channel Discriminator V2: Prototype Measurements 2009

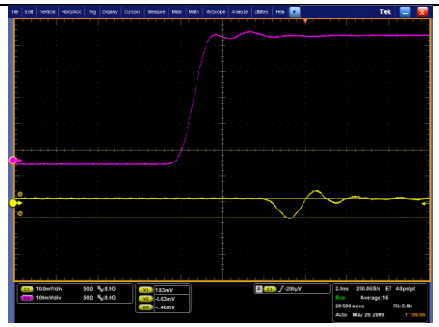
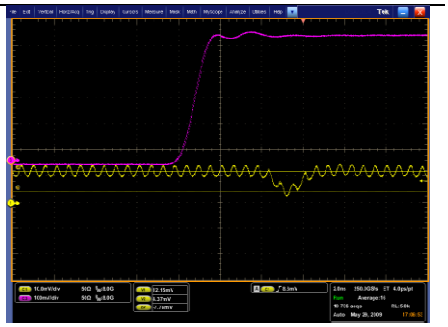
Discriminator Delay (measured on channel 2): 4.3ns



Notes:

- Channels 1 & 2 have the longest delays due to front-panel connectors & layout

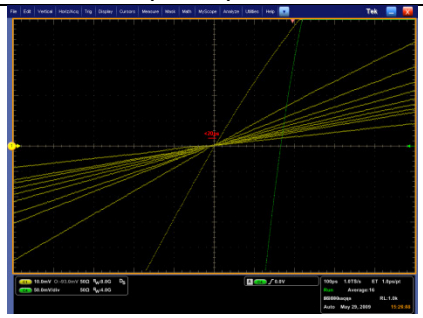
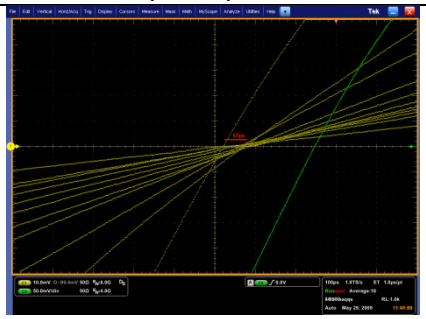
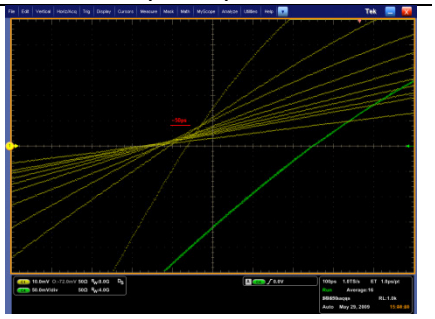
Discriminator Channel Isolation (Test Pulse 1V/ns step):

JLab Rev 2 (ch1->2)	JLab Rev 1 (ch7->8)	V895 (ch7->8)
<350µV, >69dB ch-ch Isolation	7.4mV, >42dB ch-ch Isolation	7.7mV, >42dB ch-ch Isolation
		

Notes:

- v895 (2 boards checked) have a ~1.8GHz ringing on all inputs (~5mV pk-pk)
- JLab Rev 2 Vertical Scale = 1mV/div, JLab Rev 1 & v895 Vertical Scale = 10mV/div

Discriminator Slew Rate Dispersion:

JLab Rev 2	JLab Rev 1	V895
~20ps Dispersion	~65ps Dispersion	~50ps Dispersion
		

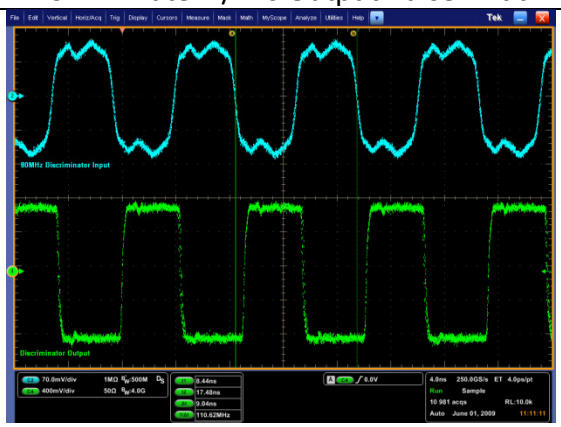
Notes:

- Input Signal: 356mV, 30ns width negative pulse
- Discriminator Overdrive: 100mV
- Edge Speed: 250mV/ns – 20mV/ns
- Pulse Rate: 100Hz

Discriminator Overdrive Dispersion:

Discriminator Maximum Rate (non-updating mode):

110MHz Rate w/4ns Output Pulse Width



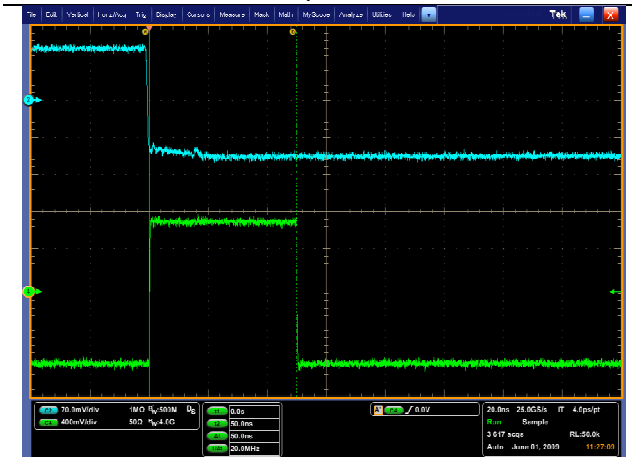
80MHz Rate w/8ns Output Pulse Width

Notes:

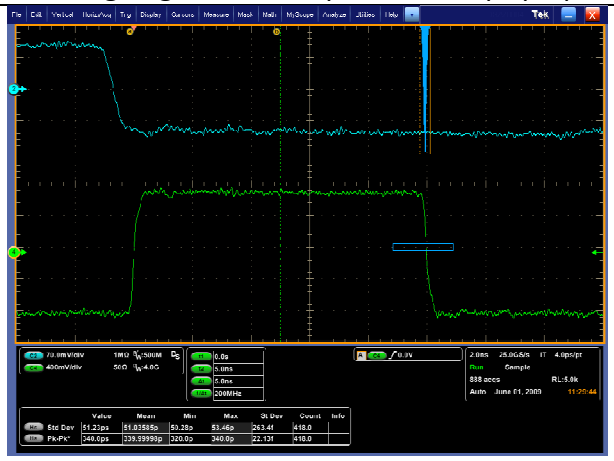
- Pusler Dead-time: ~4.5ns, constrained by maximum pulse width

Discriminator Output Pulse Width:

Maximum Output Width = 50ns



Trailing Edge Jitter = 51ps RMS, 340ps pk-pk

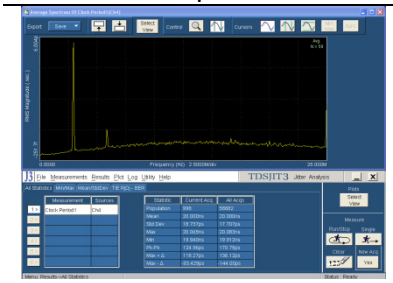
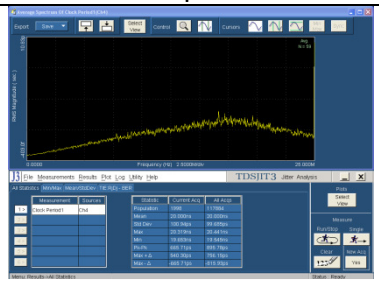
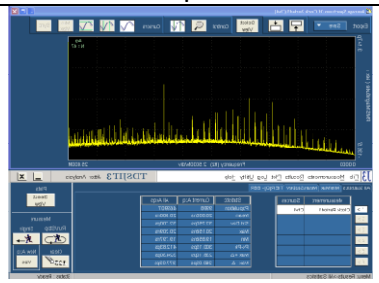


Notes:

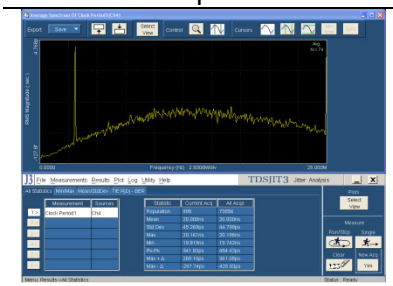
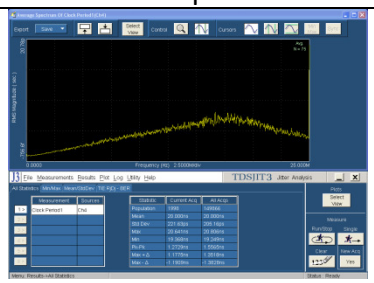
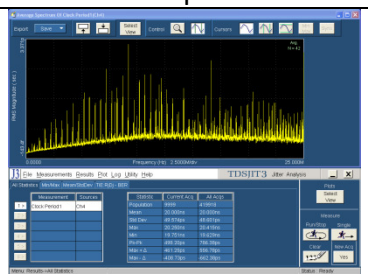
- Trailing edge jitter will likely be improved in next revision by switching to ground referenced driver for pulser output section.
- Maximum pulse width of 50ns put pulser dead-time ~4.5ns

Discriminator Jitter:

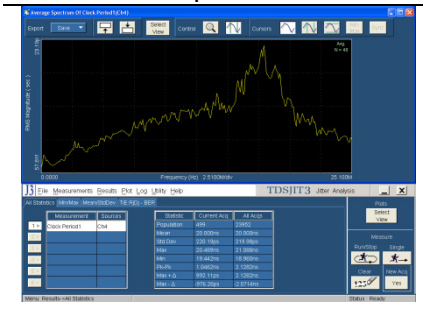
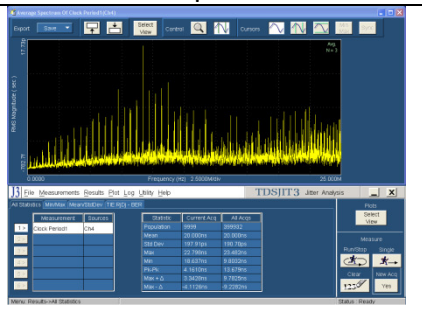
50MHz, 100mVpp Sine Wave:

JLab Rev 2	JLab Rev 1	V895
17.7ps RMS	99.6ps RMS	32.7ps RMS
		

50MHz, 50mVpp Sine Wave:

JLab Rev 2	JLab Rev 1	V895
44.8ps RMS	205.1ps RMS	48.6ps RMS
		

50MHz, 10mVpp Sine Wave:

JLab Rev 2	V895
220ps RMS	190.7ps RMS
	

Minimum Threshold: