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# Digital Pulse Processing


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# CAEN Waveform Digitizers

| | Channels | | | | | | | Form factor / Interfaces | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | VME | NIM | Desktop | PCI Express |
| Series | VME | NIM/Desktop | PCI Express | Max. Sampling Rate (MS/s) | Bandwidth (MHz) | Resolution (bits) | Memory (MS/ch) | VME64 Opt. link | USB2.0 Opt. link | USB2.0 Opt. link | PCI Express |
| 724 | 8 | 4 | 2 | 100 | 40 | 14 | 0.5/4 | Ready | New | New | Coming Soon |
| 720 | 8 | 4 | 2 | 250 | 125 | 12 | 1.25/10 | Ready | New | New | Coming Soon |
| 721 | 8 | - | - | 500 | 250 | 8 | 2 | Ready | - | - | - |
| 731 | 8-4 | - | 2-1 | 500-1000 | 250/500 | 8 | 2-4 | Ready | - | - | Coming Soon |
| 740 | 64 | 32 | - | 65 | 30 | 12 | 0.19/1.5 | Ready | New | New | - |
| 751 | 8-4 | 4-2 | - | 1000-2000 | 500 | 10 | 1.8-3.6 | New | Coming Soon | Coming Soon | - |
| 742(1) | 32+2 | 16+1 | - | 5000 | Tbd | 12 | 0.128 | Coming Soon | Coming Soon | Coming Soon | - |

(1) Switched capacitor

= New Products

= Coming Soon

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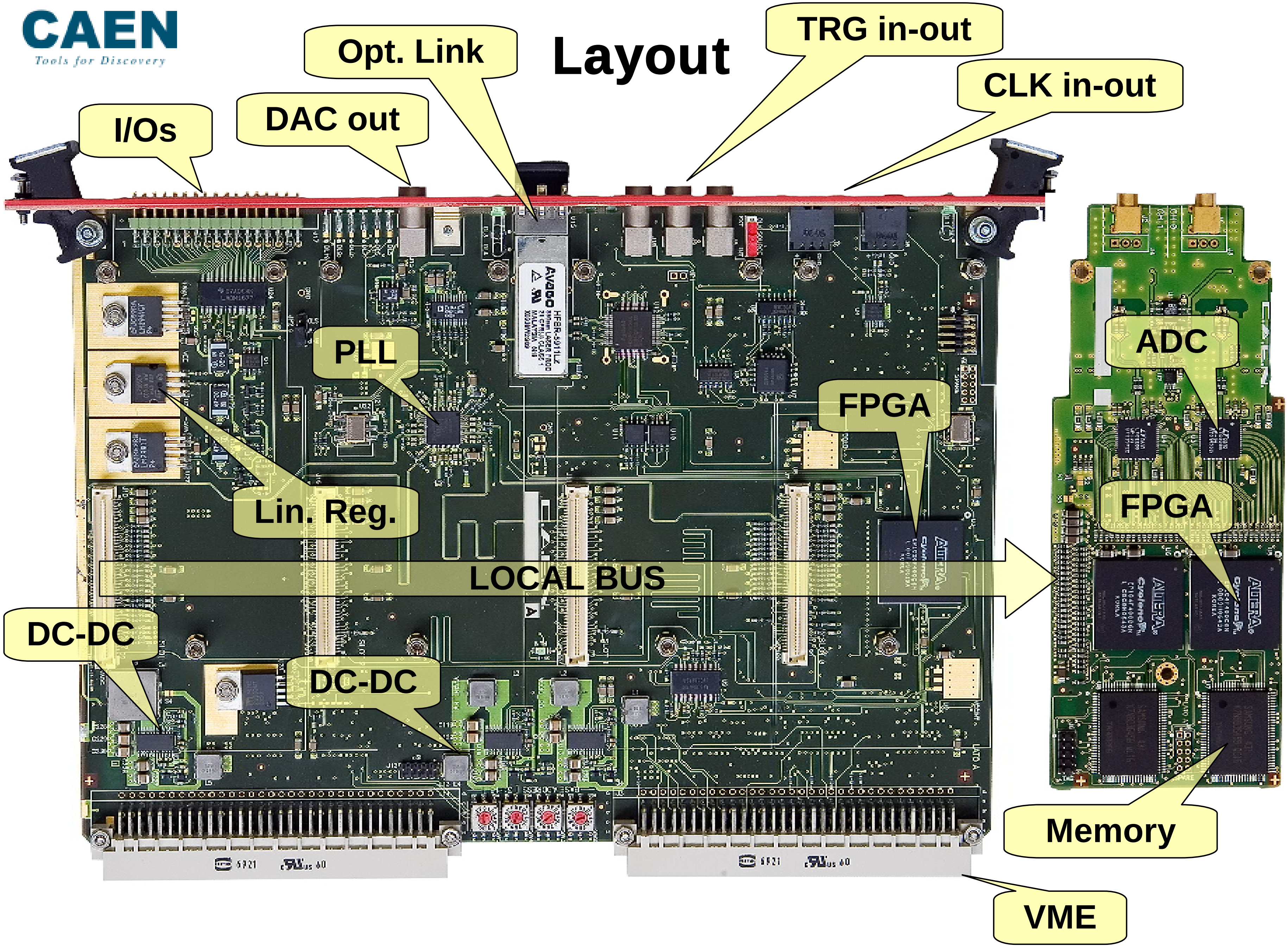
# Main features

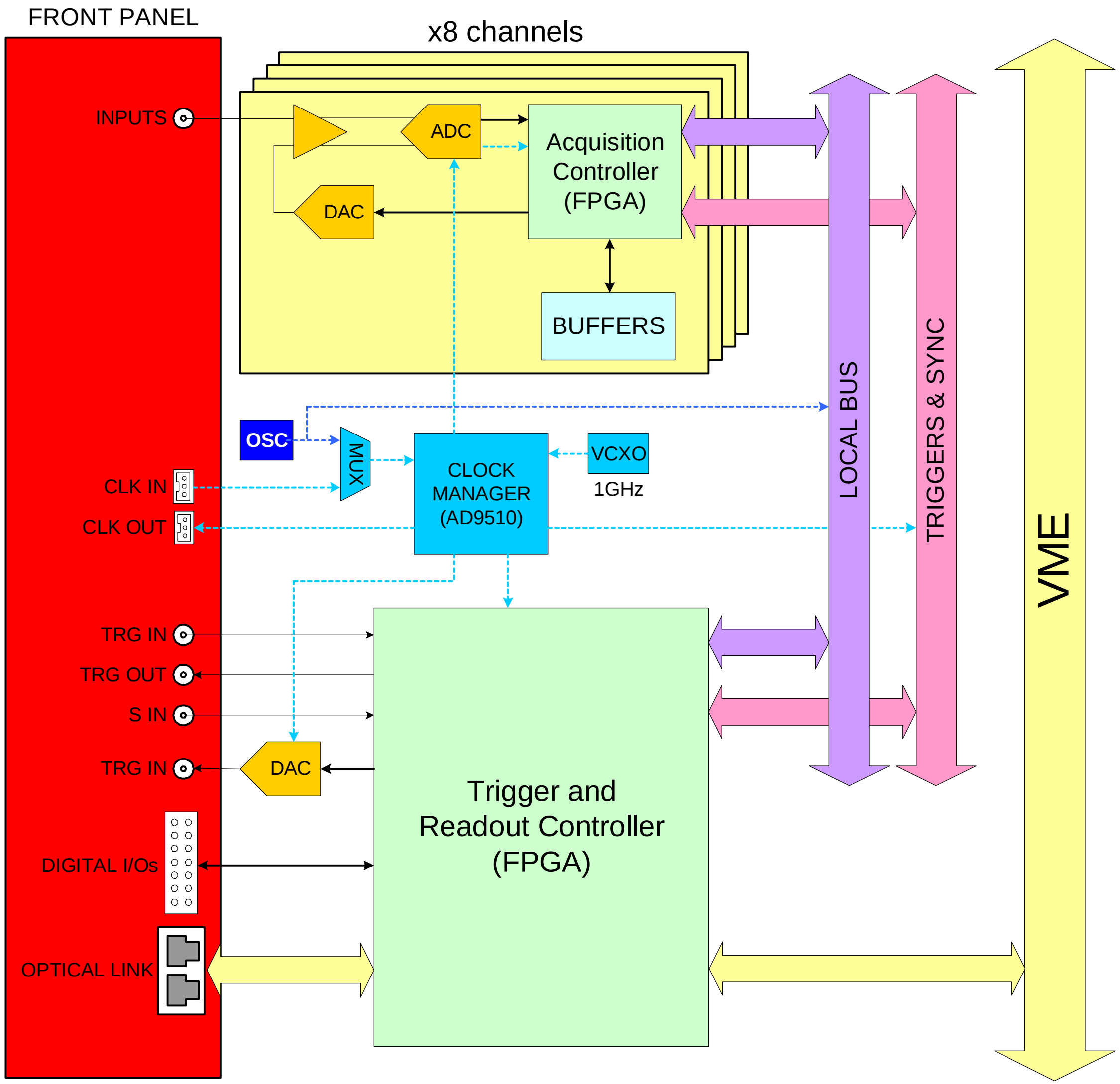
- From 2 to to 64 channels
- Up to 5 GS/s sampling rate
- Up to 14 bit resolution
- VME, NIM, PCI Express and Desktop form factors
- Available VME64X, Optical Link, USB 2.0, PCI Express Interfaces
- Memory buffer: up to 10MB/ch (max. 1024 events)
- Multi-board synchronization and trigger distribution
- Programmable PLL for clock synthesis
- Programmable digital I/Os
- Analog output with majority or linear sum
- FPGA fimware for Digital Pulse Processing
  - Zero Suppression
  - Smart Trigger for pulse detection
  - Trapezoidal Filters for energy calculation
  - Digital CFD for timing information
  - Particle Identification
  - Multichannel Scaler
  - Digital QDC
  - Digital Peak Sensing
  - Possibility of customization
- Software Tools for Windows and Linux

# Layout



Opt. Link
TRG in-out
CLK in-out
I/Os
DAC out
PLL
ADC
FPGA
FPGA
Lin. Reg.
LOCAL BUS
DC-DC
DC-DC
Memory
VME

# Block Diagram



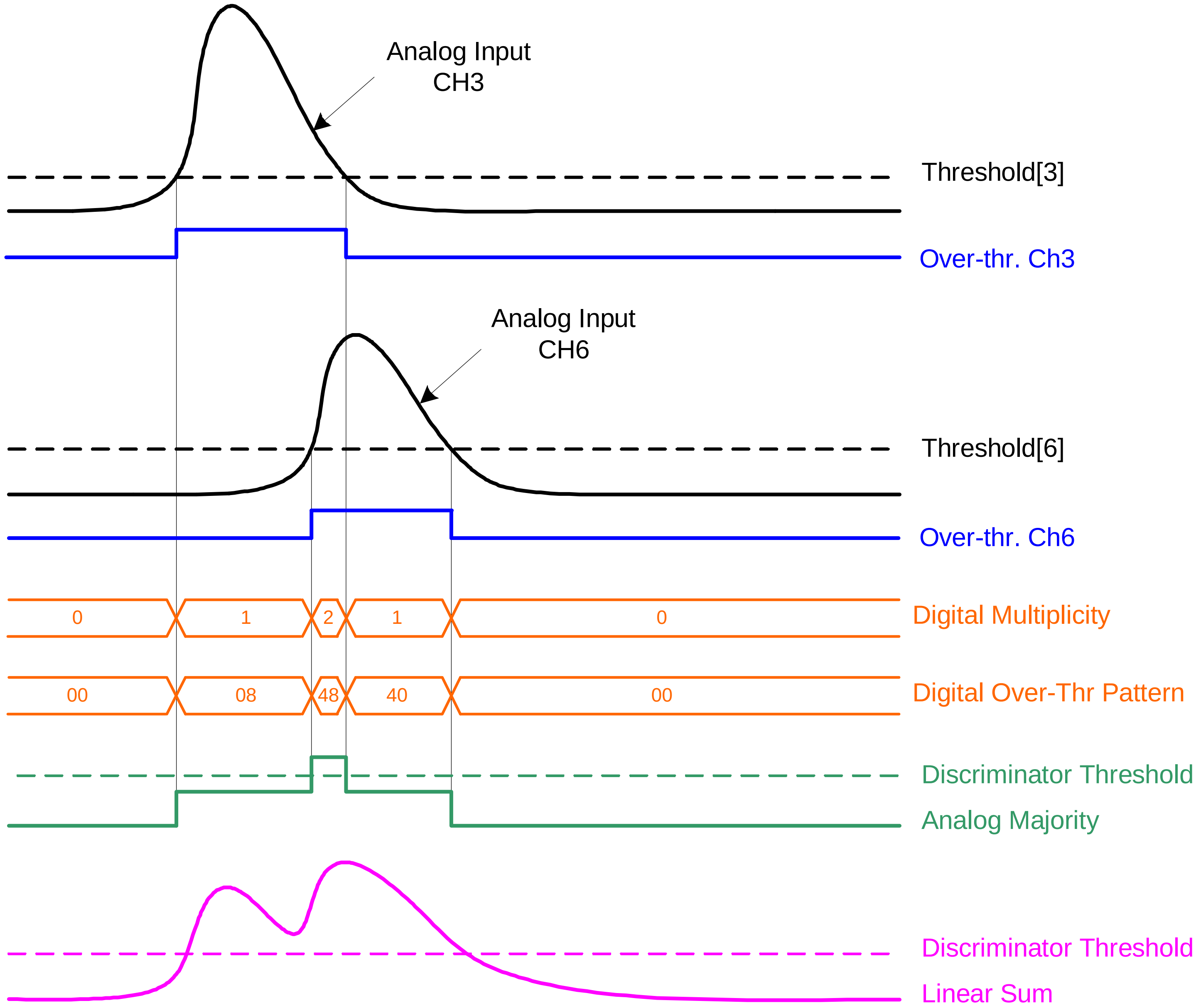
# Multi-board synchronization

- Clock distribution
  - The reference clock can be distributed in daisy chain through the clock-in and out connectors (LVDS)
  - One board can act as a clock master
  - High performance and low jitter PLL for clock synthesis
  - Programmable clock phase adjust to compensate the cable delay
- Time tag
  - Trigger time tag synchronous with the ADC sampling clock
  - Sync input to keep the time alignment between boards

# Triggers and acquisition

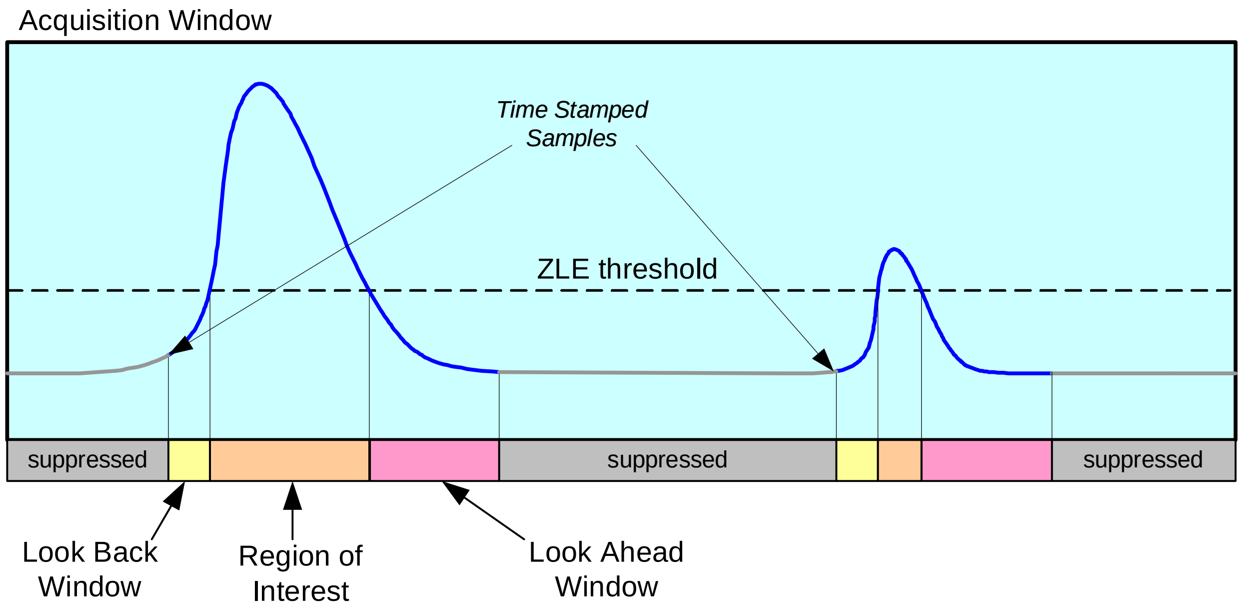
- Global trigger (hardware or software) or individual self-triggers
- Pulse triggering
- Trigger propagation from one channel/board to the others
- Analog output with linear sum or majority
- 16 programmable digital I/Os (event tagging, trigger logic, etc...)
- Coincidence/anti-coincidence logic
- Other trigger logic can be implemented in the FPGAs

# Triggering examples



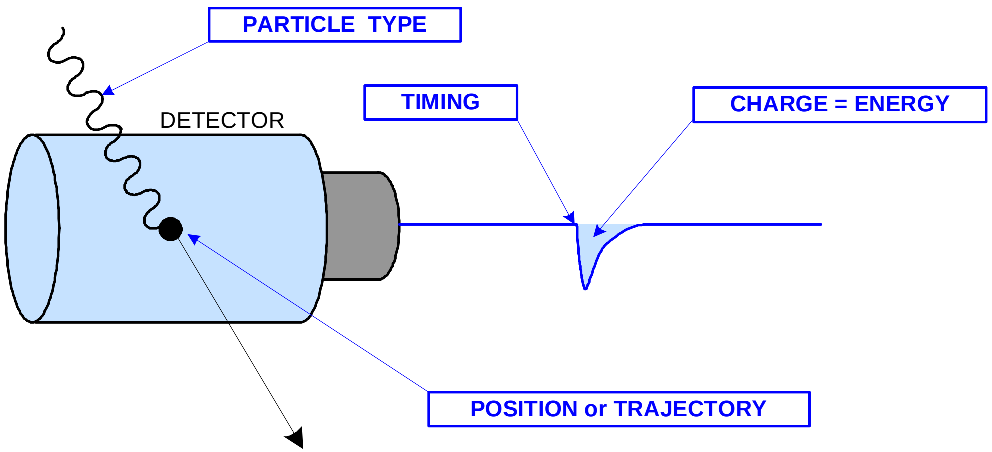
# Zero Suppression

- Programmable Thresholds and Windowing
- ***Full event suppression***: one event (acquisition window) is discarded if the signal (or its integral) does not exceed the threshold
- ***Zero Length Encoding***: only the parts exceeding the threshold (plus a certain number of samples before and after) are saved.
- Other data reduction techniques are being developed in collaboration with some users



# Digitizers for Physics Applications

- Detectors give pulses: want to know charge, timing, shape, etc...
- Modern ADC chips allow to digitize the signals with high sampling frequency and/or number of bits: good resolution!
- A/D conversion must be done as early as possible to preserve the information
- The major problem is the **throughput rate** (readout bandwidth)
- No possible to read row data and make the analysis off-line
- The FPGA can do on-line digital pulse processing (DPP) to extract and save only the quantities of interest



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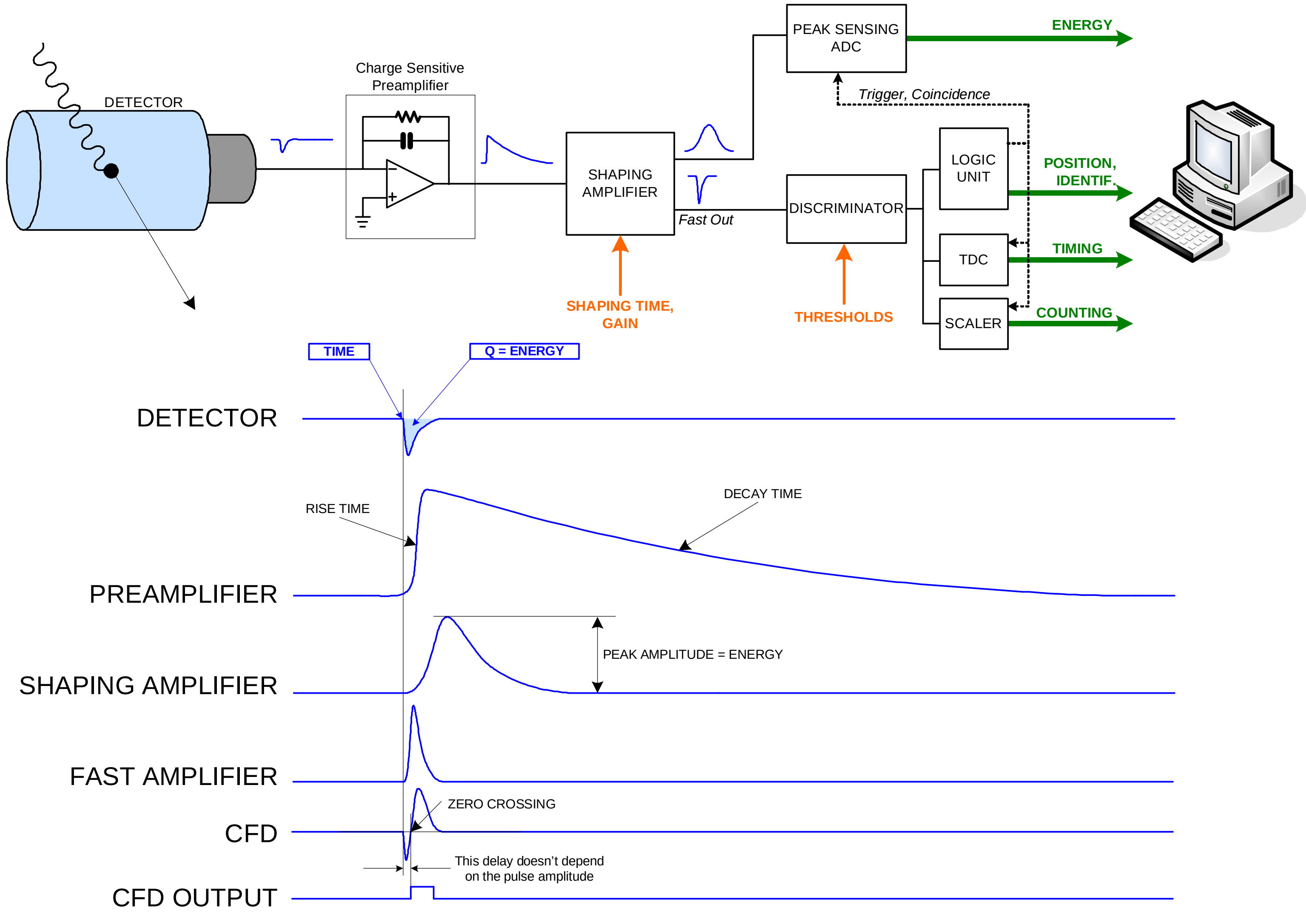
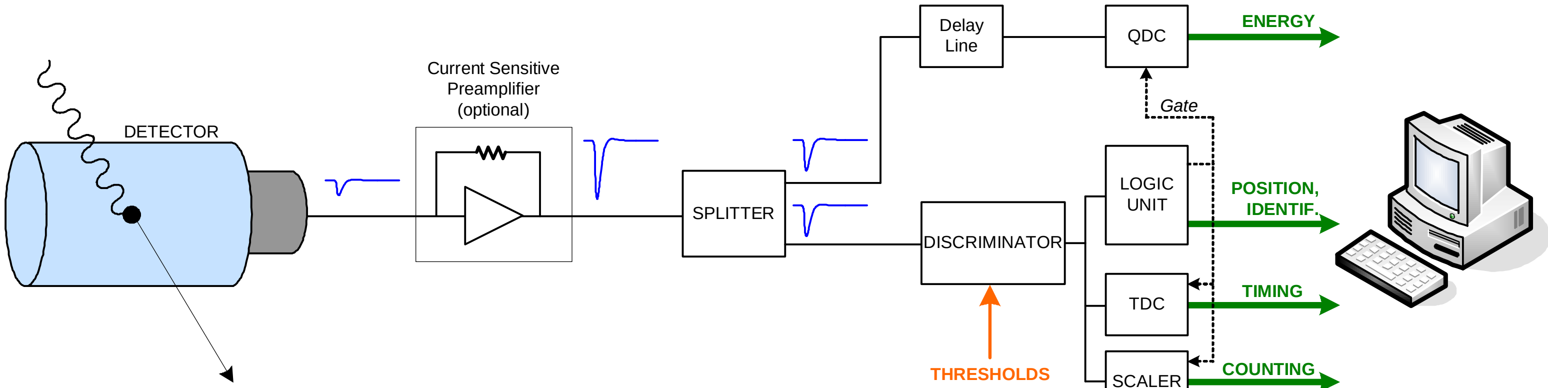
# Traditional analogue chain

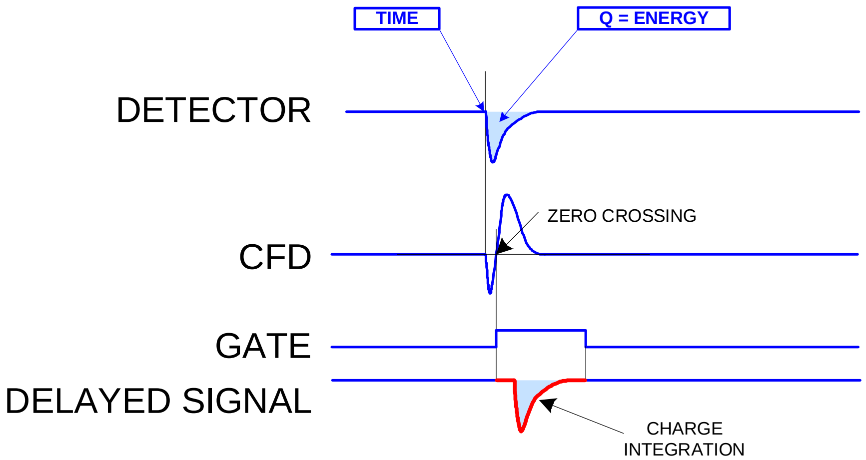
## using charge sensitive (integrating) preamplifiers



# Traditional analogue chain

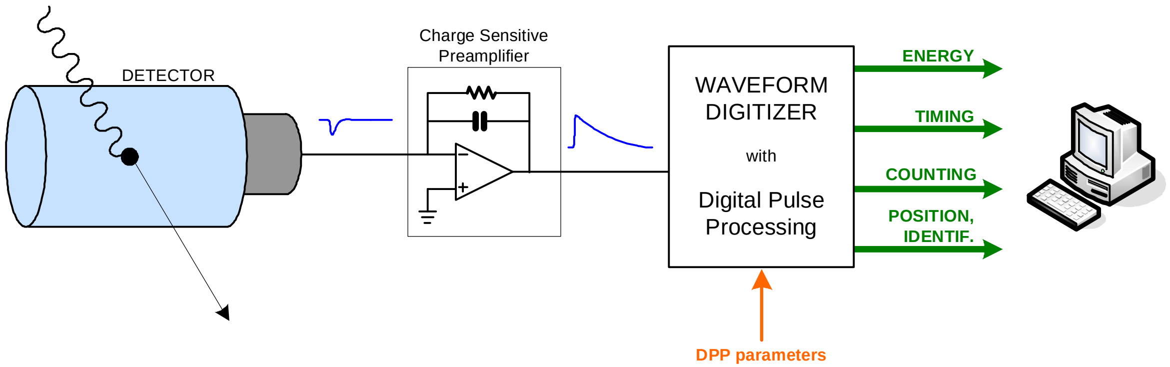
## using current sensitive (trans-impedance) preamplifiers




- The QDC is not self-triggering; you need a gate generator
- You need delay lines to compensate the delay of the gate logic (long cables!)

# Digital approach

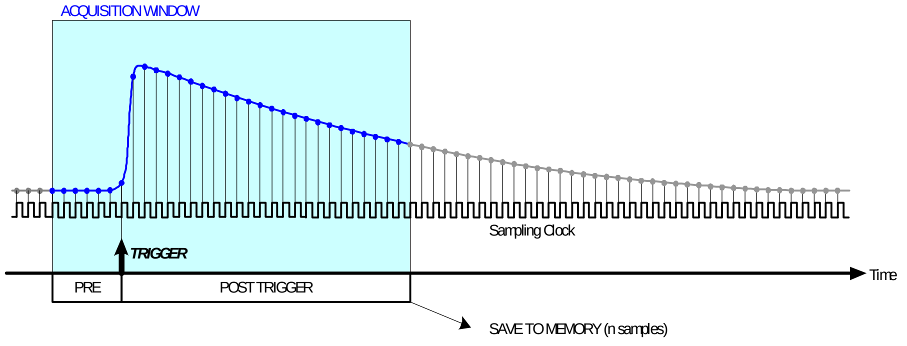


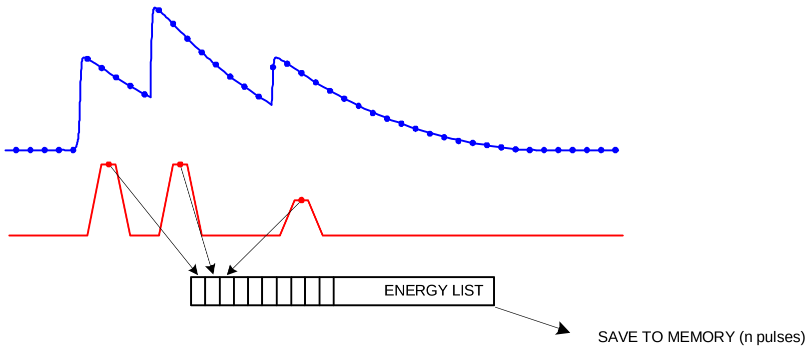

## OSCILLOSCOPE MODE

- there is a circular buffer of programmable size
- when a channel is triggered, the current buffer is saved (acquisition window)
- the acquisition can continue without dead-time in a new buffer

## MCA/LIST MODE

- the digitized signal is processed on-line and the acquisition is continuous
- the quantities of interest are calculated and saved in the memory buffer
- the amount of data to readout is very small respect to the oscilloscope mode



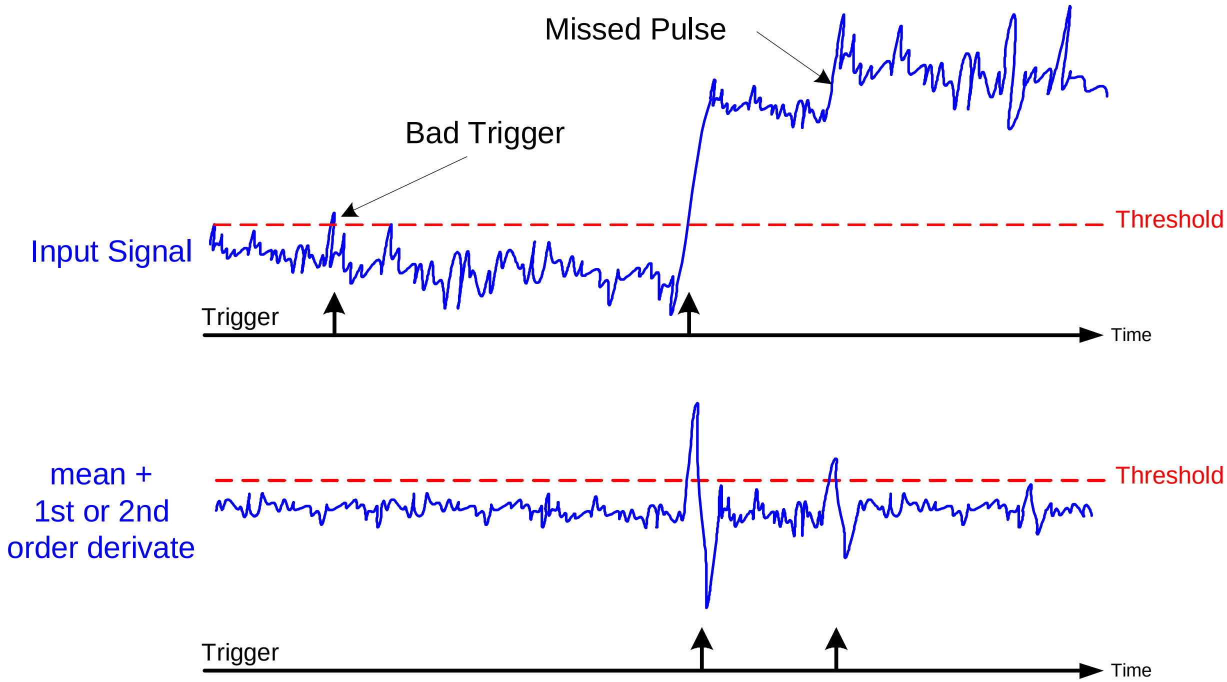



# Triggering on the pulses

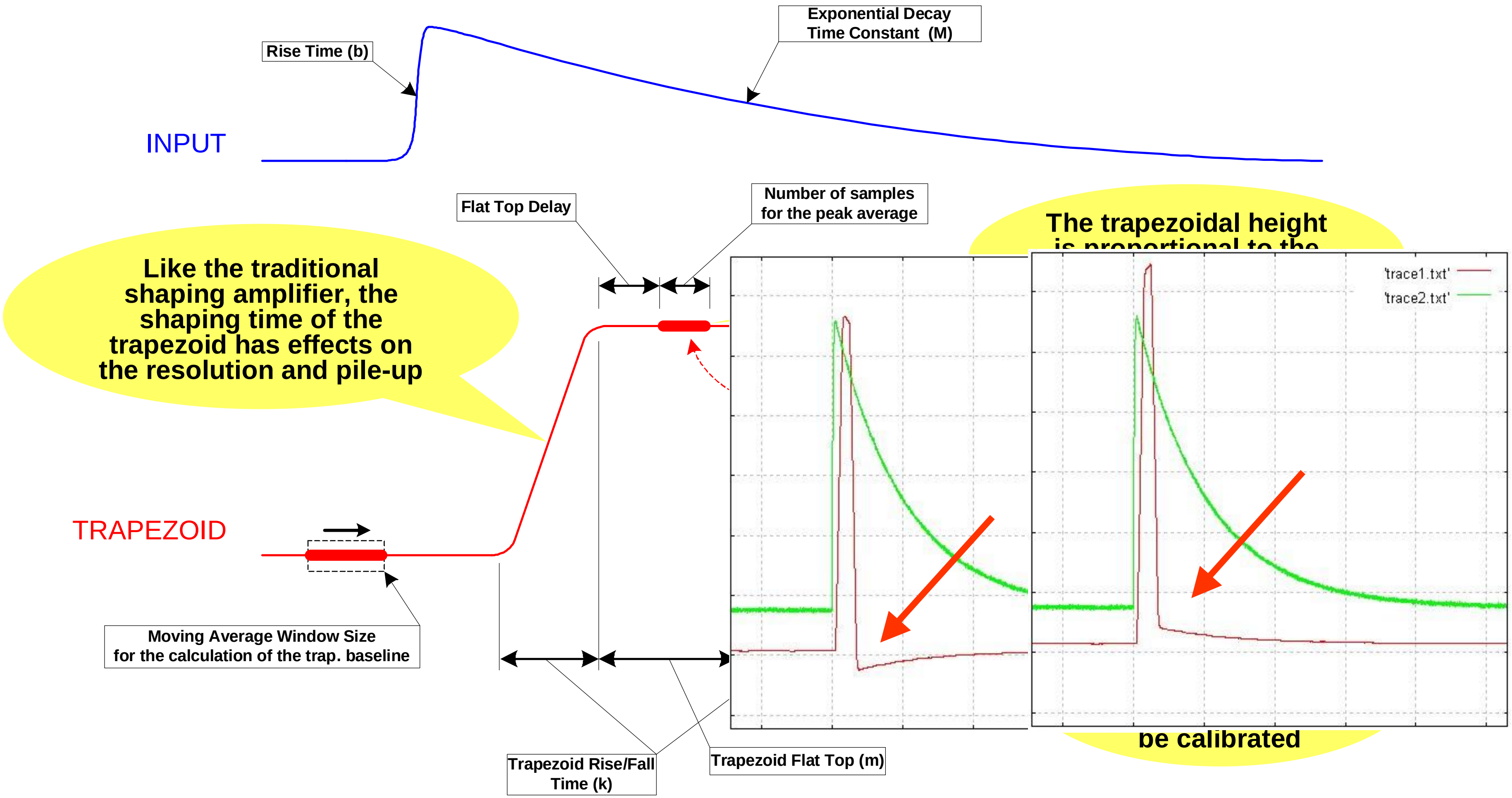
- Triggering problems are due to:
  - Baseline fluctuation
  - Noise
  - Pile-up
  - Random distribution
- Missed pulses can cause:
  - Loss of significant events
  - Bad pile-up rejection
  - Bad baseline restoration
  - Wrong coincidence or anti-coincidence

# DPP algorithms for triggering

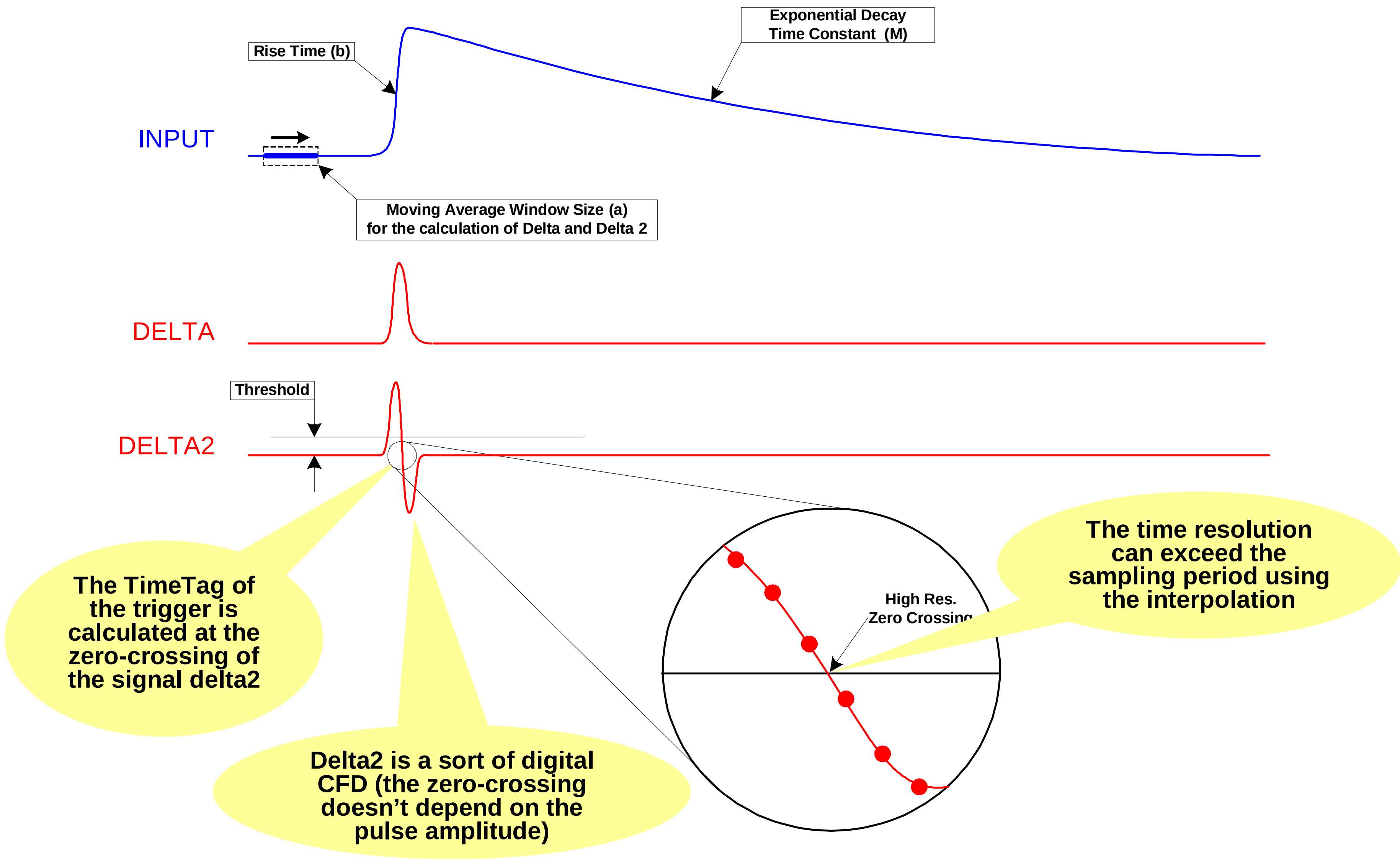
- Programmable digital threshold
- Mean on a moving window to reduce the effect of the high frequency noise
- Signal derivation (1st or 2nd order) to look for the voltage steps
- Constraints on the Time Over Threshold and/or zero crossing



# DPP algorithms for the energy (MCA)

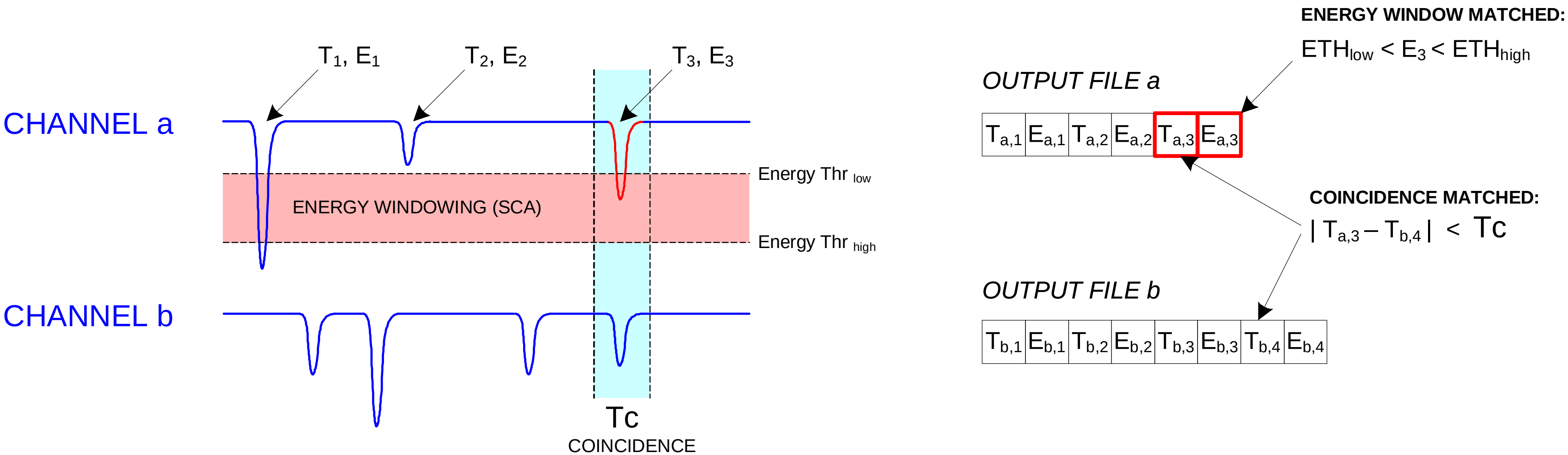


# DPP algorithms for the timing (TDC)



# DPP algorithms for counting (SCA+scaler)

- Read the time-tag and energy lists from the memory of the digitizer and save the data to local buffers or output files
- Select only the pulses within a certain energy range
- Search for coincidence/anticoincidence comparing the time tags
- Generate “virtual” veto/inhibit signals in the software
- The digitizers feature 16 general purpose I/Os and a Sync signal that can operate as hardware gate, veto, tagging signals



# DPP algorithms for the charge integration

- Traditional QDC (Charge Integrator)
  - A simple circuit with a very good resolution but...
  - Need a gate
  - Splitter + Discriminator + Delay line (long cable)
  - May have long conversion time
- Digital integrator
  - Poor resolution with fast signals but...
  - Goes straight into the digitizer input
  - Enormous dynamic range
  - Self and adaptive gate
  - Timing information
  - Pulse analysis and selective rejection
  - Dead-timeless
  - New V1742 (12 bit, 5GSps): the optimal compromise?

# DPP algorithms for the particle identification

- Particle identification: traditional approaches
  - Rise time / energy correlation
  - Rise time discrimination
  - Double charge method
  - Likelihood ratio methods
- Digital algorithms for g-**n** discrimination
  - It's a work in progress (some tests have been done at Legnaro)
  - Pulse Shape Analysis (PSA) can be done on either charge or current sensitive preamplifier output
  - Digital charge integration can easily manage double gates
  - Fast sampling rate needed in most cases (250MHz is OK?)
  - 12 bit should be OK

# Comparision Analog vs DPP

**ADVANTAGES**:

- One single board can do energy, timing and pulse shape analysis => low cost and reliability
- All in digital => good linearity and stability => reproducibility
- Wider dynamic range and uniformity of the performances over the range
- Digital techniques allow better correction of pile-up, ballistic deficit and baseline fluctuation effects
- Preserve pulse information
- You can easily keep synchronized and correlated several channels and make coincidence/anticoincidence after the acquisition (off-line)
- Low dead-time in the acquisition => high counting rate
- Flexibility (all in FPGAs) => you can change and adapt the algorithms => easy tailoring to the application
- Tuning and calibration: register programming instead of manual regulations => faster and automatic

**DISADVANTAGES:**

- Setting up the system requires a deep knowledge of the digital algorithms and the relevant parameters. It takes more time for the beginners.
- Customization requires VHDL knowledge and/or CAEN support
- Loss of resolution with fast signals

# Software: *DPPrunner*

- It is a Demo and a Software Development Kit
- It allows the user to
  - manage the parameters of the acquisition
  - program and readout the digitizers
  - view the waveforms (oscilloscope mode) and the spectra
  - save the data (histograms and lists) to file
- It is not an and user application (no spectroscopic analysis)
- It can be easily interfaced to existing tools (Root, Winner, etc...)
- It is open source; the user can adapt it to the application
- Linux and Windows supported
- The DPPrunner can run in emulation mode (waveform generated by software and/or DPP made off-line)

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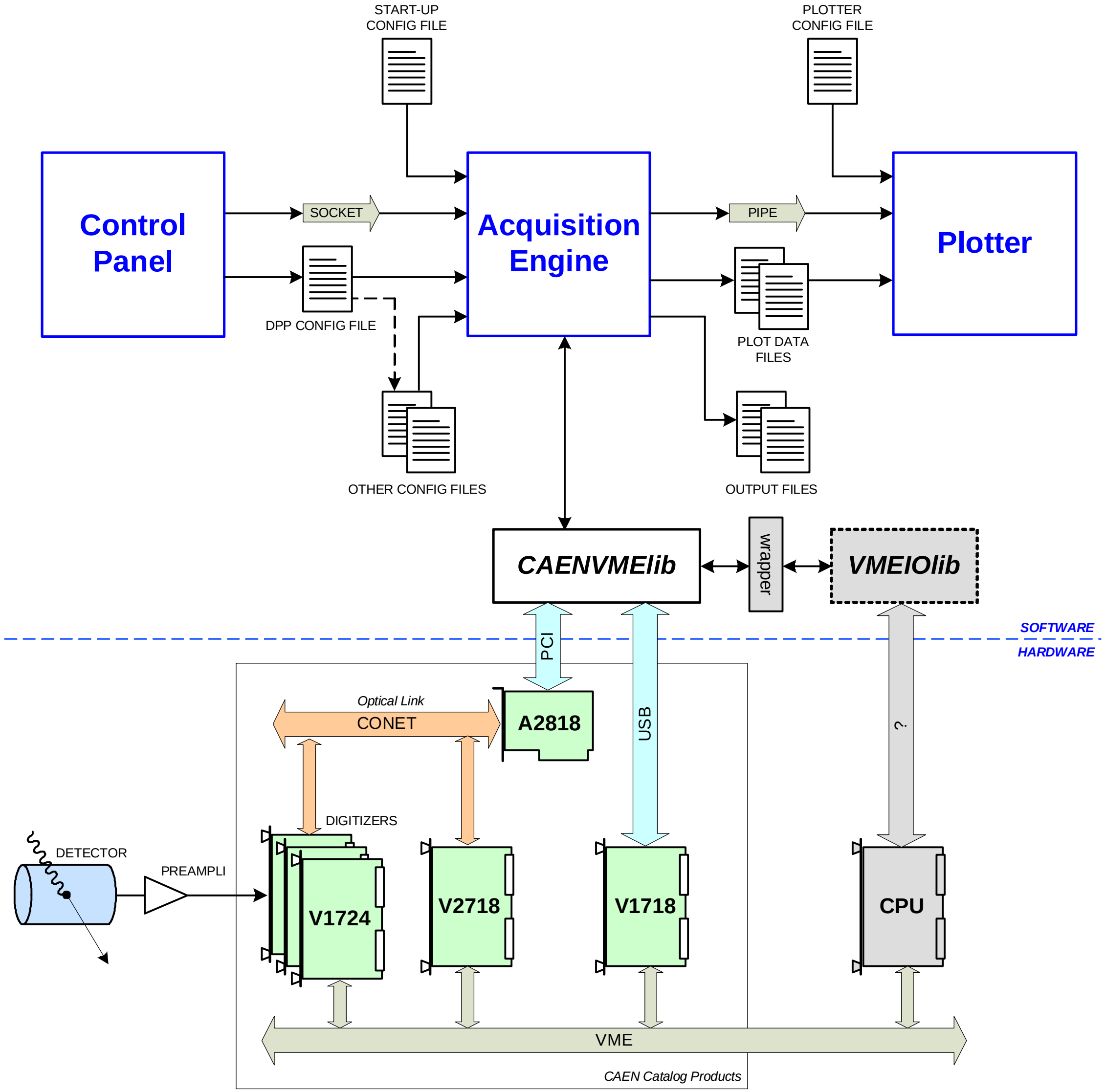
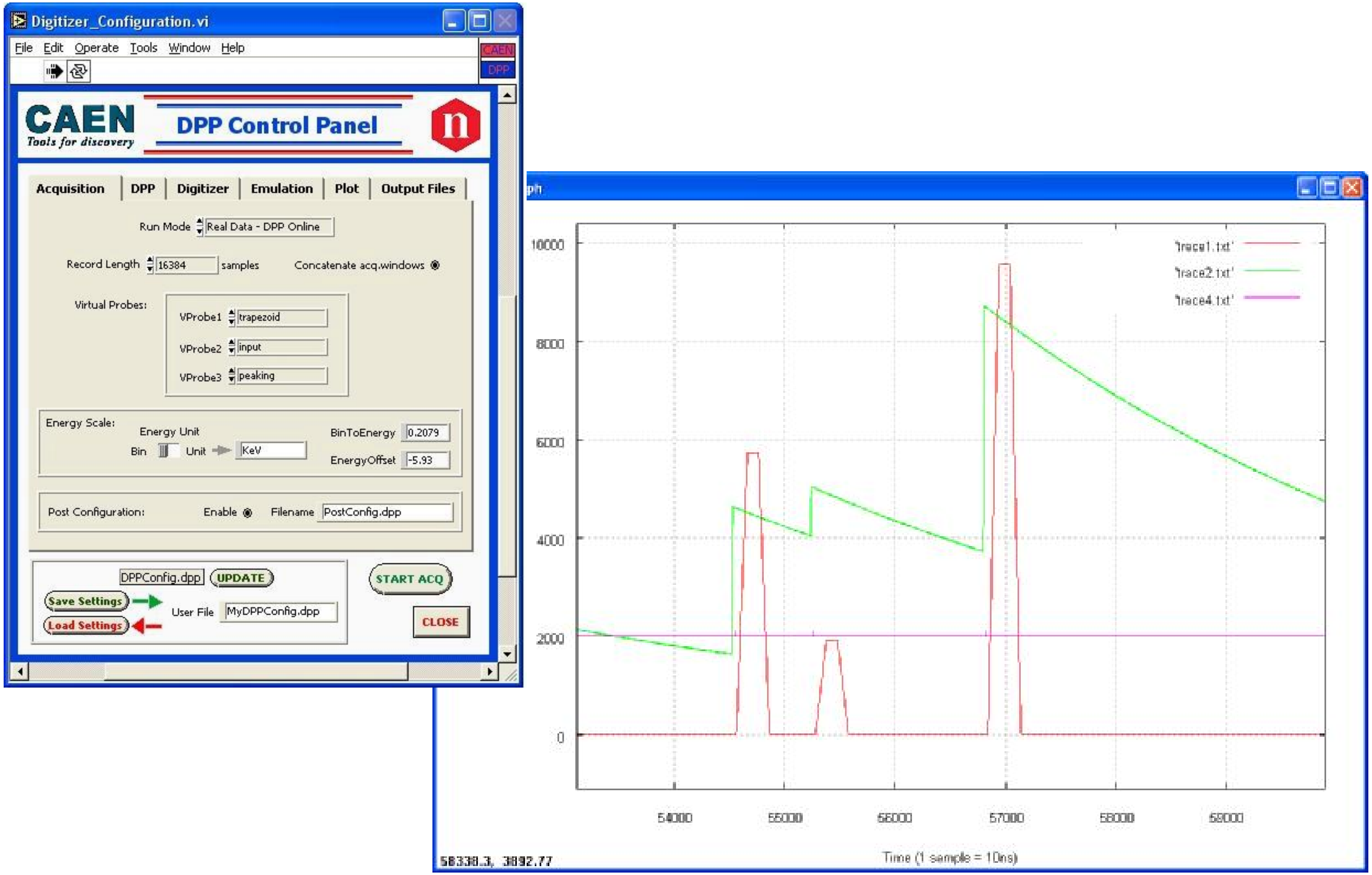
# DPPrunner block diagram



# Screenshots



# Tests with Germanium Detectors

**Nov 2008, Feb 2009: Laboratori Nazionali di Legnaro (Padova – Italy)**

**May 2009: GSI (Darmstadt - Germany)**

- Detector: GAMMA-X Germanium (Model ORTEC GMX 20200-S)
- Detector Resolution: 1.90 KeV fwhm (@1.33 MeV)
- Source: $^{60}Co$
- Measured and comparison of energy resolution @ 1.33MeV using
  - Digital Pulse Processing (using CAEN V1724 with Trapezoidal Filters )
  - Analog chain (using CAEN N968 Shaping Amplifier and N957 8k MCA)
- Acquisition rate: from 300 Hz to 3KHz
- Charge Sensitive Preamplifier features:
  - 0.1mV/Kev
  - Decay time: 50 us
  - Rise time: 100 ns

Acknowledgements
Enrico Fioretto (LNL)
Henning Shaffner (GSI)

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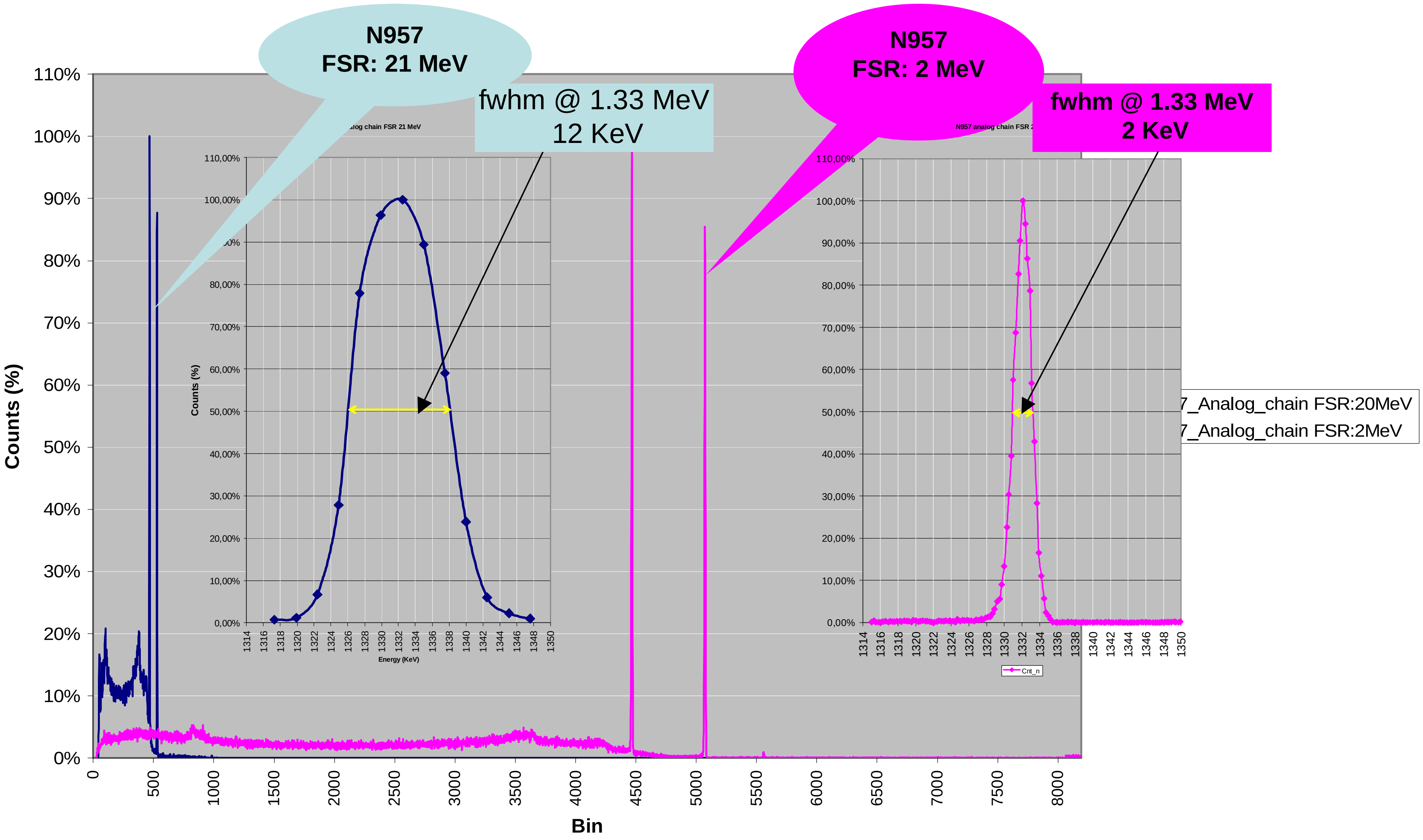
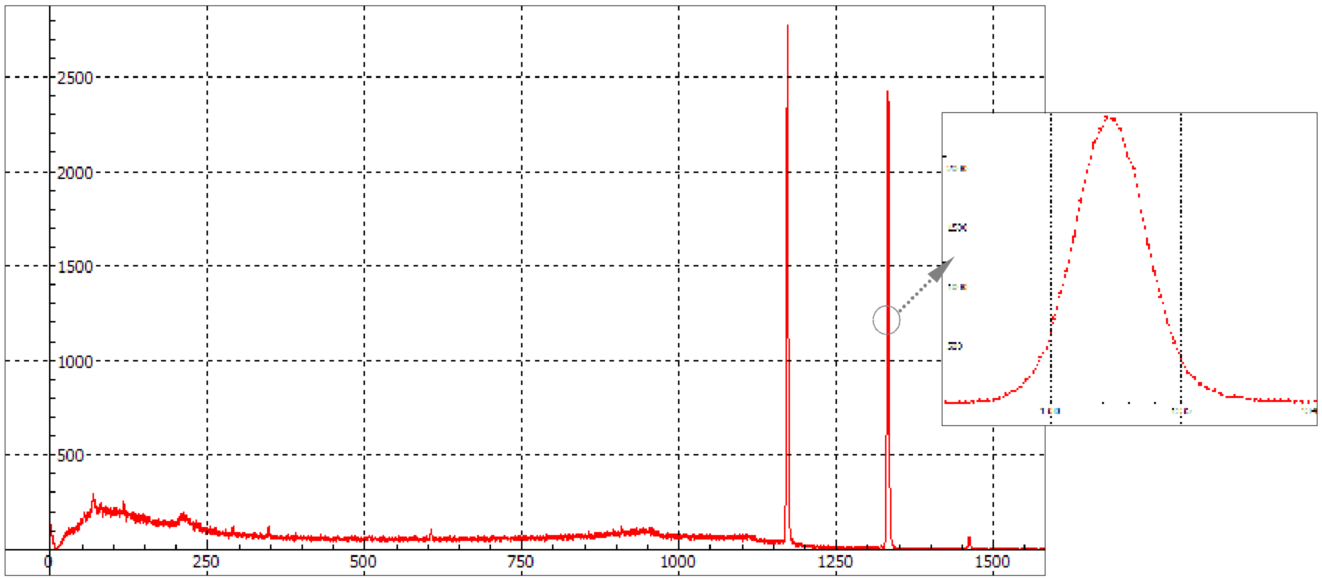
# N957 Spectrum *(Analog chain)*



# V1724-DPP Spectrum

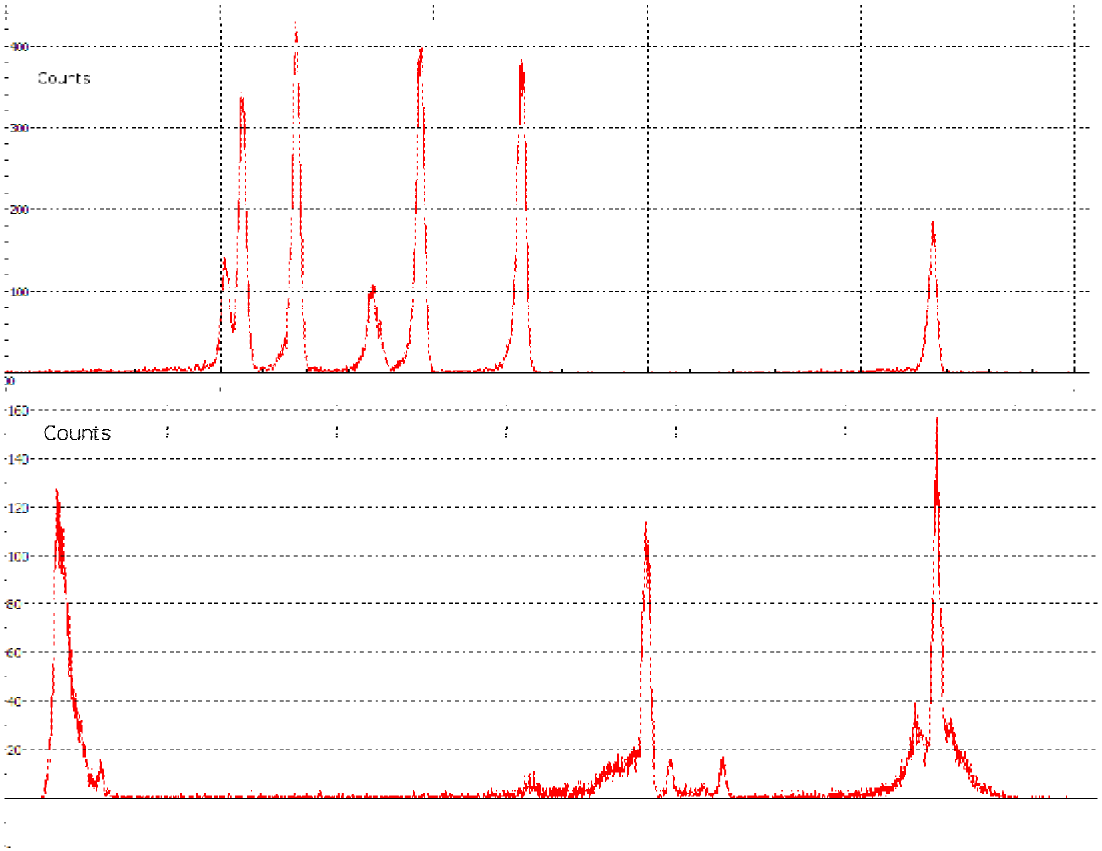
- V1724 standard: 2.25Vpp (Gain=1)
  - FSR: 30 MeV
  - Resolution @ 1.33MeV: 3.6 KeV fwhm
- V1724 modified gain: 220mVPP (Gain ~ 10 )
  - FSR: 3.34 MeV
  - Resolution @ 1.33MeV: 2.3 KeV fwhm



# Tests with Silicon Strip Detectors

**Mar 2009: Lund University (Sweden)**

- Detector: SSSSD and DSSSD
- Sources: $^{228}$Th and $^{207}$Bi
- Digitizer: V1724 with trapezoidal filters

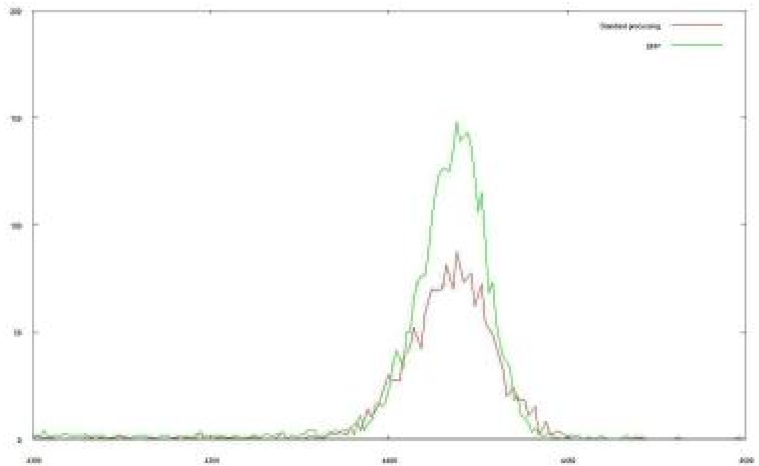


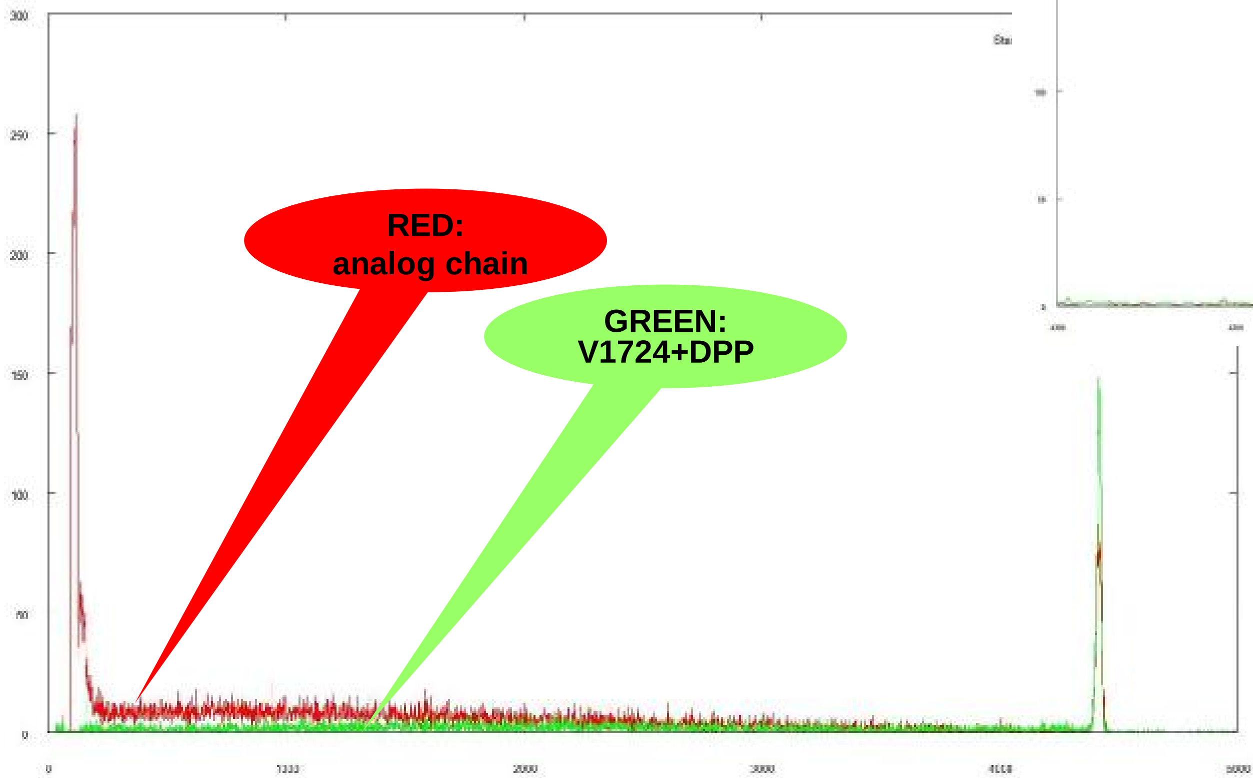

Acknowledgements
Pavel Golubev

# Tests with Cesium Iodide Detectors

**Apr 2009: The Svedberg Laboratory (TSL) (Uppsala - Sweden)**

- Detector: CsI(Tl)/PD - Cesium iodide Crystal doped with Thallium
- Ion beam test
- Digitizer: V1724 with trapezoidal filters





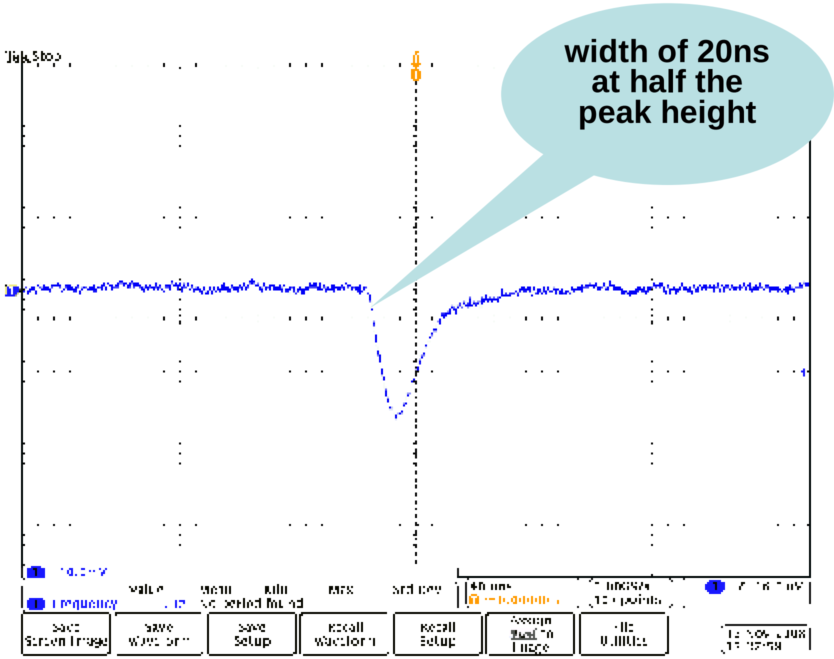


Acknowledgements
Pavel Golubev

# Tests with Silicon Photomultipliers

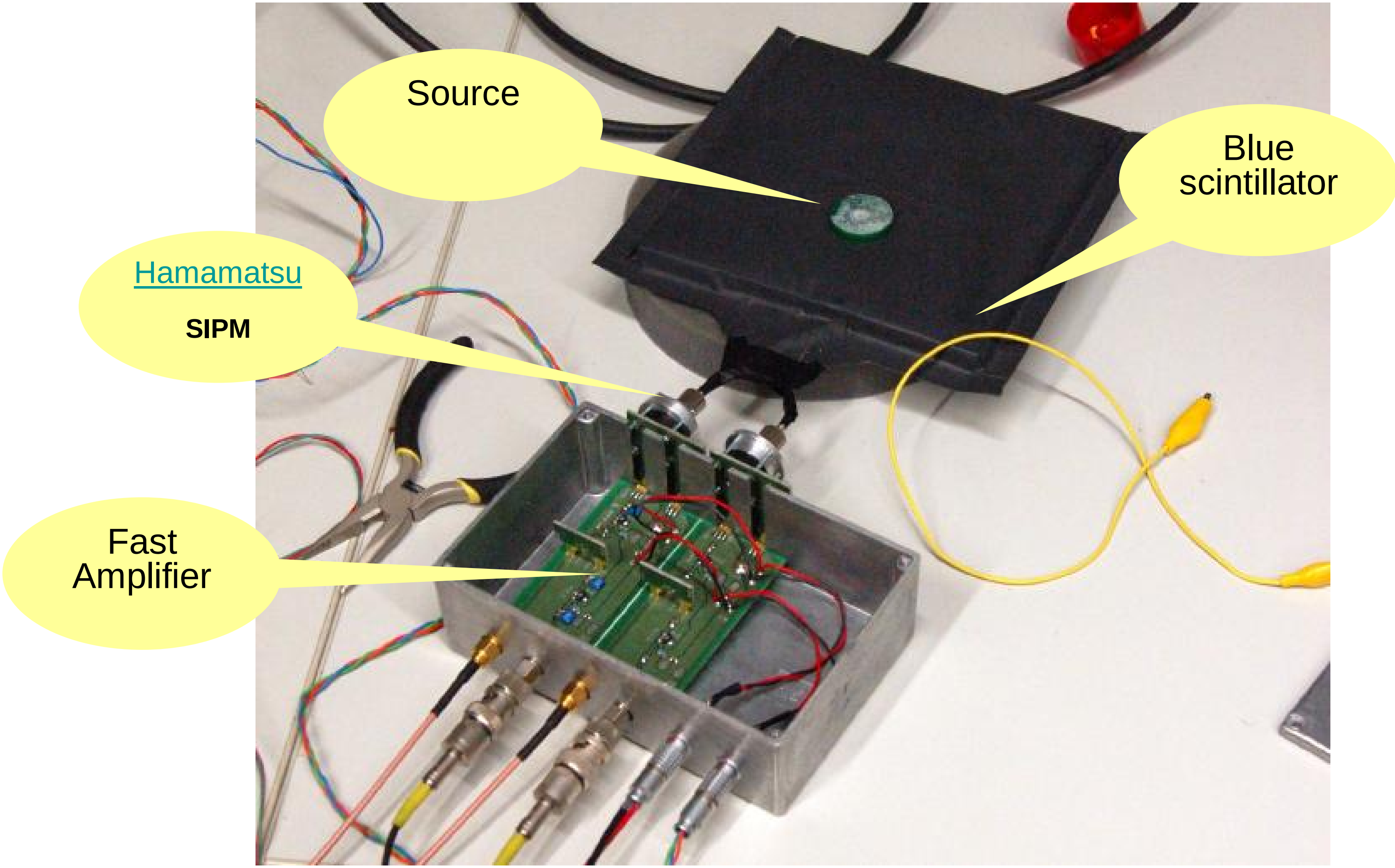
**May 2009: Università dell'Insubria (Como – Italy)**

- Detectors: scintillator tile coupled with
  - SensL SiPM (9k cells, 3x3 mm2)
  - Hamamatsu SiPM (400 cells, 1x1 mm2)
- Fast amplifier output feeding the input of the V1720
- Tested algorithms for the Digital Charge Integration

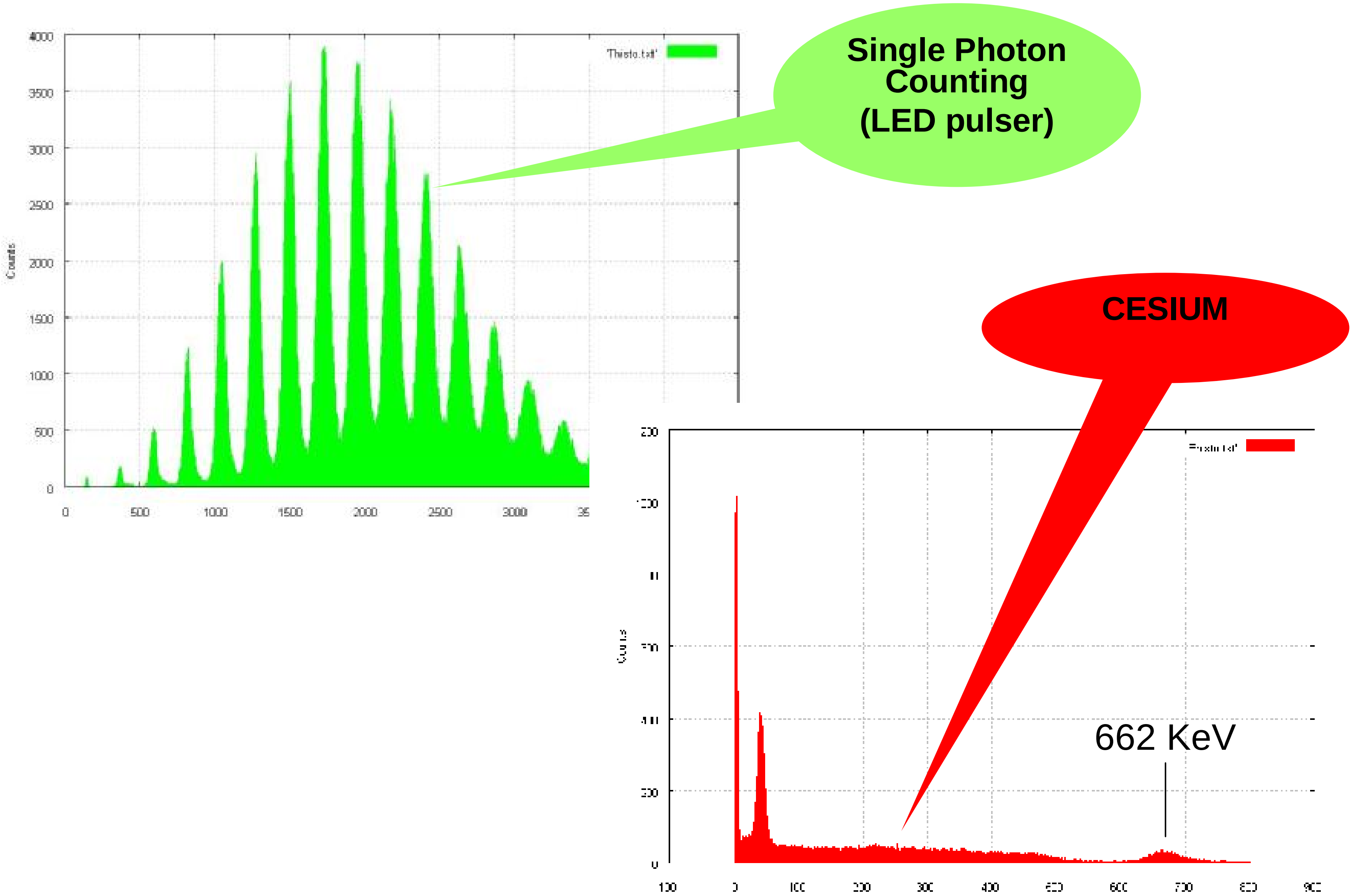



Acknowledgements
Massimo Caccia

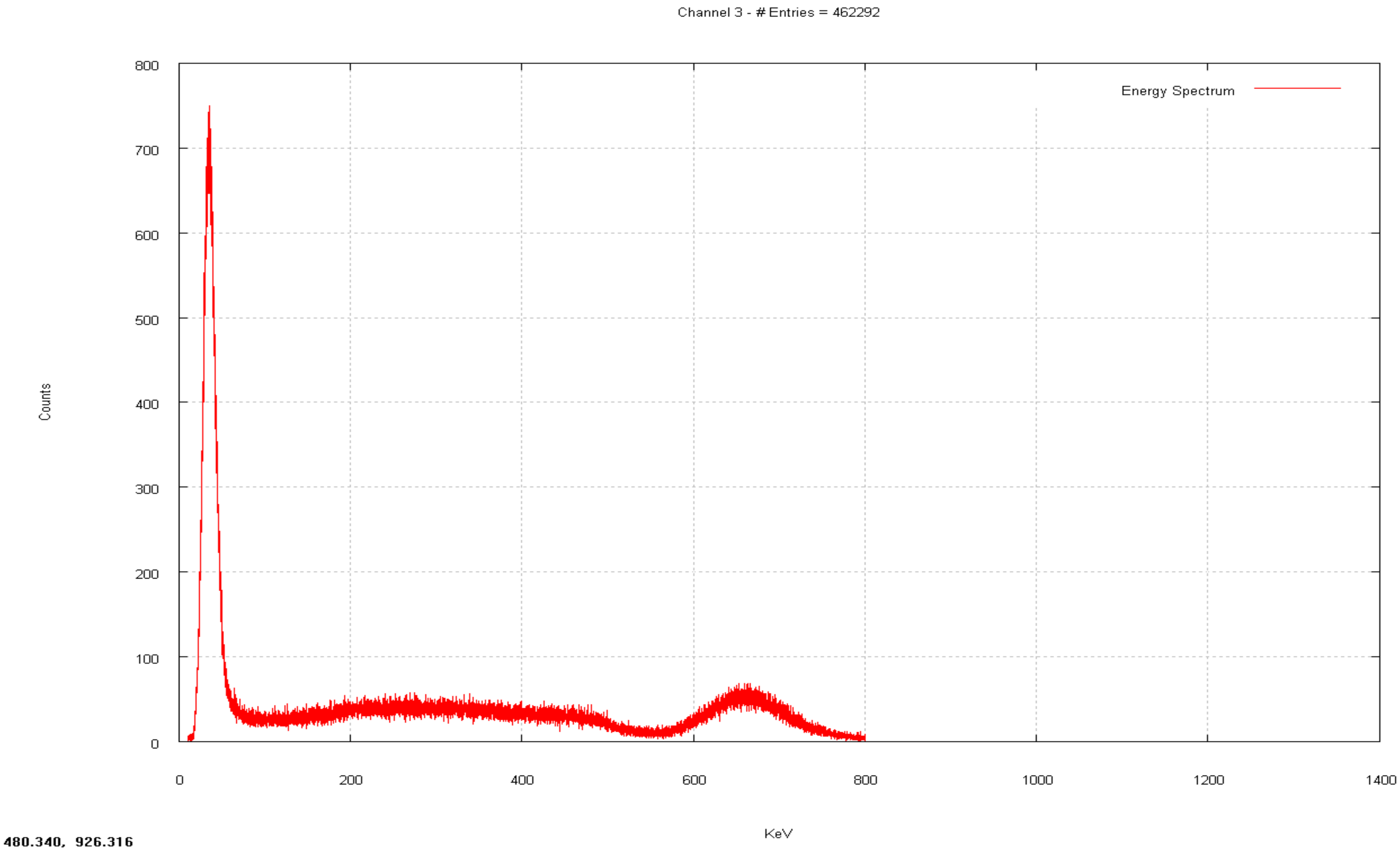
# SiPM test setup



# SiPM test results



# Lyso+SiPM



Channel 3 - # Entries = 462292
Energy Spectrum
Counts
0
100
200
300
400
500
600
700
800
0
200
400
600
800
1000
1200
1400
KeV
480.340, 926.316

# Conclusions

- The waveform digitizer is a general purpose equipment; you need dedicated hardware, firmware and software to tailor it to the specific application (system integration)
- Some vendors sell the simple hardware, other vendors sell the full system
- CAEN stays in the middle and aims to be a solution provider selling the building blocks and supporting the customers to integrate them in their systems