CLAS12 Trigger System: Level 1

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Plans

- Algorithms development (CLON,Fast El.) - in progress
- FPGA implementation (Fast El.)
- Efficiency studies (CLAS offline)

EC algorithm description

For cluster reconstruction purposes EC can be considered as 3 planes called U, V and W, crossing each other at 120 degrees (see figure 1). Each plane has 36 strips, each strip equipped with PMT to be connected to individual Flash ADC channel. EC cluster finding procedure includes following steps:

Step 1: threshold[0] applied to the energies from individual strips; only strips with energies above threshold[0] reported to the following step in a form of STRIP(strip number, strip energy)

Step 2: each plane is scanned searching for 1-dim peaks, defined as ‘group of one or several neighbor strips with energy above threshold[0] separated from another groups by at least one strip with energy below threshold[0]’ (see figure 2). Energy sum and weighted coordinate are calculated for every peak, and peaks with energy above threshold[1] are reported to the following step in a form of PEAK(peak ‘center’ strip number, peak energy)

Step 3: 1-dim peaks from each of three planes are processed using following simple formula: (37-delta)<=(U+V+W)<=(37+delta) (see figure 3). If three peaks from 3 planes satisfies to that formula they considered as parts of one 2-dim cluster. Energy sum and weighted coordinate are calculated for every 2-dim cluster, and clusters with energy above threshold[2] are reported as final result in a form of CLUSTER(three cluster ‘center’ strip numbers, cluster energy)

Described algorithm works in online and offline data processing for years. Now we should try to implement something like that into Level1 trigger electronics.

Figure 1: EC (Forward Calorimeter)

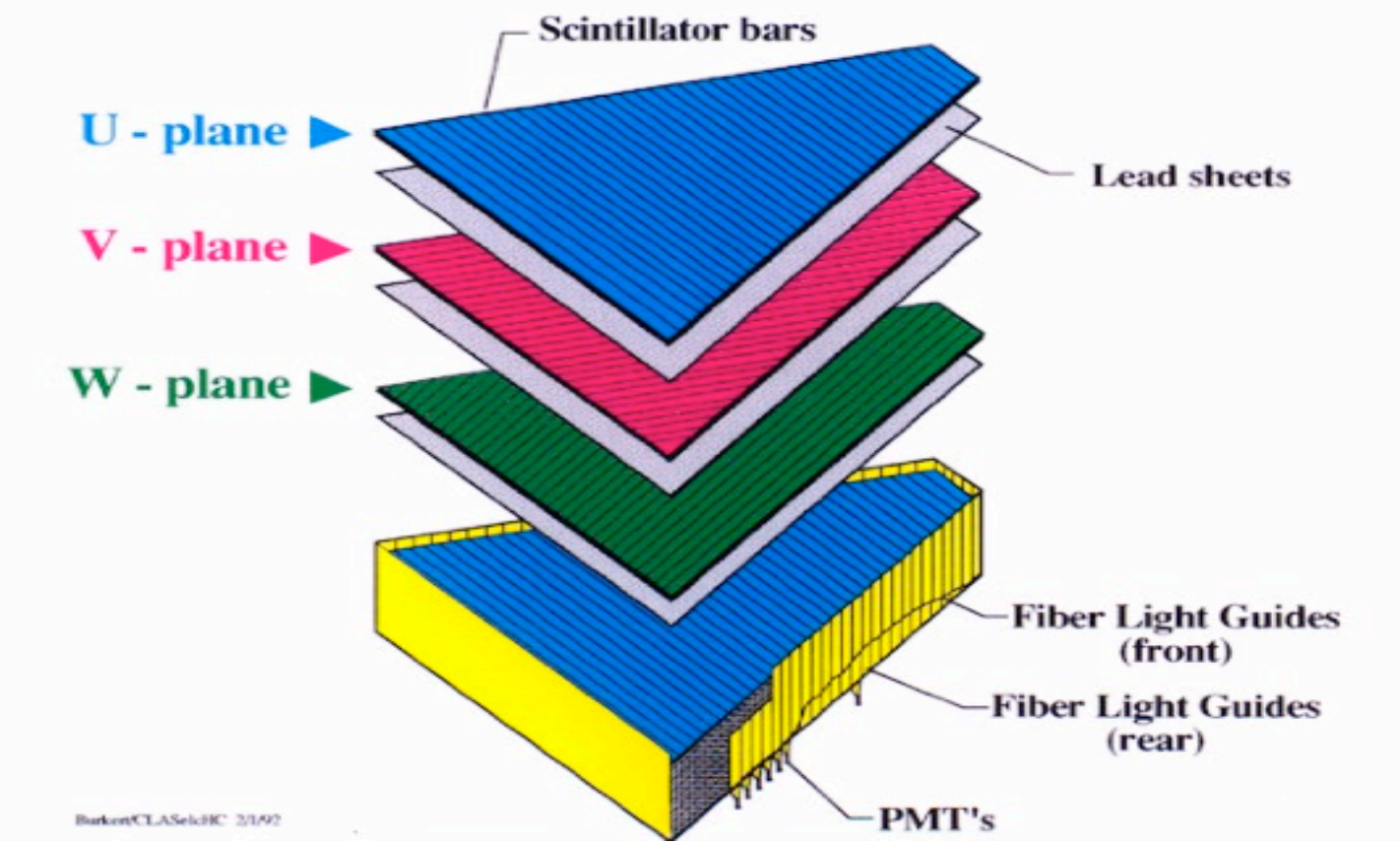


Figure 2:
1-dim peaks
(example)

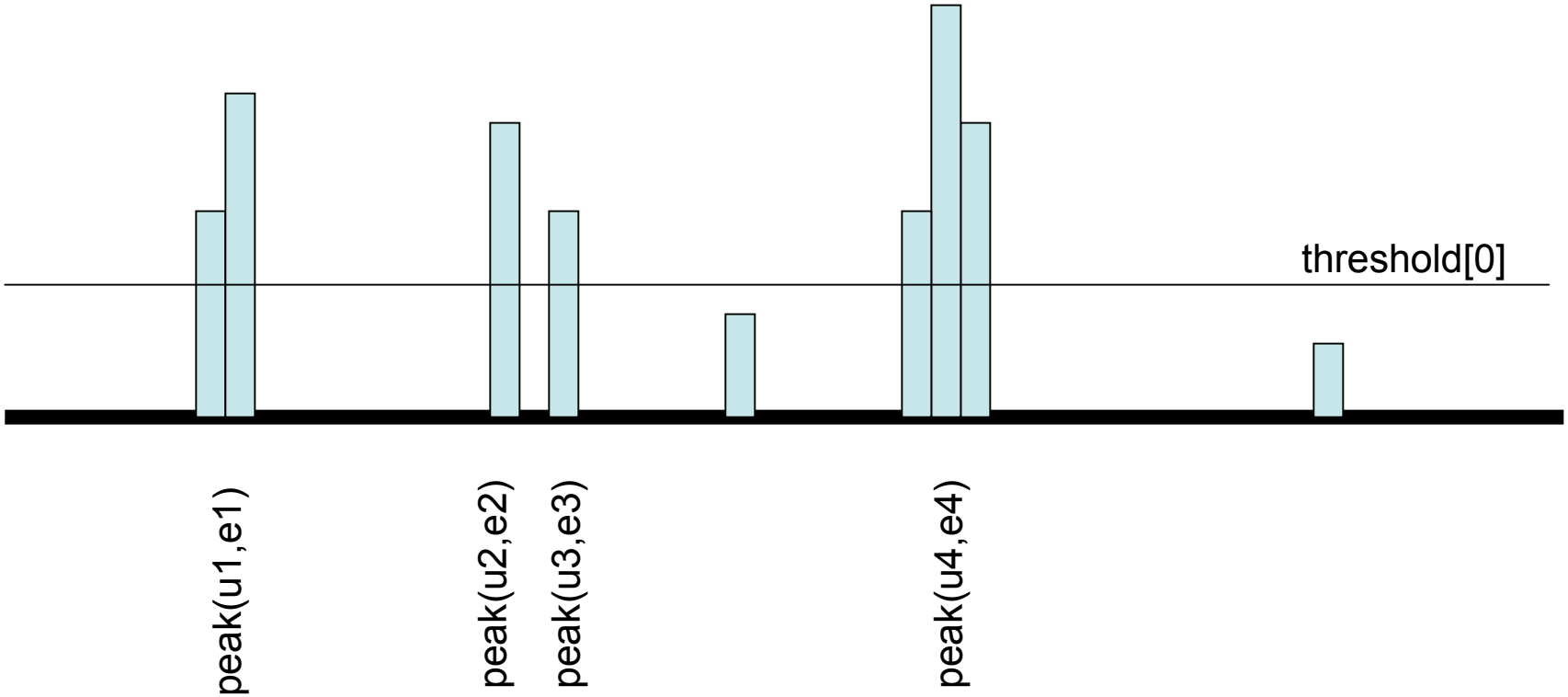
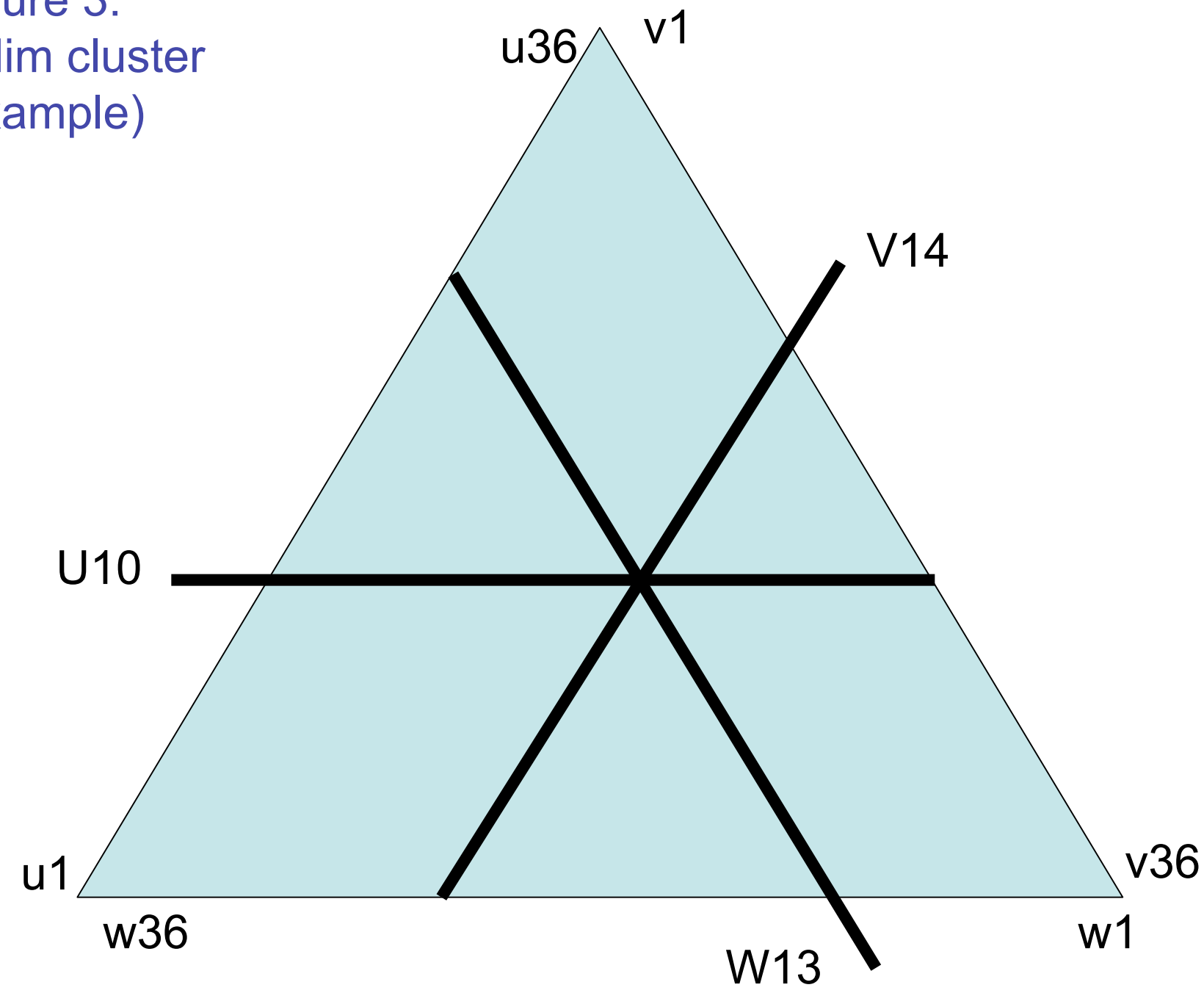


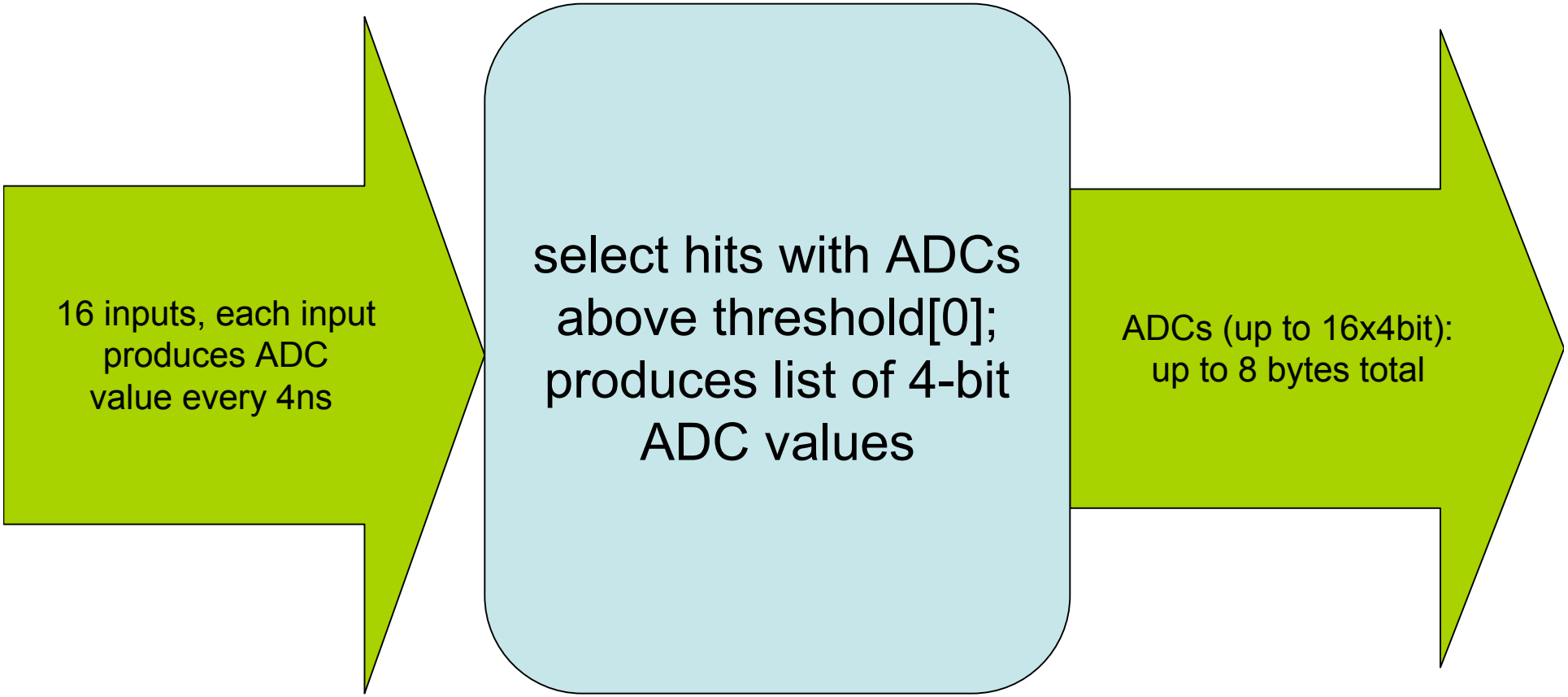
Figure 3:
2-dim cluster
(example)



Level1: Forward Calorimeter Cluster Finding

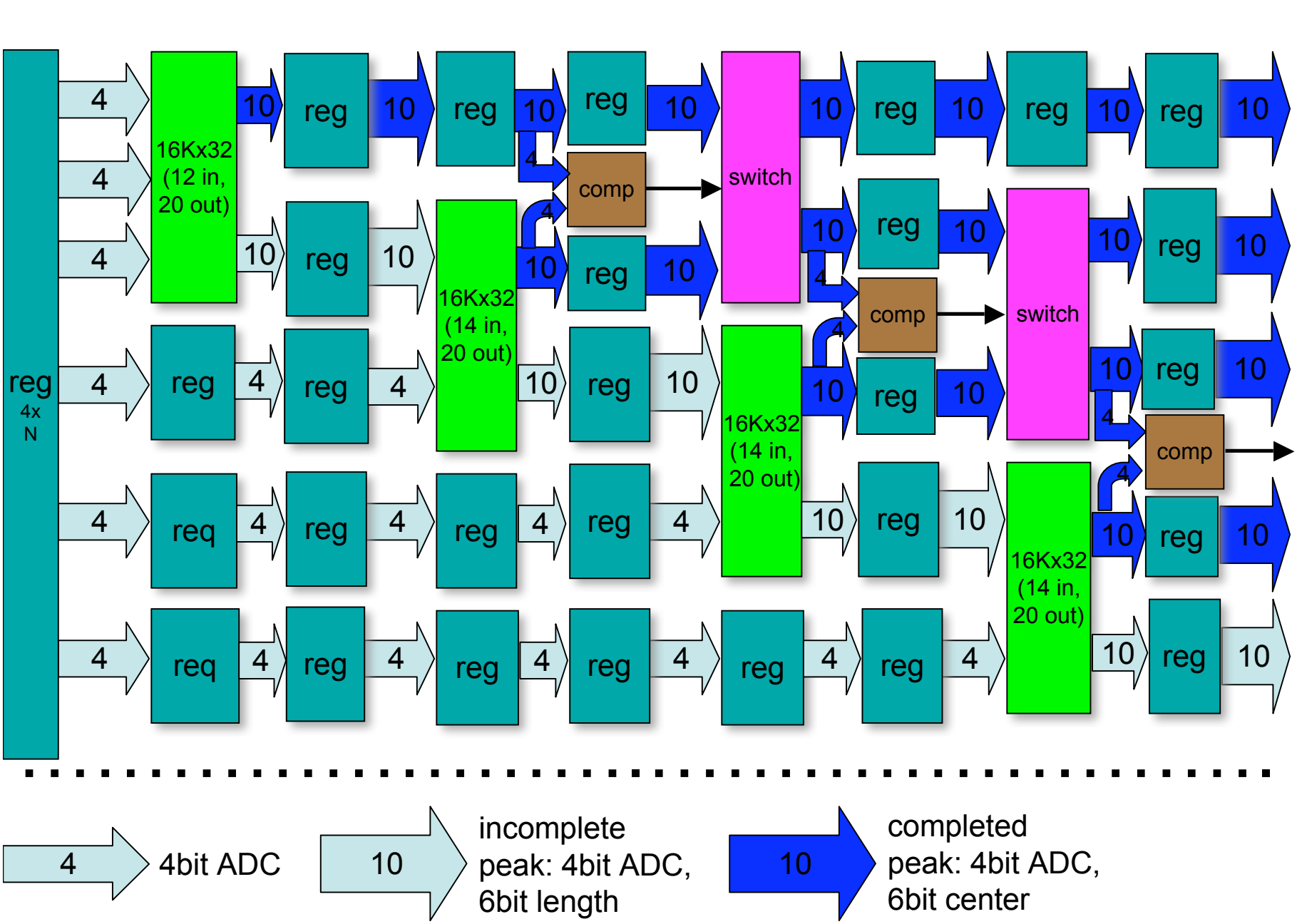
- 16-channel Flash ADCs
- 21-slot crate: 16 FADC boards, dual-width processing unit, CPU, TI
- 256 channels maximum, we need 216 per sector

Level 1, Stage 1: FADC board, 4ns event clock

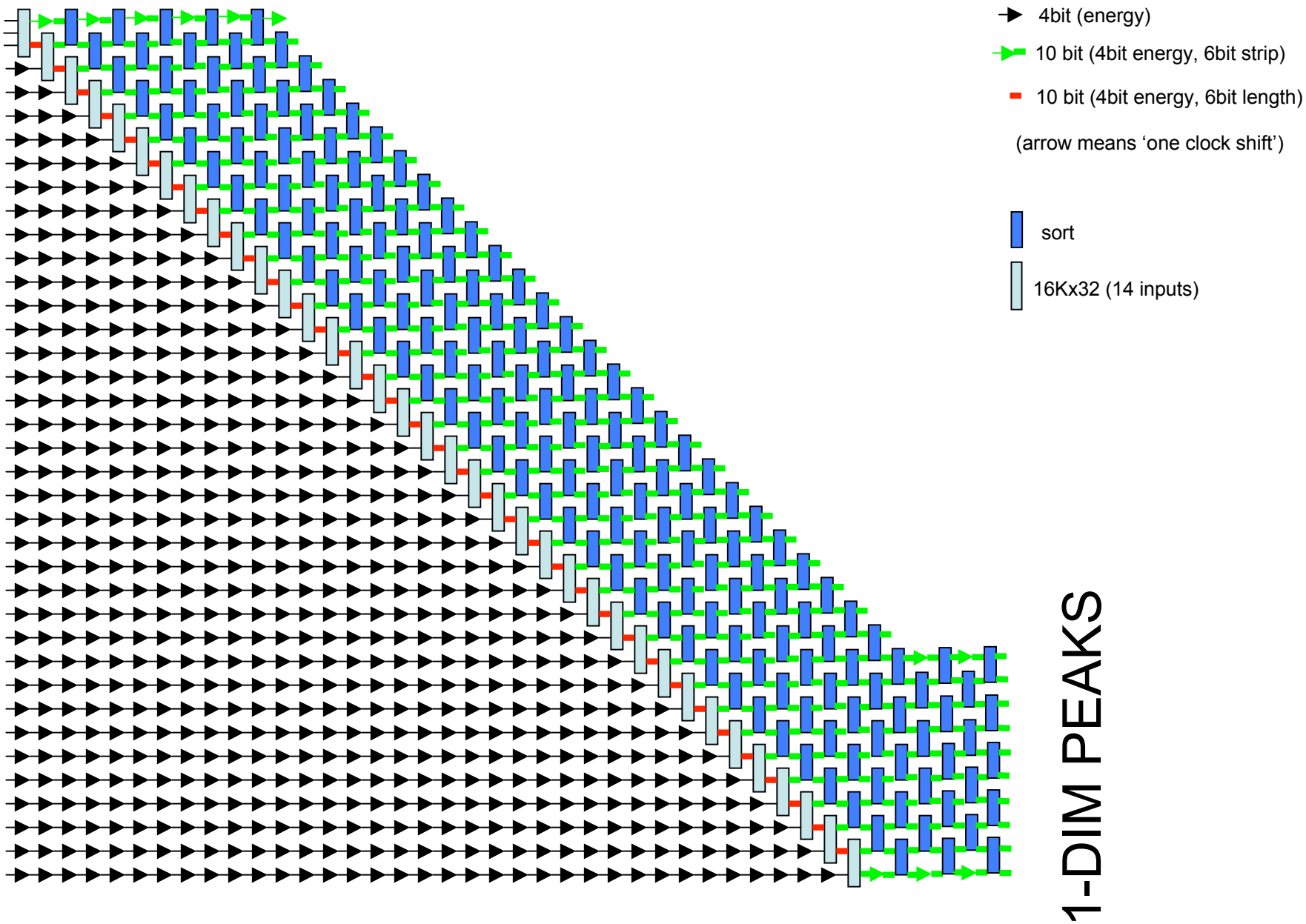


NOTE: 10GBit link can transfer 8bytes in 8ns, so following processing units may have 8ns event clock; BUT: average number will be less, so buffering and/or compressing should help

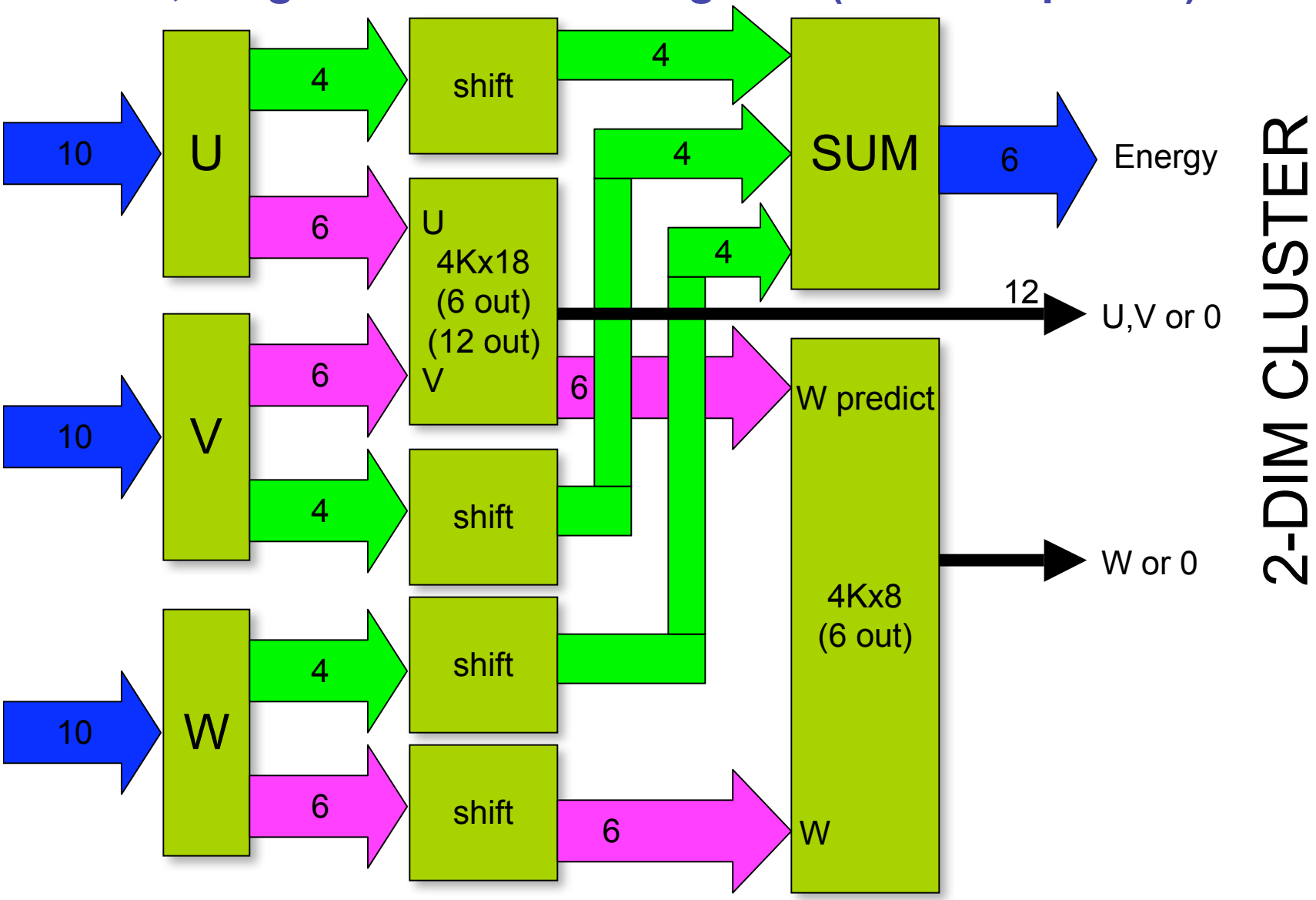
Level 1, Stage 2: Peak Finding Unit (N inputs from FADCs)



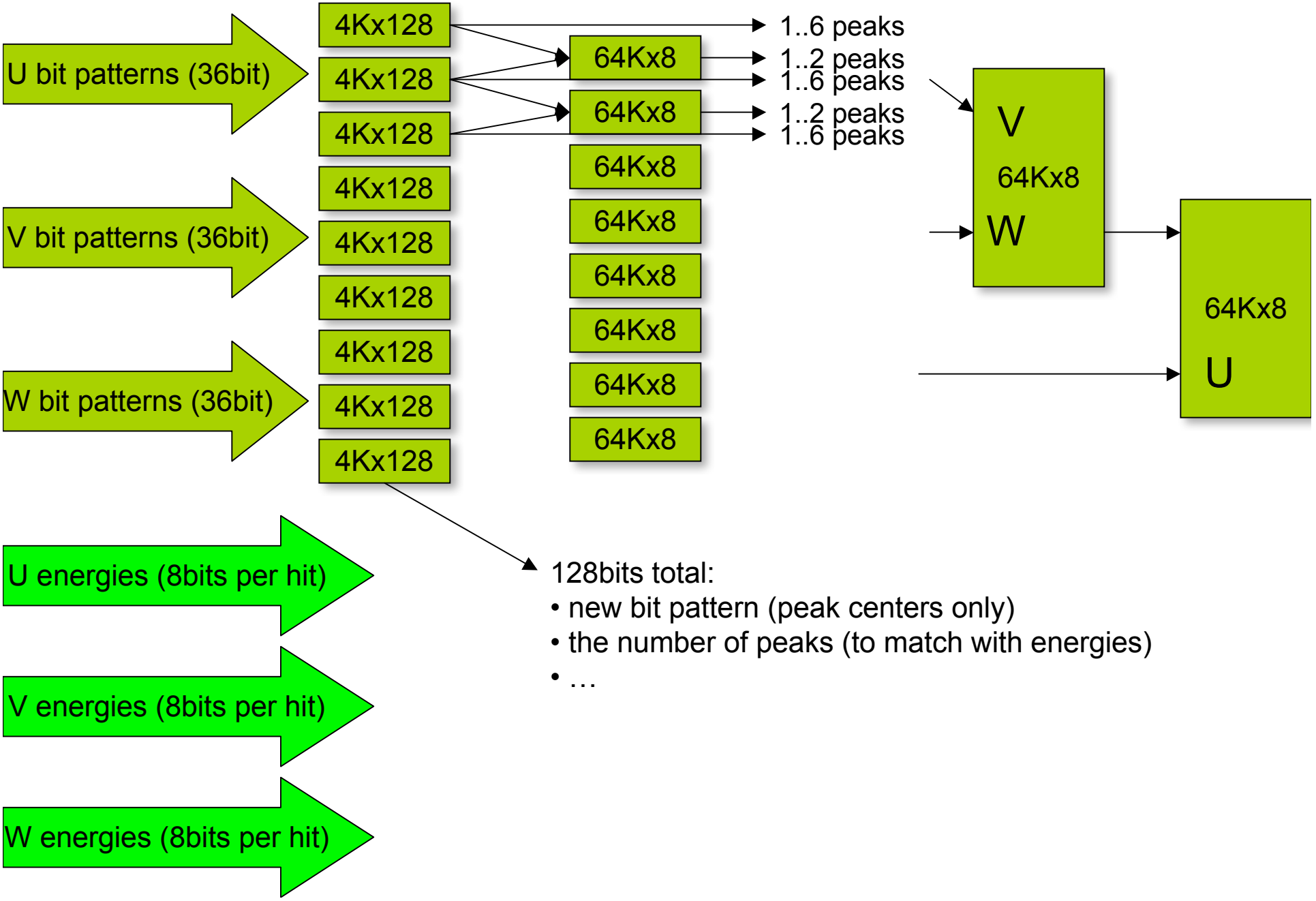
Level 1, Stage 2: Peak Finding Unit (one EC plane, 36 inputs)



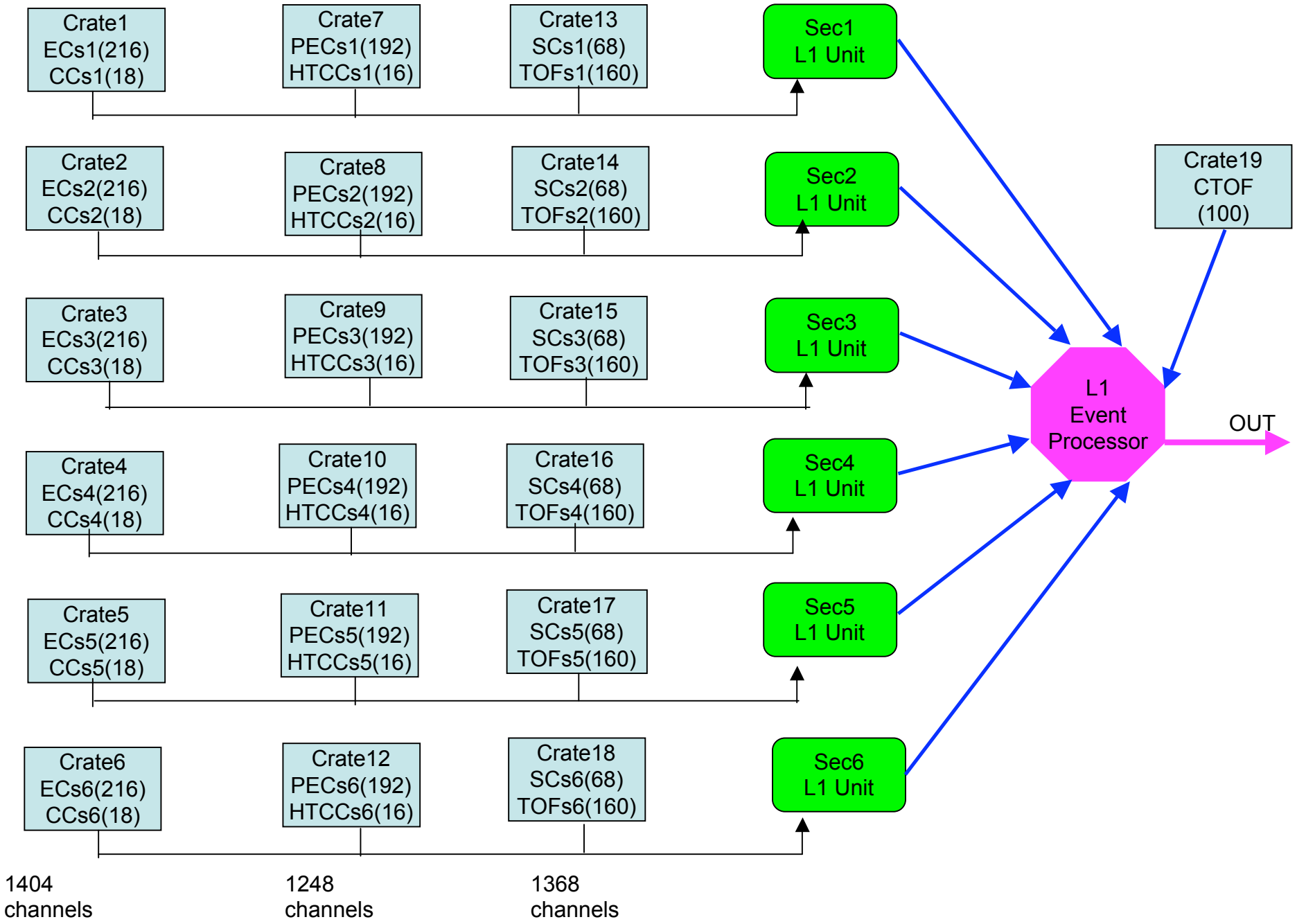
Level 1, Stage 3: Cluster Finding Unit (three EC planes)



Level 1, Stage 2+3: Peak and Cluster Finding Unit (three EC planes)



Level 1, generic scheme: 4120 FADC channels (1812 old, 2308 new)



TO DO: FPGA implementation

- Fast Electronic Group experts
- Some level of knowledge for CLON group is required

TO DO: Efficiency studies

- Electron identification using energy cuts and cluster finding in both calorimeters in conjunction with hits in time-of-flight and cherenkov counters
- Proposed algorithms must be tested using existing data